IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 8, Issue 3, Ver. I (May.-June. 2018), PP 25-30
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

CMOS Design of Wideband Inductor-Less LNA

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Abstract: *With the current trend of ever developing communication systems, and every communicating system consisting of an antenna and receiver requires foremost a Low Noise Amplifier with a good gain and as well contributing to not much noise, hence LNA design has been an ever challenging task to Analog designers. With this work a wideband, inductor-less LNA with noise canceling technique is examined and designed in 45-nm CMOS process. The proposed LNA combines two techniques, resistive feedback and noise cancellation to provide both a wideband input match and good noise performance. The result is a wideband, differential LNA without any need for external matching components. As the solution is inductor-less hence saves valuable area on chip. The LNA covers frequency bands within 0.1 – 2GHz a voltage gain of 24.7 dB. The NF is below 3.46 dB with a power consumption of only 6 mW. This solution has many features such as high bandwidth with a good input match, inductor-less design saving area and cost.*

Index Terms: *Inductor-less, Low Noise Amplifier (LNA), Low Area, Wideband.*

Date of Submission: 30-05-2018 Date of acceptance: 17-06-2018

I. Introduction

Today everywhere around us radio signals and systems co-exist and operate side by side such as GSM, 3G, WLAN, Bluetooth, FM-radio and many more. The demand for power efficient, accurate and small transmitters and receivers is ever growing and s big research area worldwide. LNA stands for Low Noise Amplifier, the first stage in any receiver after the antenna. With sole purpose to amplify the desired signal as much as possible without adding noise or consuming much power. Hence by Maximum power transfer theorem we require to obtain a good impedance match between the antenna and the LNA input. And the conventional solution has been to use inductors on-chip and as well off-chip to achieve the same. Because of the resonance circuits the bandwidth for this type of LNA is low and cellular phones must be able to receive signals at wide range of frequencies. In current handsets the solution is to implement a number of [6] LNAs to cover the whole bandwidth. A switch activates the appropriate LNA according to the frequency to be received. In this solution each LNA has its own inductors which gives good gain and low noise at the price of large chip area. Inductors use a lot of area on chip and all the matching components off chip utilize valuable PCB area. To make matters even worse inductors on chip require expensive manufacturing steps to get a high Q.

The analog part of a basic radio system consists of an antenna with an impedance of 50, duplexer, receiver and a transmitter. This work focuses on the receiver part of the system, when a signal is received at the input of the receiver the frequency is between 100 MHz and 2 GHz and would have maximum amplitude of -26 dBm. The incoming signal is first amplified by an LNA. The output of the amplifier is then down converted in a mixer which uses a local oscillator, synchronized in frequency to the carrier of the desired signal. Finally the baseband signal is amplified and can be used in the rest of the system. To amplify such low signals it is crucial that the input stage (LNA) itself does not contribute with noise and distortion that could destroy the input signal. In today's solution the mixer is passive due to the linearity requirement. A passive mixer leads to a loss in signal amplitude and put an even higher requirement of the LNA gain.

II. Literature

Important parameters in a LNA design are Noise Figure, Matching, Gain, Stability and linearity [6].

A. Noise Figure

Noise Figure (NF) is a measure of Signal to Noise R degradation as the signal travels the receiver front-end. Mathematically, NF is defined as the ratio of the input SNR to the output SNR of the system. NF may be defined for each block as well as the entire receiver. Generally it is not possible to obtain minimum noise figure and maximum gain for an amplifier, and so it is always a trade-off between the two. The value of NF below 5dB is considerable for a LNA design. And is the most important parameter of an LNA.

B. Gain

Gain is a ratio between the output signal and input signal showing how much the signal can be amplified. It is usually defined in voltage, hence leading to the expression "voltage gain" and is often expressed in the logarithmic scale defined as

Gain= 20*log (V_{out} / V_{in}) dB

Another gain definition is power gain, which is defined as the output power to the input power. There are sub three power gain definitions that are more frequently used in RF applications. Figure1 illustrates the different powers coming in and out of an amplifier and the different gains. The definitions of each are as follows:

P_{AVS} - Power available from source
P_{AVN} - Power available from network
P_{IN} - Power delivered to the input
P_L - Power delivered to the load

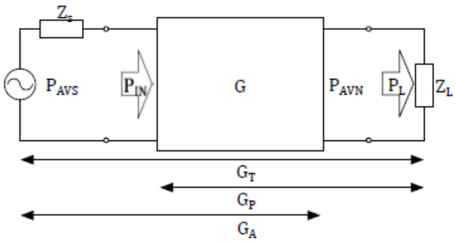

Figure 1

And the corresponding gains G_T, G_P, G_A are defined as follows
Transducer gain = $G_T = P_L \div P_{IN}$
Operating gain = $G_P = P_L \div P_{AVS}$
Available gain = $G_A = P_{AVN} \div P_{AVS}$

C. Matching

For maximum power transfer and best performance we require a very good matching between the input and output to source and load respectively. S-parameter is a tool that is used to describe e.g. matching and gain for a circuit.

S-parameter: Scattering Parameter

In Figure 2 a_1 is the incident wave at each port and b1 is the reflected but b_1 contains contribution from both incident wave a1 and a2, as they scatter through the two-port. From the figure we can write the s-parameter equation as

$$b1 = S_{11}a_1 + S_{12}a_2$$

$$b2 = S_{21}a_1 + S_{22}a_2$$

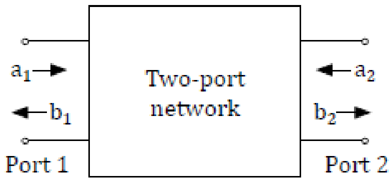

Figure 2

$$\begin{bmatrix} b1 \\ b2 \end{bmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{bmatrix} a1 \\ a2 \end{bmatrix}$$

S11 describes how much of a1 is reflected back through b1, it is a measure of how good the input matching is and also a measure of input impedance. S12 quantifies how much of a2 gets scattered through the system to reach till b1 and hence indicative of how good the isolation is from the output to the input. S22 is as similar to S11 but at the output, hence indicative of the output impedance. S21 is the measure of how much the incident wave at the input affects the reflected wave at the output and in simple how the input signal affects the output signal. A good amplifier would have a S11 and S22 low, S21 high and S12 equal to zero.

III. Wide Band Lna Design

In this work we propose a wide band LNA with resistive feedback and noise cancellation stage. A common source cascaded type amplifier is used in the input core.
The circuit diagram is as shown below figure 3.

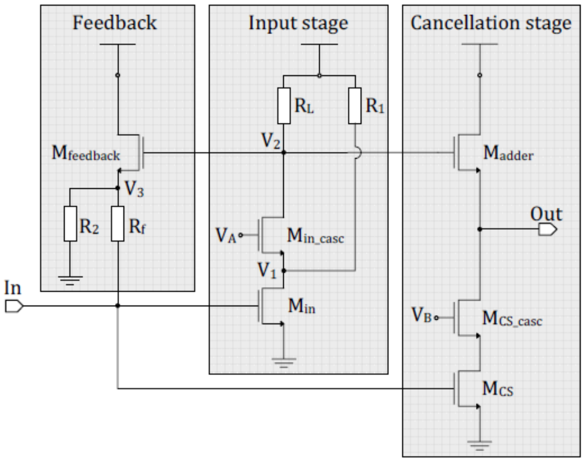

Figure 3: Proposed Circuit

D. Input Stage

Input stage is chosen as Common Source Stage with Cascode transistor, this technique is chosen due to its simplicity and relatively good performance in terms of noise and gain. And with using a cascode transistor [3] we obtain increased gain and input isolation and lower input capacitance. The input is biased through RL, which also serves as the load for the cascode. To ease the requirements on M_{incas} and to lower the voltage drop over the transistor, a resistor R1 is added as a current source to lead some of the drain current from M_{in} past M_{incas} and RL. This makes it easier to find good bias levels for the input stage but it also lowers the gain, as some of the ac current will pass through R1 instead of RL.

E. Negative Feedback

In amplifiers negative feedback is employed to improve stability and linearity. In this work the feedback is primarily to obtain a wideband input match. Instead of inductors as matching components the trans-conductance of the input stage is being utilized for the input match. From [3] a solution with an active feedback is presented and by using this technique, one can isolate the input from node V2 and improve the input match. The active feedback network is implemented using a source follower. This feedback has the drawback that it has gain below unity compared with a CS stage which contribute to more noise. The main advantage is a more stable circuit. The active feedback also increases the gain since it relaxes the load contributed by the feedback. Even though $M_{feedback}$ is introduced Rf is kept in the feedback loop for two reasons. First of all it gives one more variable to set for making the input match and second the feedback loop contributes less noise with a resistor. A resistor is the least noisy element and by adding Rf $M_{feedback}$ can be kept smaller, thus there is less noise introduced in the feedback. To prevent DC current from going through Rf , which will lead only to higher current consumption in the source, a DC bias is placed between the source of the transistor and the resistor Rf .

F. Noise Cancelling

All of circuit elements contribute to noise and once added it becomes not possible to remove it. The design goal has always been to minimize the amount of so generated noise within each element and thus get a low NF [2]. Referring to figure 4, we see that if the high frequency signals are noise and the others is the desired signal then the output would only contain the desired signal while the noise is eliminated. If it is possible to create two nodes where the signal has the same phase and the noise has the opposite then noise canceling would be possible.

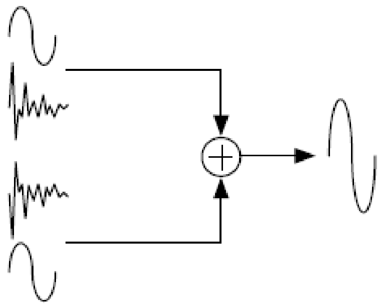

Figure 4: Basic noise canceling theory

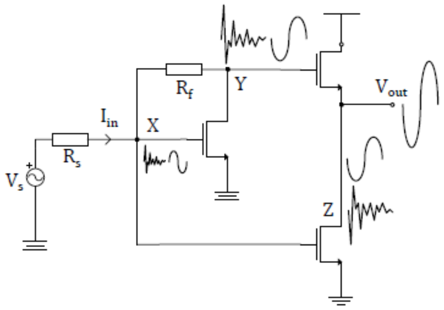

Figure 5: Basic noise canceling circuit with CMOS devices

IV. Results

Figure 6 shows the detailed circuit diagram for the LNA amplifier as designed on cadence. Figure 7 shows the test bench circuit employed for analyzing the gain, noise figure and s- parameter calculation on the tool. Figure 8 is implicative of gain achieved by the so proposed circuit and is well above 24 dB. While figure 9 is indicative of noise figure achieved by the LNA and is well below 2.45dB for frequencies of 0.1 to 2 GHz

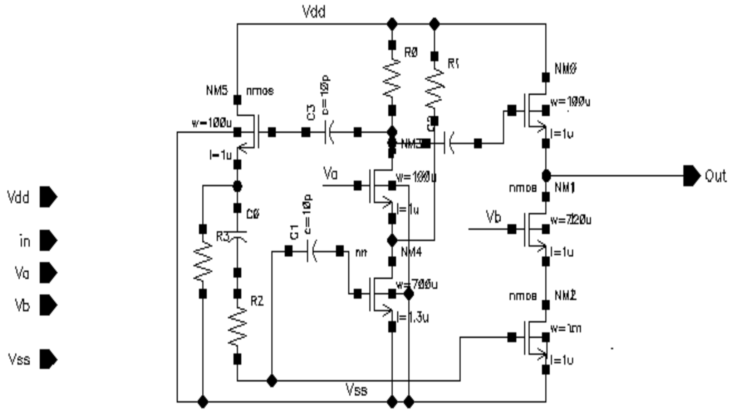

Figure 6 LNA Amplifier Circuit in 45nm Tech node

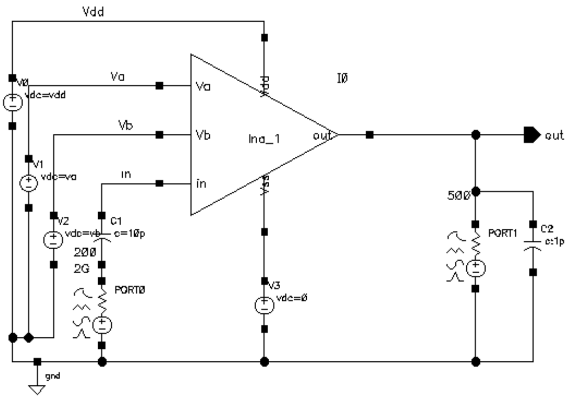

Figure 7: LNA Test Bench

Table 1 Comparison with referred works [2], [3], [4]

Specifications	[2]	[3]	[4]	This Work
Gain (dB)	13.7 dB	25.2 dB	21 dB	24.69 dB
S11 (dB)	<-8 dB	<- 15 dB	<-12 dB	<-12 db
NF (dB)	2	2.6	2.5	3.46
Power (mW)	35	42	21	27

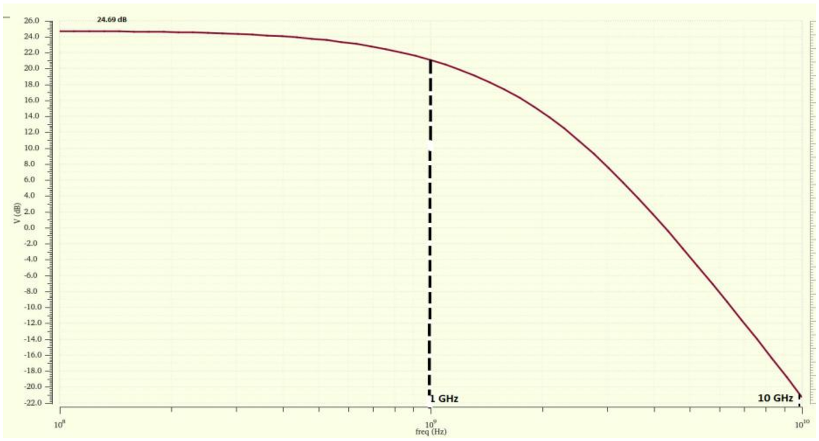

Figure 8: Gain in dB

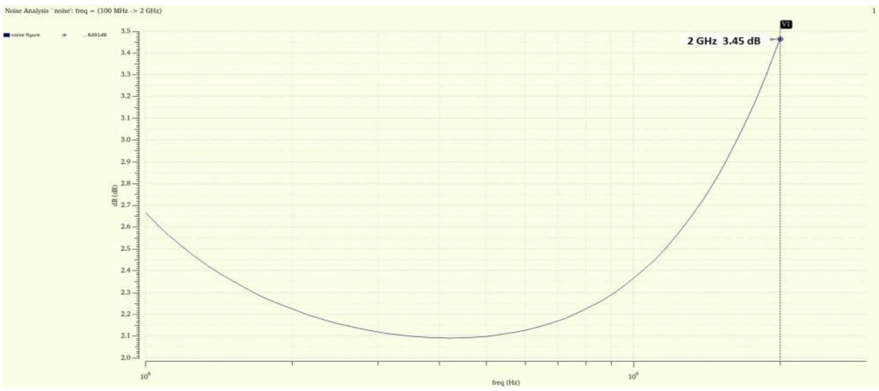

Figure 9 Noise Figure

V. Conclusion

The proposed circuit is implemented on cadence 45nm technology node and obtained a gain of 24.69 dB with noise figure well below 3.45dB for 0.1 to 2 GHz of frequencies.

Acknowledgement

This work is been carried out as a part of DRDO sponsored research work in the department. We are grateful to DRDO for providing resources.

References

[1]. S. C. Blaakmer, E. A. M. Klumperink, D. M. W. Leenaerts, B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling", IEEE J. Solid-State Circuits, vol. 43, No. 6, Jun. 2008.

[2]. F. Bruccoleri, E. A. M. Klumperink, B. Nauta, "Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling", IEEE J. Solid-State Circuits, vol. 39, No. 2, Feb. 2004

[3]. B. G. Perumana, J. C. Zhan, S. S. Taylor, "A 5 GHz, 21dB dBm Output-IP3 Resistive Feedback LNA in 90-nm CMOS", IEEE, 33rd European Solid State Circuits Conference, 2007. ESSCIRC

[4]. S. C. Blaakmer, E. A. M. Klumperink, D. M. W. Leenaerts, B. Nauta, "The BLIXER, a Wideband Balun-LNA-I/Q-Mixer Topology", IEEE J. Solid-State Circuits, vol. 43, No. 12, Dec. 2008.

[5]. B. Razavi, 2005, "Design of Analog CMOS Integrated Circuits", McGraw-Hill Higher Education (1 Oct 2003), ISBN 0-07-238032-2

[6]. T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press; 2 edition (22 Dec 2003), ISBN 978-0521835398

[7]. P. H. Young, Electronic Communication Techniques, Prentice Hall; 5 edition (28 Aug 2003), ISBN 0-13-048285-4

[8]. Gray, Hurst, Lewis & Meyer: "Analysis and Design of Analog Integrated Circuits, 4th Edition", John Wiley & Sons, 2008

[9]. F. Bruccoleri, E. A. M. Klumperink, B. Nauta, Wideband Low Noise Amplifiers Exploiting Thermal Noise Cancellation, Springer, ISBN 1-4020-3187-4

Dr. Jamuna S. "CMOS Design of Wideband Inductor-Less LNA." IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) , vol. 8, no. 3, 2018, pp. 25-30