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Implementation of Low Power CMOS Full Adders Using Pass Transistor Logic

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Abstract: *The efficiency of a system mainly depends on the performance of internal components present in the system. The internal components should be designed in such a way that they consume low power with high speed. Lot of components is in circuits including full-adder. This is mainly used in processors. A new Pass transistor full adder circuit is implemented in this paper. The main idea is to introduce the design of high performance and based pass transistor full adders which acquires less area and transistor count. The high performance of pass transistor low power full adder circuit is designed and the simulation has been carried out on Tanner EDA Tool. The result shows that the proposed full adder is an efficient full adder cell with least MOS transistor count that reduces the high power consumption and increases the speed. In this paper CMOS full adder circuits are designed to reduce the power and area and to increase the speed of operation in arithmetic application. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem*
Keywords: *Arithmetic, Full-adder, Power consumption, High-speed.*

I. Introduction

Addition, subtraction are basic arithmetic operations. It is mainly used in lot of VLSI systems such as microprocessors and application specific DSP architecture. In addition its main task is adding two numbers, it is used in many other useful operations such as, subtraction, multiplication, address calculation, etc. Building low power VLSI system has emerged as significant performance goal because of the fast technology in mobile communication and computation. The developments in battery technology have not taken place as fast as the advances in electronic devices. So the developers are attained with more; high speed, high throughput and at the same time, low power consumption as possible.

Energy-efficiency is the one which required most features in modern electronic systems designed for high-performance and/or portable applications. In this, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. This module is the core of many arithmetic operations like Addition and Subtraction etc. The PDP exhibited by the full-adder would affect the system's overall performance [1]. The PDP can be taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital design systems. In this paper, we have reported the design and comparison, performance of three full-adder cells implemented with an alternative internal logic structure, depends upon the multiplexing of the Boolean functions XOR/XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, severally, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption.

Several CMOS logic styles have been evolved for the developing the of cell libraries. They are willing to immortalize the ability to further reduce the cost-per function and improve the performance of integrated circuits. By lowering the threshold voltage in ultra deep submicron technology, low supply voltage appears to be the most eminent means to reduce power consumption. The resultant full-adders show more efficiency in power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

II. Logic Styles

Many papers have been published for the optimization of low-power full-adders, Different logic styles can be used to reduce the full-adder such as (regular CMOS [2], differential cascade voltage switch (DCVS) [3], complementary pass-transistor logic (CPL) [4], double pass-transistor logic (DPL) [5], swing restored CPL (SR-CPL) [6],

2.1 Existing Logic

2.1.1 Double-Pass Transistor Logic

Double-pass transistor logic eliminates some of the inverter stages required for complementary pass transistor logic by using both N and P channel transistors, with dual logical paths for each function. Though it has high speed due to low input capacitance, it has limited capacity to drive a load. The switching tree of a DPL gate consist of both NMOS and PMOS pass transistors, in contrast to the switching tree of a CPL gate, using only NMOS transistors there. Full swing operation is attained by simply adding PMOS transistors in parallel with the NMOS transistors. However, this addition will result in increasing input capacitance. The switching tree of a CPL gate consists of only NMOS transistors, which results in a lower input capacitance. The full-swing output-voltage restoration of a DPL-gate is done by the combination of an NMOS and a PMOS transistor, instead of the PMOS-latches and inverters which are used by means of Complementary Pass Transistor logic. Double pass-transistor logic (DPL) uses both PMOS and NMOS devices in the pass-transistor network to avoid non full swing problems, but it has high-area and high-power drawbacks [5].

2.1.2 Swing Restored Pass Transistor Logic

SRPL is very similar to CPL, because it uses the same NMOS pass-transistor network. The two cross-coupled inverters are used for recovering the output signal. An advantage of pass-transistor logic is its simplicity, but a disadvantage of SRPL is similar to a disadvantage of standard CMOS, namely the spikes on the power-supply that occur during switching. A SRPL-CEU has the same disadvantages as a CPL-cell [6].

2.1.3 Complementary Pass - Transistor Logic

Complementary pass-transistor logic or Differential pass transistor logic refers to a logic family which is designed for definite advantages. It is usual to use this logic family for multiplexers and latches. CPL uses series of transistors to select between possible inverted output values of the logic, by which output can be used to drive an inverter to generate the non-inverted output signal. Inverted and non-inverted inputs are required to drive the gates of the pass-transistors. The main concept behind CPL is the use of an NMOS pass-transistor network for logic organization. CPL consists of complementary inputs/outputs and NMOS pass-transistor logic network, CMOS output inverters. These inverters can be replaced by PMOS latches. The high level of the pass-transistor outputs (nodes Q and Q') is a threshold voltage which is lower than the supply voltage. This loss in output voltage pulls up by PMOS latches or CMOS output inverters. To maintain high speed switching and to make sure that the output signal has the same voltage swing as the input signal, it is important to use the PMOS latches or output inverters. This has the disadvantage that spikes occur on the power supply during switching.

The input voltage-levels are equivalent to those of standard CMOS, and this has the disadvantage that the voltage-swing is equal to Vdd. Complementary pass-transistor logic (CPL) uses a complementary output pass-transistor logic network to perform logic evaluation and CMOS inverters for driving of the outputs. This arrangement, however, can have leakage current through the inverter if the soft pull-up latch is not used [4]

2.2 Proposed Logic

2.2.1 Pass Transistor Logic

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input[5].By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Simulation of circuits may be required to ensure adequate performance.

III. Alternative Logic Structure For A Full Adder

The full-adder true-table is shown in Table 1, it can be seen that the output Sum is equal to the $A \oplus B$ value when Ci=0, and it is equal to $\overline{A \oplus B}$ when Ci=1. Here a 2*1 multiplexer can be used to obtain the respective value taking the Ci input as the selection signal. Following the same criteria, the output Co is equal to the A.B value when Ci=0, and it is equal to A+B value when Ci=1. Again, Ci can be used to select the respective value for the necessary condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the $A \oplus B$ and $\overline{A \oplus B}$ signals, another block to obtain the

A.B and A+B signals, and two multiplexers being driven by the C input to generate the *Sum* and *Co* outputs, as shown in Figure 1 [13].

The characteristics and benefits of this logic structure are as follows.

- There signals are not generated internally to control the selection of output multiplexers. The input signal, Ci exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.
- The capacitive load for the Ci input is reduced, as it is connected to some transistor gates and no longer to some drain or source terminals, as the diffusion capacitance is becoming a very large for sub-micrometer technology. Hence, the overall delay for larger modules where the Ci signal falls on the critical path can be reduced

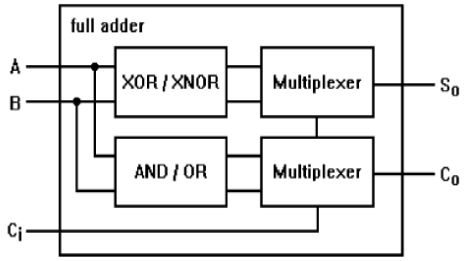

Figure 1: Alternative logic scheme for designing full-adder cells.

Table 1

TRUE-TABLE FOR A 1-BIT FULL-ADDER: A, B, AND Ci ARE INPUTS; Sum and Co ARE OUTPUTS

Ci	A	B	Sum	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

- The propagation delays for the *Sum* and *Co* outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; the feature advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipelining), and for having well balanced propagation delays at the outputs Sum and Co to reduce the chance of glitches in cascaded applications.
- Including buffers at the output of the full-adders can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

As per the results obtained in [13], three new full-adders have been designed using the logic styles DPL and SR-CPL, and a new pass-transistor logic structure is presented in Fig. 4.

DPL logic presents a full-adder design to build the XOR/XNOR gates, and a pass-transistor logic based multiplexer to obtain the *Sum* output.

In Figure 3, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration, and a pass-transistor based multiplexer to get the *Co* output. In Fig. 4, the pass transistor logicXOR/XNOR gates for the output of Sum is built using the SR -CPL and carry C0 is produced in the AND/OR gate

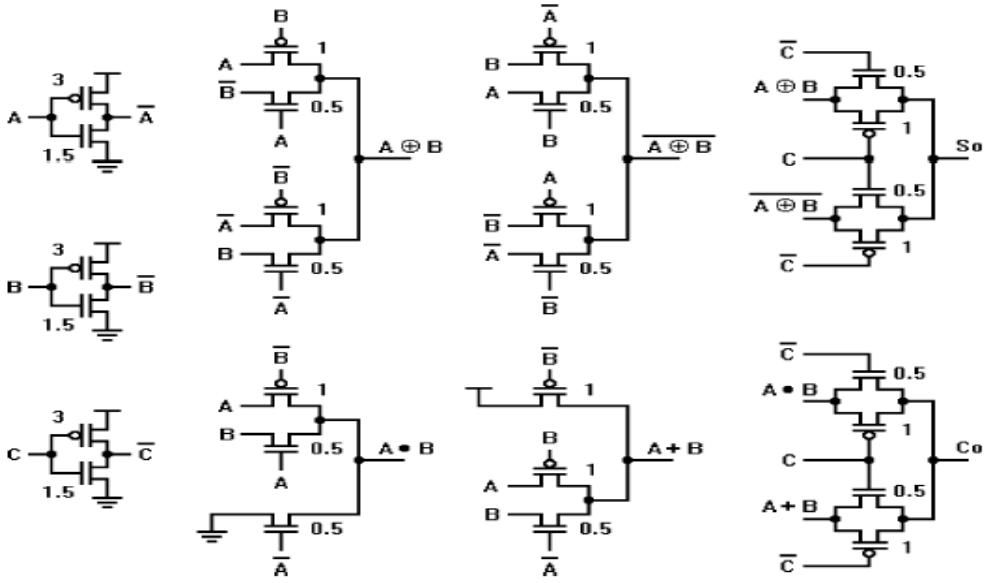

Figure 2: Full-adder designed with the Existing logic Structure and a DPL Logic Style.

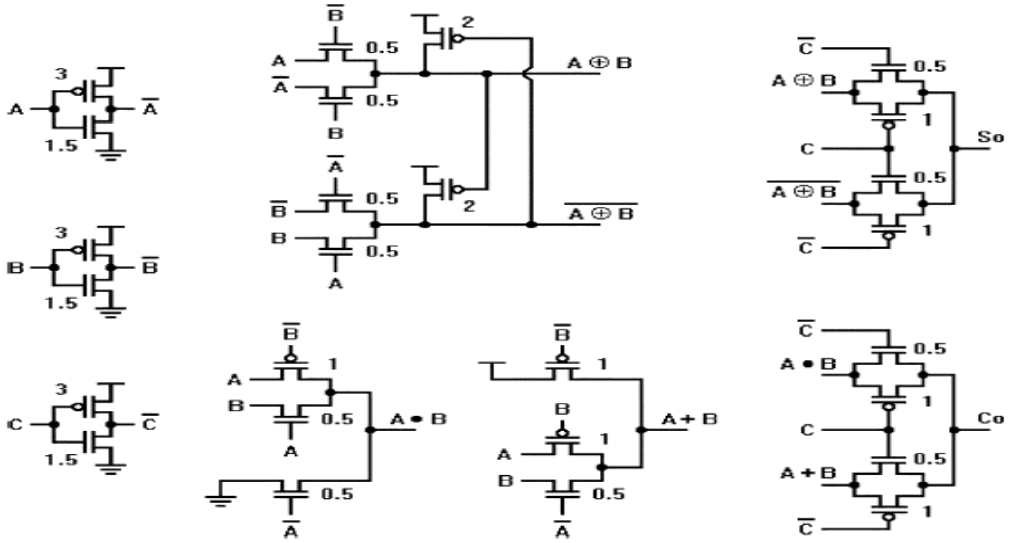

Figure 3: Full-Adder designed with the Existing logic Structure and a SR-CPL Logic Style.

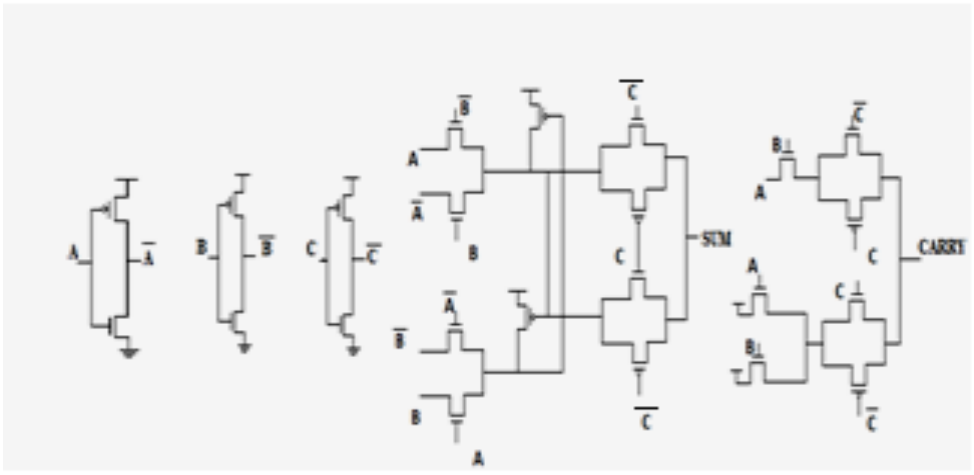

Figure 4: Full-adder designed with the Proposed Logic structure and a Pass Transistor Logic Style

Table 2: Parameter comparison of Existing and Proposed Logics

Parameters	DPL	SR-CPL	PASSTRANSISTOR, SR-CPL
NODES	**18**	**14**	**14**
N-MOS	**14**	**14**	**14**
P-MOS	**14**	**12**	**9**
MOSFETS	**28**	**26**	**23**
TIME(ns)	**2.76**	**2.24**	**2.23**
POWER (in watts)	**1.32e-003**	**1.18e-003**	**1.52e-004**

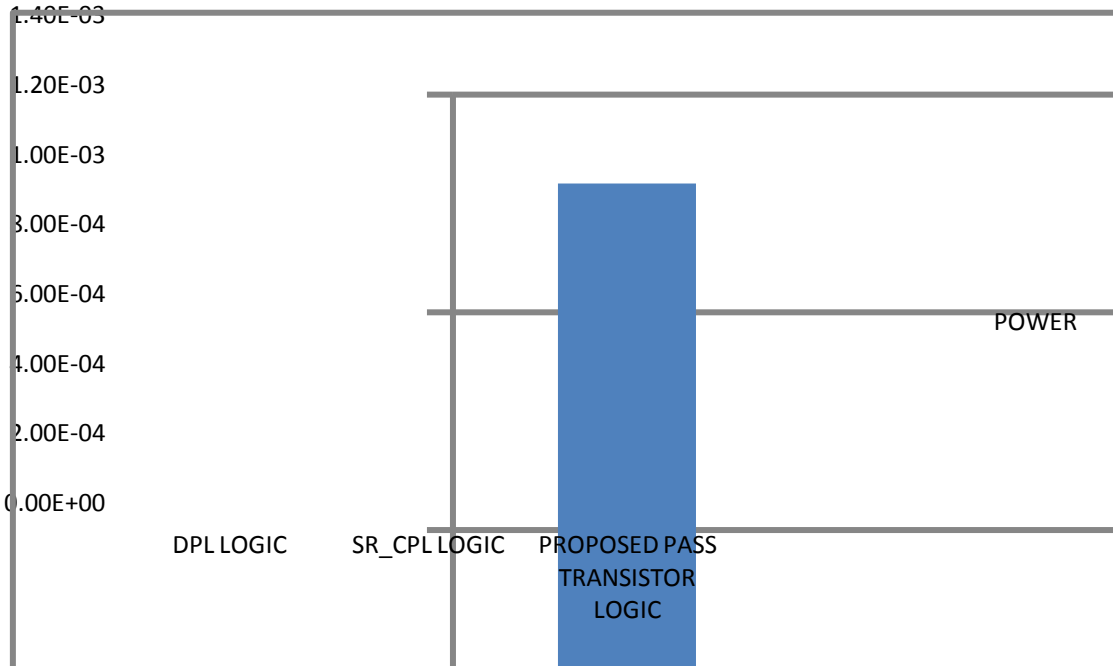

Figure 5:Power Comparison Chart for Existing and Proposed Logic

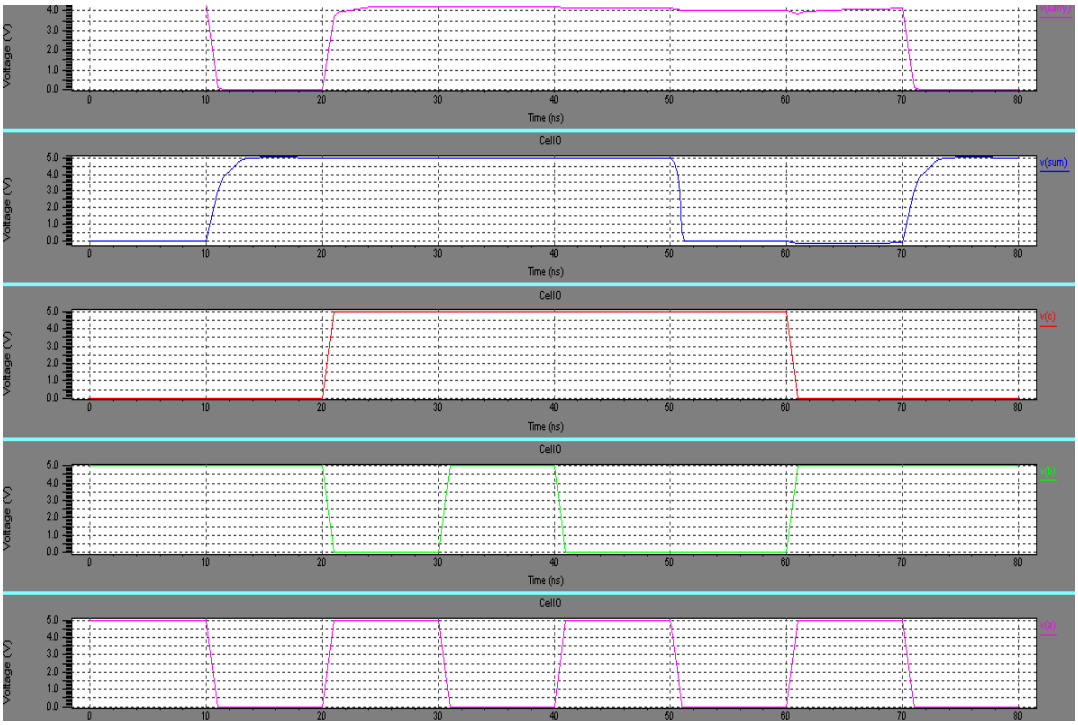

Figure 6: Waveform of Proposed Logic

IV. Simulation Environment

Figure 7 shows the test used for the analysis of the full-adders. This simulation is used for comparing the full-adders analyzed in [9], [14], with the addition of the inverters at the outputs. The size of the input buffers experience some degradation in the input signals. The size of the output buffers equals the load of four small inverters. This test is presented as a static CMOS gate for driving the full-adder cell under test. The benefit of using this simulation is less power consumption.

The short-circuit power consuming inverters are connected to the device under test (DUT) inputs. This power consumption varies as per the capacitive load that the DUT offers at the inputs. The energy required to charge and discharge the DUT internal nodes when the module has no direct power supply connections, comes through these inverters connected at the DUT inputs.

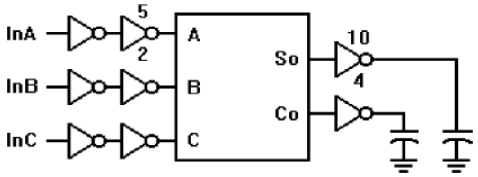

Figure 7: Test bed used for simulating the full-adders under comparison

- The short-circuit consumption of the DUT on its own, receives signals with finite slopes coming from the buffers are connected at the inputs, instead of ideal ones coming from voltage sources.
- The short-circuit and static power consumption of the inverters connected to the outputs of the DUT, which are because of the finite slopes and degraded voltage swing of the full-adder output signals.

The importance of including the effects and power consumption of the buffers connected at the inputs and outputs of the DUT comes from the fact that the DUT is always be used in combination with other devices to build a larger system. These static inverters are a good generalization for any operating scenario to be considered.

For the stimulus vectors, we used the test inputs patterns as recommended in 1-bit CMOS adder, as they exercise all the input combinations necessary to determine the propagation delay and power consumption

V. Conclusion

The main idea is to introduce the design of high performance and power efficient full adder design using multiplexer based pass transistor logic. In the present work, the full adder design is realized by different logics like DPL, SR-CPL. Further the design is implemented by using pass transistor logic combine with other logic. The number of transistors required for realizing mixed CMOS design of full adder is less than the number of transistors required in realizing the design of full adder using CMOS transistors independently. So, the required logic can be realized within an optimized area which performs faster when compared to the conventional static CMOS full adder design.

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