Microchannel heat sink fabrication techniques

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ABSTRACT Heat fluxes in IC chips and other electronics equipment have reached the current limits of air cooling technology. Some of the applications require heat fluxes well beyond the limit of 100 W/cm2, requiring advanced cooling solutions. This paper provides a roadmap of development in the thermal and fabrication aspects of microchannels as applied in microelectronics and other high heat flux cooling application. The formation of a monolithic microchannel heat sink and its performance is also discussed. **Keywords:** Bulk etching, deep reactive ion etching, microchannel, microfabrication, wafer bonding.

1.Introduction

Technology scaling continues in spite of tremendous technology development barriers, design challenges and prohibitive costs. Miniaturization of electronic devices and circuits has led to the emergence of self heating as a critical bottleneck to the performance and reliability of emerging microelectronic circuits and systems. Heat fluxes in integrated circuit (IC) chips and other electronics equipment have reached the current limits of air cooling technology. Some of the applications have heat fluxes well beyond the limit of 100 W/cm², requiring advanced cooling solutions.

Therefore, thermal management is one of the major reliability concerns. A workshop on "Thermal Challenges in Next Generation Electronics Systems (THERMES 2007)" [1] was held in January 7 to 10, 2007, in Santa Fe, USA chaired by Suresh Garimella (Purdue University) and Amy Fleischer (Villanova University). The panel discussions pointed to common themes as key concerns which must be addressed for next generation electronics systems. Some of them were as follows:

- novel low thermal resistance materials;
- power efficient design strategies;
- interface interactions;
- electro thermal integration issues;
- tradeoffs to be made between thermal, power and acoustic considerations;
- platform level design and tradeoffs;
- enhanced passive thermal management solutions;

Discussions were held on number of topics of which "Progress and needs in High Heat Flux Thermal Management" is considered here. The thermal management options for high heat flux applications were identified as follows



Second International Conference on Emerging Trends in Engineering (SICETE) 51 | Page Dr.J.J.Magdum College of Engineering, Jaysingpur

macro & microchannels schemes

The use of microchannel heat sinks in the thermal management of electronic and optical devices has been studied for about three decades. Due to their high area-to-volume ratio, and also due to area enhancement microchannel heat sinks are strong candidates for the effective dissipation of heat from devices, such as, integrated circuits.

Microchannel heat sinks are utilized generally with liquid coolants which provide higher heat transfer coefficients compared to gaseous coolants. The heat is removed from the surface either by single-phase liquid flow or phase change of the coolant with flow boiling (two-phase flow). The unique characteristics of microchannel heat sinks (small length scales, conductive substrate, abrupt contraction/expansion at the entrance/exit, and high pressure drop) give rise to conditions that are quite different from those of conventional channels.

Single-phase flows in microchannels have been studied extensively since the pioneering work of Tuckerman and Pease in 1981 [2]. They were able to remove up to 790 W/cm² heat flux using silicon etched microchannels; however the pressure drop was quite large 200kPa. Agostani et al. [3] reviewed the recent articles on single-phase microchannel heat sinks and stated that, on the average, heat fluxes of 300W/cm² can be handled with a heat sink unit thermal resistance of 0.18 K cm²/W. Improved results can be obtained by optimizing the channel geometry and flow conditions. Kandlikar reported that, by using enhanced microchannel structures it seems possible to dissipate heat fluxes as high as 1000 W/cm² from electronic circuits [4]. Wei et al. proposed liquid cooled multilayered microchannel heat sinks with overall thermal resistances as low as 0.09 K cm²/W [5]. Two major problems associated with microchannel heat sinks are the cost of fabrication and the integration of the cooling system with the electronic device.

1.1 Integration of the cooling system with electronic device:

The microchannel heat sinks are manufactured by different techniques such as, micromilling, micromolding, silicon etching or electroplating. Micromilling and micromolding processes require thick metal substrate; the heat sink is manufactured and then combined with the chip package through thermal interface materials. Figure 1 shows a typical packaging assembly of a desktop processor with the heat sink attached to an integrated heat spreader (IHS) mounted on the back side of the chip [6].





A layer of thermal interface material (TIM) is used between the die and the IHS and between the IHS and the heat sink to reduce contact resistance. Figure 1 also illustrates the thermal resistance network for this heat sink system, including five thermal resistances in series.

A considerable portion of the thermal resistance (more than 35%) in the cooling system is due to the housing and the thermal interface materials between the electronic circuit and the coolant (Fig.2) [6]. The thermal interface resistance between a heat sink and the chip is a major contributor to the total resistance in the heat flow path from the junction to ambient air. This is a topic of major research effort in the chip cooling industry. With the current Thermal Interface Materials (TIM), this resistance is approaching as low as 0.02 cm² °C/W in commercial units.



Fig. 2. Thermal resistance breakdown for microchannel design¹¹.

As seen from the figure 2, thermal resistance of TIM (35%) and baseplate (21%) form more than half of the thermal resistance of the microchannel heat sink. Microchannels can be deployed in two alternative configurations in cooling applications (Fig. 3a, 3b). Kumari et al. [7] showed that the heat sink thermal resistance is higher for the integrated microchannels on die compared to microchannel mounted on the IHS or on the lid; however, the total resistance of the heat sink assembly is minimized with the microchannels-on-die configuration due to the absence of the TIM and the IHS resistances,



Fig.3. Schematic diagrams of microchannels formed (a) in a cold plate mounted on the IHS, and (b) directly into the die.

2 Microchannel Fabrication

The evolution of microchannel-based heat exchangers has largely been paced by advances in microfabrication technology. In this section, an overview of existing microfabrication techniques with an emphasis on those

Second International Conference on Emerging Trends in Engineering (SICETE) Dr.J.J.Magdum College of Engineering, Jaysingpur particularly suited for building microchannel devices is given. A group of microchannel fabrication technologies is depicted taxonomically [8] in Figure 4.

Miniaturized traditional techniques are rooted in conventional machine shop and manufacturing practices but adapted to achieve microscale features. These miniature techniques often use conventional machine tools especially adapted to operate in the micro regime. The adaptations range from shrinking the machine tool itself, such as miniature milling machines, to the introduction of lithographic patterning. Sawing has been taken into the micro realm, especially in the form of wafer dicing. Saw cuts on the order of 25 ¹m width with a placement accuracy of 4 ¹m at 3 sigma can be obtained with commercially available equipment [9]. Micro-electro discharge machining [10–12] has been demonstrated using very fine wires as electrodes. Commercial electroforming, molding, and stereo lithographic fabrication have been brought into the micro regime through the incorporation of lithographic and laser-based patterning.



Fig. 4 Taxonomic chart of microfabrication technologies [8].

The "modern" technologies can be distinguished as either serial or batch type. Silicon-based micromachining techniques can be broadly divided into two groups. In bulk micromachining, the final part is made by selectively removing portions of the starting substrate. Because the final part is made from the original single-crystal silicon, it has tremendous strength and is virtually stress-free. In contrast, surface micromachining creates the final part on or above the starting substrate through a series of deposition, patterning, and etching steps. In many cases, the substrate is completely irrelevant to the fabrication process, and silicon becomes the substrate of choice for reasons of cost and process compatibility.

The major issue in bulk micromachining is the etch process. Bulk etching can be carried out in either a wet chemical or dry plasma format, and both techniques have isotropic and anisotropic variants. Anisotropic wet chemical etching (WCE) of silicon has been the workhorse technique since the original work of Tuckerman and Pease [2]. A number of etchants, including potassium hydroxide and ethylene diamine pyrocatechol, will etch the f111g planes of silicon at such a slowrate. Anisotropic WCE etch rates are typically in the range of 1µm/min; as such, etch times of many hours are common. Wafers can, however, be etched in batches to improve throughput. A recent advance in etch technology has been the emergence of dry etch techniques [13–16]. Of particular

Second International Conference on Emerging Trends in Engineering (SICETE) 54 | Page Dr.J.J.Magdum College of Engineering, Jaysingpur

interest are the deep reactive ion etch (DRIE) processes that can produce vertical etch profiles in silicon. The most commercially prominent technique is the so-called "Bosch etch" [17], which uses alternating etch and polymer passivation chemistries. The reaction chamber is typically fitted with an inductively coupled energy source to create plasmas that are one to two orders of magnitude denser that those obtained by conventional parallel-plate reactive ion etching. The substrate is either mechanically or electro statically held to a cooled platen with a separate bias to control incident ion energy. Typical etch rates are in the range $2-8 \mu m/min$; however, etch rates greater than $20 \mu m/min$ have been reported in a specially designed tool.

Bulk micromachining and surface micromachining are complementary techniques that can be combined to build multifunctional systems. Zohar and coworkers [18, 19] have built microchannel devices with integrated heaters and temperature sensor arrays. It is anticipated that true systems-on-chip that combine microcooling with sensing, computation, active fluidic components, on-board power sources, and communication to the outside world will evolve in the future.

A class of very high aspect ratio fabrication processes based on the lost wax molding technique has come to be known by the term LIGA, a German acronym for lithographie, galvanoformung, abformung (meaning lithography, electroplating, and molding). LIGA uses highly collimated X-rays projected through a special X-ray mask to provide near diffraction-free exposure of a thick photoresist. The developed features in the photoresist can then be filled with a variety of materials and planarized. The technique can create structures with aspect ratios in excess of 100:1 and can hold submicron tolerances over many hundreds of microns of vertical height. Final parts can be obtained in three distinct ways. First, the patterned resist can be separated from the substrate and used as a precision machined polymer. Second, the molded deposit, which is typically an electroformed metal such as nickel or copper, can be separated from the substrate. Lastly, the substrate and deposited metal can be used in combination as a high precision molding master. A wide variety of structures and devices have been demonstrated using LIGA, including fluid channels and fluidic components, geared micromotors, and high precision connectors. However, LIGA has failed to become widely accepted because of the difficulty in making suitable X-ray masks and the cost and limited availability of the exposure equipment.

There is great interest in alternative techniques that can provide high aspect patterning using conventional ultraviolet sources. These so-called ultraviolet-LIGA (or UV-LIGA) processes have become increasingly viable with the development of multiple coating techniques, thick layer coating equipment, and chemically amplified resists.

2.1 Wafer Bonding Techniques:

None of the technologies described above can individually produce a complete microsystem. Hybridization is the process of combining all the necessary disparate substrates, structures, components, and subassemblies into a final product. An extremely versatile variant of hybridization is wafer bonding, where two flat substrates of nearly arbitrary composition can be permanently attached.Direct wafer bonding is a collection of processes of which the exact details vary with material but the technique can generally be tailored to obtain a wide range of adhesive bond strengths. Pl^o⁻¹ and Kr^oauter have extensively reviewed wafer bonding and its application to microsystems construction [20]. Three bonding techniques of particular interest are fusion bonding, anodic bonding, and adhesive bonding.

In fusion bonding, two wafers of which the surfaces are silicon or silicon compounds, such as oxide and nitride, can be covalently bonded through a combination of chemical surface treatments, pressure, and annealing at elevated temperature. When properly performed, the bond strength is at least as great as the bulk wafer strength. Wafer stacks of greater than two wafers can be bonded in either a serial or parallel fashion. Prior to fusion bonding, the wafers can be extensively machined. A variety of fusion bonded microsystems with complex internal cavities and moving parts have been realized, including accelerometers, microfluidic valves, and micro turbine engines. In anodic bonding, silicon and ionic glass surfaces are joined through a combination of pressure, temperature, and electric field. While both fusion and anodic bonding can produce interfaces with great strength, they are quite material specific. For generic hetero-bonding, adhesive techniques are the most general. Figure 5 shows how microchannel devices can be formed by wafer bonding.



Fig. 5 The wafer bonding process.

3. Monolithic microchannel heat sink

Koyuncuoglu et al. [21] implemented a monolithic microchannel heat sink design, channels of two different heights, 20 and 50 μ m, have been considered. In the fabrication, only metal electroplating and polymer chemical deposition processes were applied on top of the circuit avoiding any bulk silicon etching process. The microchannel dimensions enabled single-phase water-cooling rather than air cooling. The device can be fabricated within the CMOS fabrication flow (Figure 6). As a first stage, the microchannel heat sinks were fabricated on top of thin film resistor heaters instead of actual integrated circuits. An extension would be the fabrication of them on actual microchips.

An experimental investigation of the microchannel by Koyuncuoglu et al. [21] indicated that the fabricated microchannel heat sinks are capable of cooling high heat flux electronic devices such as CPUs. During the tests, heat flux values up to 50 W/cm² were successfully removed from the entire chip surface. A single channel heater, simulating a hot spot on a CPU was operated successfully up to 127 W/cm² heat flux.



Fig. 6. Microchannel heat sink on a CMOS circuit and cross-sectional view of one of the microchannels.

In fabrication of heat sinks on the top of microchips some major issues need to be addressed: the stresses induced in the chip due to bonding/gluing, circulation of pressurized coolant during operation, leakage concerns, channel blockages due to particulates, etc.

4. Conclusion

As seen in the introduction, lot of research work on microchannel heat sinks is done with objectives such as:

- a) Development of low cost and efficient microchannels.
- b) Identifying various approaches to generate vortices in the flow passages which enhance the heat transfer performance.
- c) Means to obtain homogeneous temperature profiles in the microchannels, which will increase the life of the microchannel.
- d) Understand the effects of surface roughness on the performance of microchannel heat sinks.
- e) Development of generalized correlations, useful for the design and optimization of microchannel heat sinks.

Efficient fabrication techniques are needed to achieve the objectives of microchannel research. Monolithic microchannel heat sink can be one of them.

References

[1] S.V.Garimella, A.S.Fleischer, Murthy, A. Keshavarzi, R. Prasher, C.Patel, S.Bhavnani, R. Venkatsubramanian, R. Mahajan, Y. Joshi, B. Sammakia, B. Myers, L. Chorosinski, M Baelmans, P. Sathyamurthy and P. Raad, "Thermal challenges in next generation electronic systems". IEEE Trans. Comp. And Packaging Tech. Vol.31 No. 4 (Dec.2008)

[2] D.B. Tuckerman, R.F.W. Pease, "High-performance heat sinking for VLSI", IEEE Electron Device Letters 2 (1981) 126-129.

[3] B. Agostini, M. Fabbri, J.E. Park, L.Wojtan, J.R. Thome, B. Michel, "State of the art of high heat flux cooling technologies", Heat TransferEngineering28(2007) 258-281.

[4] S.G. Kandlikar, "High flux heat removal with microchannels a roadmap of challenges and opportunities", Heat Transfer Engineering 26 (2005) 5-14.

[5] X. Wei, Y. Joshi, M.K. Patterson,"Experimental and numerical study of a stacked microchannel heat sink for liquid cooling of microelectronic devices", Journal of Heat Transfer 129 (2007) 1432.

[6] S. V. Garimella & Tannaz Harirchian, "Set 1: Thermal Packaging Techniques" (A 6-Volume Set) Volume 1: Microchannel Heat Sinks for Electronics Cooling.

[7] N. Kumari, S. Krishnan, and S.V. Garimella, "Analysis and performance comparison of competing desktop cooling technologies", Proceedings of the ASME InterPack Conference, IPACK 2007, Vol. 2 (2007), pp. 1018–1027.

[8] S.G.Kandlikar, W.J. Grande, "Evolution of microchannel flow passages- thermohydraulic performance and fabrication technology", Heat Transfer Engg. 24 (1); 3-17, 2003

[9] Disco Corp's website www.disco.co.jp

[10] Masaki, T., Kawata, K., and Masuzawa, T., Micro Electro-Discharge Machining and its Applications, *IEEE Micro Electro Mechanical Systems Workshop*, Napa Valley, California, pp. 21–26, 1990.

[11] Kuo, C.-L., Masuzawa, T., and Fujino, M., A Micropipe Fabrication Process, *IEEE Micro Electro Mechanical SystemsWorkshop*, Nara, Japan, pp. 80–85, 1991.

[12] Furutani, K., Enami, T., and Mohri, N., Dot-Matrix Electrical Discharge Machining for Shaping Fine Structure, *Proc. IEEE 10th Annual International Workshop on Micro Electro Mechanical Systems*, Nagoya, Japan, pp. 180–185, January 26–30, 1997.

[13] Klaassen, E. H., et al., Silicon Fusion Bonding and Deep Reactive Ion Etching: A New Technology for Microstructures, *Digest of Technical Papers from Transducers '95/Eurosensors IX*, Stockholm, Sweden, vol. 1, pp. 556–559, June 25–29, 1995.

[14] Fleming, J. G., and Barron, C. C., Characterization and Application of Deep Si Trench Etching, SPIE Conference on Micromachining and Microfabrication Process Technology II, SPIE vol. 2879, pp. 73–79, 1996.

[15] Pandhumsoporn, T., et al., High Etch Rate, Anisotropic Deep Silicon Plasma Etching for the Fabrication of Microsensors, *SPIE Conference on Micromachining and Microfabrication Process Technology II*, SPIE vol. 2879, pp. 94–102, 1996.

[16] Bhardwaj, J., Ashraf, H., and McGuarrie, A., Dry Silicon Etching for MEMS, *Proc. 1997 Meeting of the Electrochemical Society, Microstructures and Microfabricated Systems III Symposium*, Montr´eal, PQ, vol. 97–5, pp. 118–130, May 4–9, 1997.

[17] L'armer, F., and Schilp, P., Method of Anisotropically Etching Silicon, German Patent No. DE 4,241,045, 1994.

[18] Jiang, L., et al., Fabrication and Characterization of a Microsystem for a Micro-Scale Heat Transfer Study, J. Micromech. Microeng., vol. 9, pp. 422–428, 1999.

[19] Jiang, L., Wong, M., and Zohar, Y., Phase Change in Microchannel Heat Sinks with Integrated Temperature Sensors, *J MEMS*, vol. 8, no. 4, pp. 358–365, 1999.

[20] Pl"o⁻¹, A., and Kr"auter, G., Wafer Direct Bonding: Tailoring Adhesion Between Brittle Materials, *Materials Science and Engineering*, R25, pp. 1–88, 1999.

[21] Aziz Koyuncuoglu, Rahim Jafari, Tuba Okutucu-Özyurt, Haluk Külah, "Heat transfer and pressure drop experiments on CMOS compatible microchannel heat sinks for monolithic chip cooling applications", International Journal of Thermal Sciences xxx (2012) 1 9 Article in Press.

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