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Secondary Distribution for Grid Interconnected Nine-level Inverter using PV system

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Abstract : *This paper proposes a Secondary distribution (single phase) nine -level inverter for grid-connected photovoltaic systems, with a novel pulse width modulated (PWM) control scheme. Four reference signals that are identical to each other with an offset that is equivalent to the amplitude of the triangular carrier signal were used to generate the PWM signals. The inverter is capable of producing nine levels of output-voltage levels* (V_{dc} , $3V_{dc}/4$, $V_{dc}/2$, $Vdc/4$, 0, $-V_{dc}$, $-3V_{dc}/4$, $-V_{dc}/2$, $Vdc/4$) *from the dc supply voltage. A digital proportional–integral current-control algorithm was implemented in a TMS320F2812 DSP to keep the current injected into the grid sinusoidal. The proposed system was verified through simulation and implemented in a prototype.*

Keywords - *Grid connected, modulation index, multilevel inverter, photovoltaic (PV) system, pulse width modulated (PWM), total harmonic distortion (THD).*

I. INTRODUCTION

The ever-increasing energy consumption, fossil fuels' soaring costs and exhaustible nature, and worsening global environment have created a booming interest in renewable energy generation systems, one of which is photovoltaic. Such a system generates electricity by converting the Sun's energy directly into electricity. Photovoltaic-generated energy can be delivered to power system networks through grid-connected inverters. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW. Types of single-phase grid-connected inverters have been investigated. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter's switching operation. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact. Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped, flying capacitor or multi cell, cascaded H-bridge, and modified H-bridge multilevel. This paper recounts the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique. The topology was applied to a grid-connected photovoltaic system with considerations for a maximum-power-point tracker (MPPT) and a current-control algorithm.

II. PROPOSED MULTILEVEL INVERTER

The proposed single-phase nine-level inverter was developed from the seven-level inverter in. It comprises a single-phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by C_1, C_2, C_3, and C_4 as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitors for inverters of the same number of levels. Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to the power network, so the utility grid, rather than a load, was used. The dc–dc boost converter was required. The because the PV arrays had a voltage that was lower than the grid voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the grid. A filtering inductance Lf was used to filter the current injected into the grid. Proper switching of the inverter can produce seven output-voltage levels (V_{dc}, $3V_{dc}/4$, $V_{dc}/2$, $Vdc/4$, 0, $-V_{dc}$, $-3V_{dc}/4$, $-V_{dc}/2$, $Vdc/4$) from the dc supply voltage.

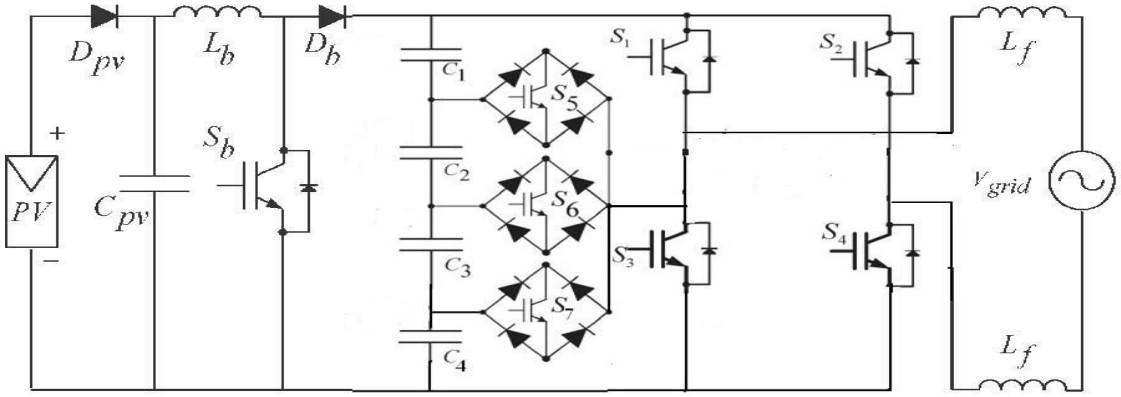

Fig. 1. Proposed single phase nine-level grid-connected inverter for photovoltaic systems.

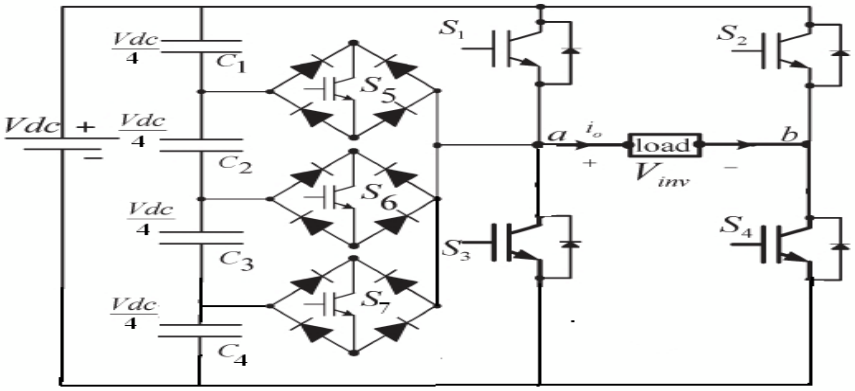

Fig. 2. Nine-level inverter for switching operation.

The single-phase nine-level inverter was developed from the seven-level inverter as shown in Fig.1. It comprises a single-phase conventional H-bridge inverter, three bidirectional switches, and a capacitor voltage divider formed by C1, C2,C3 and C4, , as shown in Fig. 1. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels. Photovoltaic (PV) arrays were connected to the inverter via a dc–dc boost converter. The power generated by the inverter is to be delivered to induction Motor. The dc–dc boost converter was required because the PV arrays had a voltage that was lower than the single-phase voltage. High dc bus voltages are necessary to ensure that power flows from the PV arrays to the single-phase induction motor. The LC-filter is modeled to obtain pure sine-wave and is given to drive a single-phase induction motor.. Proper switching of the inverter can produce nine- output-voltage-levels (Vdc, 3 V d c /4, V d c /2, V d c /4, 0 ,-Vdc/4, -Vdc/2, -3Vdc/4, - Vdc) from the dc supply voltage. The proposed inverter's operation can be divided into nine switching states. The required nine levels of output voltage were generated as follows.

Maximum positive output (Vdc): S1 is ON; connecting the load positive terminal to Vdc, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc.

Three-fourth positive output (3Vdc/4): The bidirectional switch S5 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is 3Vdc/4.

Half of the positive output (Vdc/2): The bidirectional switch S6 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc/2.

One-fourth of the positive output (Vdc/4): The bidirectional switch S7 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc/4.

Zero output: This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1 andS2 are ON, and all other controlled switches are OFF; terminal ab is a short circuit, and the voltage applied to the load terminals is zero.

One-fourth negative output (−Vdc/4): The bidirectional switch S5 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to Vdc. All other controlled switches are OFF; the voltage applied to the load terminals is −Vdc/4.

Half of the negative output (−Vdc/2): The bidirectional switch S6 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is −Vdc/2

Three-fourth negative output (−3Vdc/4): The bidirectional switch S7 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is −3Vdc/4.

Maximum negative output (−Vdc): S2 is ON; connecting the load negative terminal to Vdc, and S3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is −Vdc.

Table I shows the switching combinations that generated the nine output-voltage levels (Vdc, 3Vdc/4, Vdc/2, Vdc/4, 0,-Vdc/4, -Vdc/2, -3Vdc/4, - Vdc)

TABLE 1

Out Put Voltage According To The Switches On Off

Vo	S1	S2	S3	S4	S5	S6	S7
Vdc	On	Off	Off	On	Off	Off	Off
3Vdc/4	Off	Off	Off	On	On	Off	Off
Vdc/2	Off	Off	Off	On	Off	On	Off
Vdc/4	Off	Off	Off	On	Off	Off	On
0	Off	Off	On	On	Off	Off	Off
-Vdc/4	Off	On	Off	Off	On	Off	Off
-Vdc/2	Off	On	Off	Off	Off	On	Off
-3Vdc/4	Off	On	Off	Off	Off	Off	On
-Vdc	Off	On	On	Off	Off	Off	Off

III. PWM TECHNIQUE

A novel PWM modulation technique was introduced to generate the PWM switching signals. Four reference signals (V_{ref1}, V_{ref2}, V_{ref3}, and V_{ref4}) were compared with a carrier signal ($V_{carrier}$). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If V_{ref1} had exceeded the peak amplitude of $V_{carrier}$, V_{ref2} was compared with $V_{carrier}$ until it had exceeded the peak amplitude of $V_{carrier}$. Then, onward, V_{ref3} would take charge and would be compared with $V_{carrier}$ until it had exceeded the peak amplitude of $V_{carrier}$. Then V_{ref4} would take the charge to reached zero. Once V_{ref4} had reached zero, V_{ref3} would be compared until it reached zero. Then, onward, V_{ref2} would take charge to reached zero; V_{ref1} would be compared with $V_{carrier}$. The resulting switching pattern. Switches S_1, S_3, S_5, S_6, and S_7 would be switching at the rate of the carrier signal frequency, whereas S_2 and S_4 would operate at a frequency that was equivalent to the fundamental frequency.Fig.2 shown signal generation.

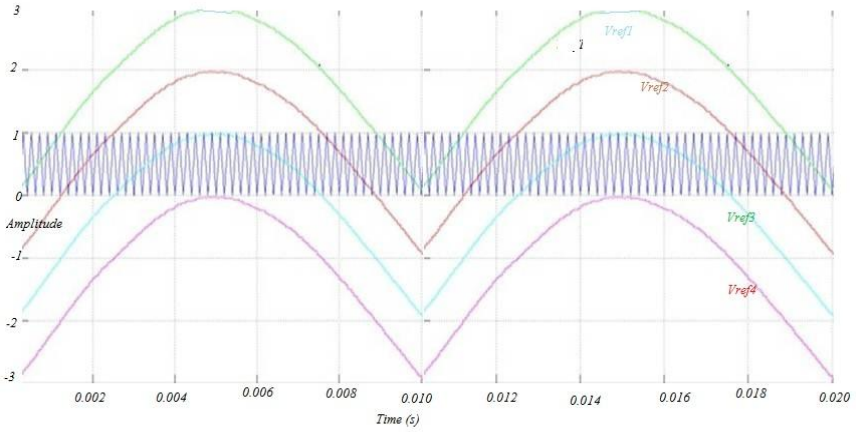

Fig.2. PWM Switching signal generator.

IV. CLOSED LOOP CONTROL SYSTEM

The control system comprises a MPPT algorithm, a dc-bus voltage controller, reference-current generation and a current controller. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also under the presence of grid voltage harmonics. The proposed inverter utilizes the perturb-and-observe (P&O) algorithm for its wide usage in MPPT owing to its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the previous perturbation cycle. If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm will oscillate around it. The P&O algorithm was implemented in the dc–dc boost converter. The output of the MPPT is the duty-cycle function. Fig.3. shown closed loop system. As the dc-link voltage *V*dc was controlled in the dc–ac seven level PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels. A PID controller was implemented to keep the output voltage of the dc–dc boost converter (*V*dc) constant by comparing *V*dc and *V*dc ref and feeding the error into the PID controller, which subsequently tries to reduce the error. In this way, the *V*dc can be maintained at a constant value and at more than √2 of *V*grid to inject power into the grid. To deliver energy to the grid, the frequency and phase of the PV inverter must equal those of the grid; therefore, a grid synchronization method is needed. The sine lookup table that generates reference current must be brought into phase with the grid voltage (*V*grid). For this, the grid period and phase must be detected. The proposed inverter provides an analog zero-crossing detection circuit on one of its input ports where the grid voltage is to be connected. The zero-crossing circuit then produces an in-phase square-wave output that is fed into the digital I/O port on eZdsp board TMS320F2812. A PI algorithm was used as the feedback current controller for the application. The current injected into the grid, also known as grid current *I*grid, was sensed and fed back to a comparator that compared it with the reference current *I*gridref . *I*gridref is the result of the MPPT algorithm. The error from the comparison process of *I*grid and *I*gridref was fed into the PI controller. The output of the PI controller, also known as *V*ref, goes through an anti windup process before being compared with the triangular wave to produce the switching signals for *S*1–*S*7 Eventually, *V*ref becomes *V*ref1; *V*ref2; *V*ref3 and *V*ref4 can be derived from *V*ref1 by shifting the offset value, which was equivalent to the amplitude of the triangular wave.

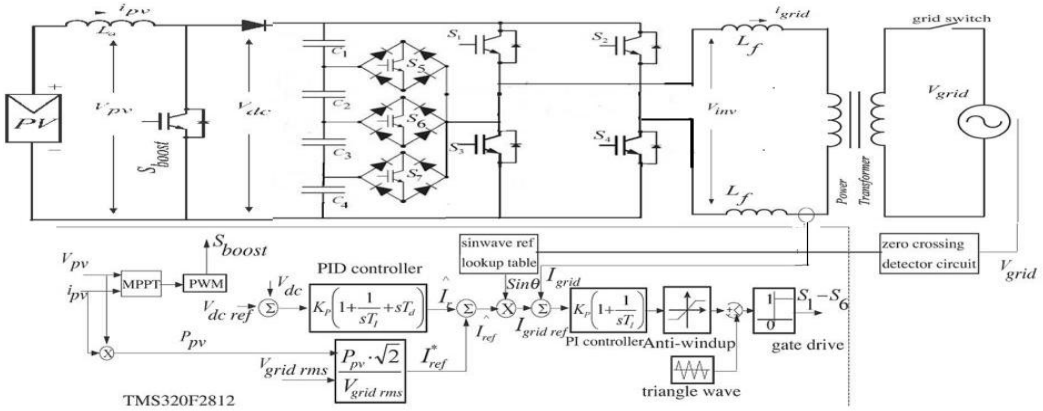

Fig.3. Nine-level inverter with closed-loop algorithm.

V. SIMULATION RESULTS

MATLAB SIMULINK simulated the proposed configuration before it was physically implemented in a prototype. The PWM switching patterns were generated by comparing three reference signals (*V*ref1, *V*ref2, *V*ref3, and *V*ref4) against a triangular carrier signal. Subsequently, the comparing process produced PWM switching signals for switches *S*1–*S*7, as. One leg of the inverter operated at a high switching rate that was equivalent to the frequency of the carrier signal, while the other leg operated at the rate of the fundamental frequency (i.e., 50 Hz). Switches *S*5 and *S*6 also operated at the rate of the carrier signal. Inverter output voltage (*V*inv). Fig.10. shows Grid voltage (*V*grid) and grid current (*I*grid) of the carrier signal. Fig.9. shows the simulation result of inverter output voltage *V*inv. The dc-bus voltage was set at 300 V (>√2*V*grid; in this case, *V*grid was 120 V). The dc-bus voltage must always be higher than √2 of *V*grid to inject current into the grid, or current will be injected from the grid into the inverter. Therefore, operation is recommended to be between *Ma* = 0.66 and *Ma* = 1.0. Fig.5-8. Shows PWM signals for *S*1 to *S*7 switches. *V*inv comprises seven voltage levels, namely, *V*dc, 3*V*dc/4, *V*dc/2, *V*dc/4, 0; −*V*dc, −3*V*dc/4, −*V*dc/2, and *V*dc/4.The current flowing into the grid was filtered to resemble a pure sine wave in phase with the grid voltage see Fig. 10). As *I*grid is almost a pure sine wave at unity power factor, the total harmonic distortion (THD) can be reduced compared with the THD.

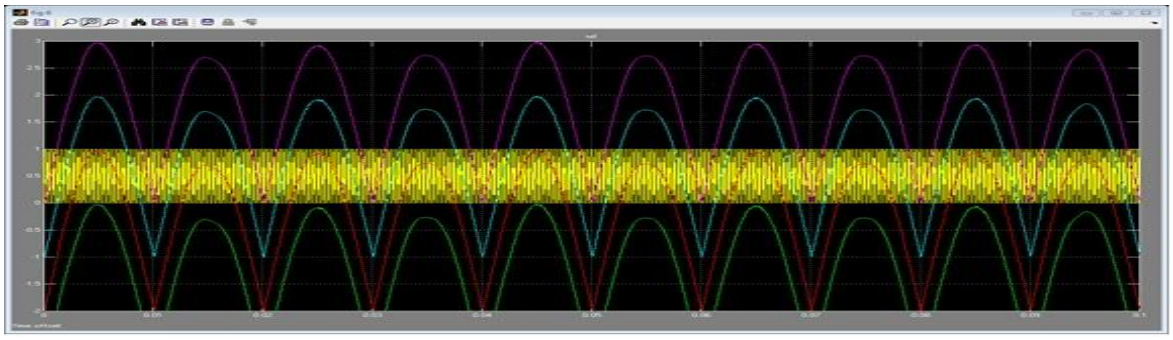

Fig.4. Simulink output of PWM switching signal generation.

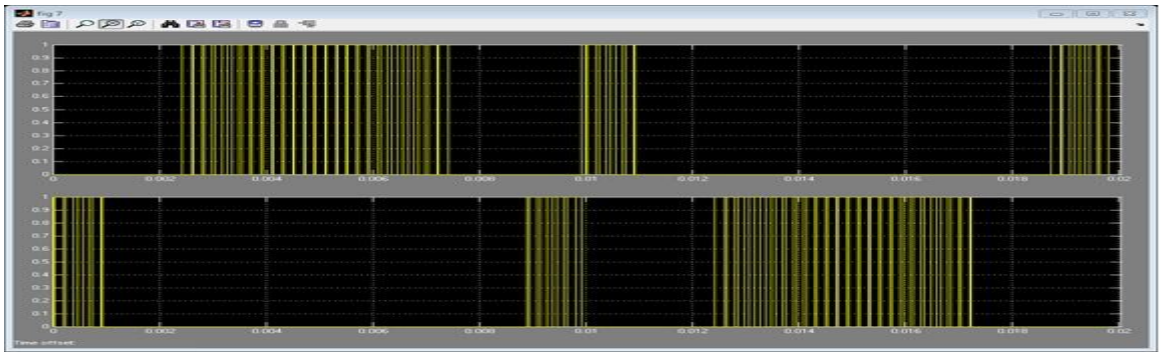

Fig.5. PWM signals for *S*1 and *S*2.

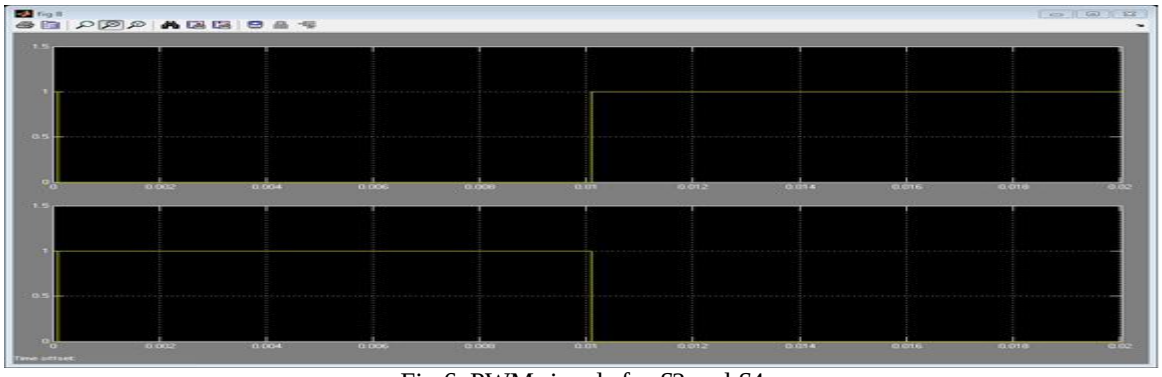

Fig.6. PWM signals for *S*2 and *S*4.

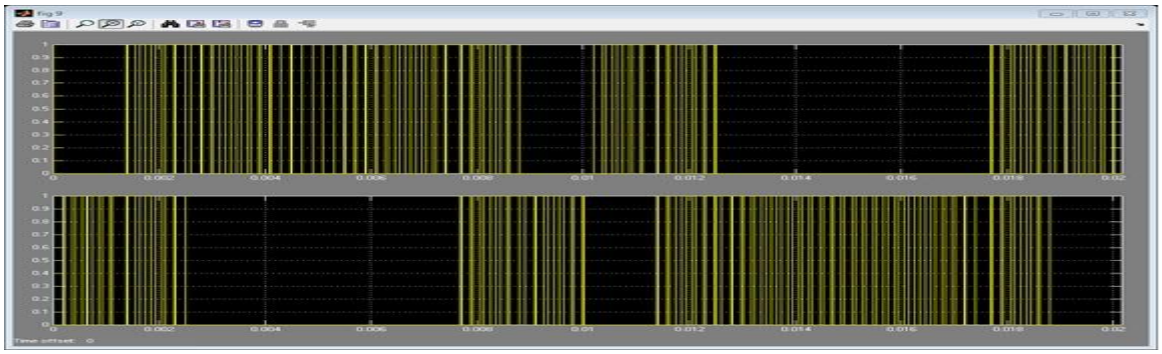

Fig.7. PWM signals for *S*5 and *S*6.

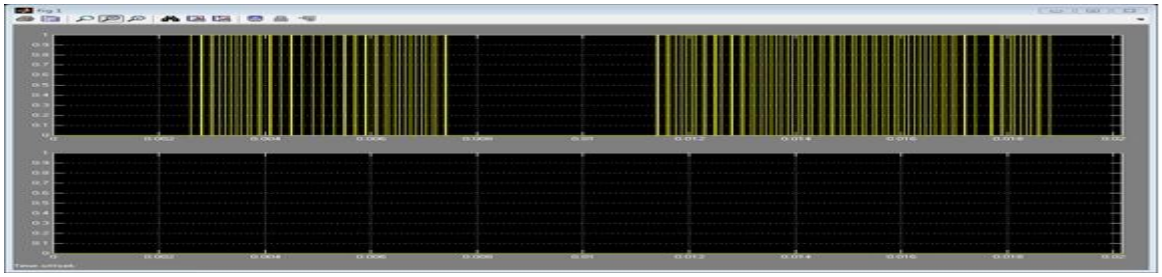

Fig.8. PWM signal for *S*7.

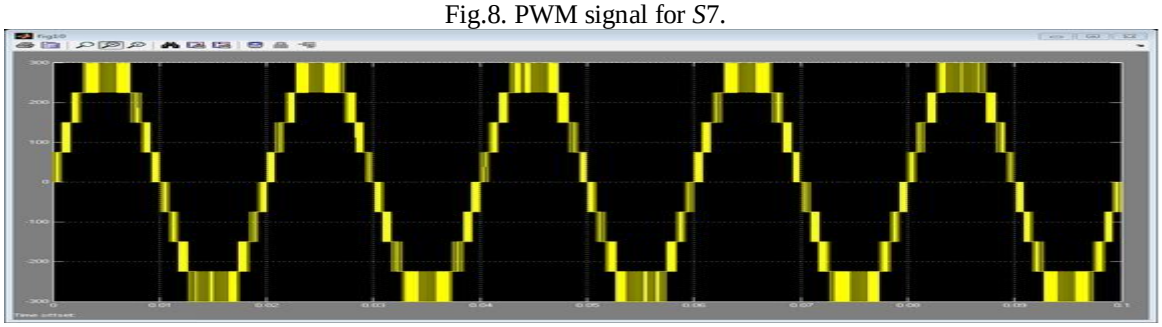

Fig.9. Inverter output voltage.

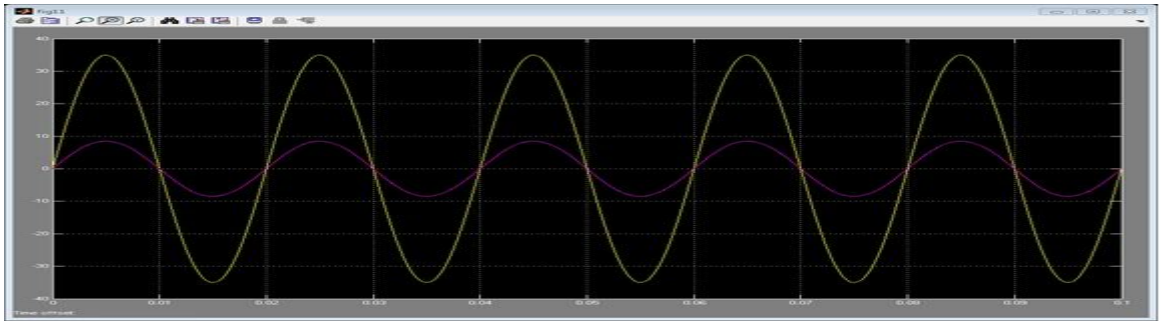

Fig.10. Grid voltage (V_{grid}) and grid current (I_{grid}).

TABLE 2
COMPARISON OF THD IN DIFFERENT LEVELS

Sl. No.	Levels	Total Harmonic Distortion (THD) in %	Ripple current (A)	Frequency
1.	3-level	8.0	1.92	50.00
2.	5-level	5.4	1.94	50.03
3.	7-level	3.9	2.48	50.00
4.	9-level	2.8	2.76	50.03

VI. CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes four reference signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel inverter was analyzed in detail. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. Table 2 shows the less THD in the nine-level inverter compared with that in the seven- level, five-level and three level inverters is an attractive solution for grid-connected PV inverters.

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