IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676, p-ISSN: 2320-3331, Volume 18, Issue 3 Ser. I (May. – June. 2023), PP 24-30
www.iosrjournals.org

Kink Effect Reduction in Partially Depleted SOI MOSFET

Towhid Adnan Chowdhury
Assistant Professor
Department of Electrical & Electronic Engineering,
Ahsanullah University of Science & Technology,
Dhaka,Bangladesh.

Abstract:*Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been of crucial importance for the progress of nanoelectronics technology. Silicon on insulator (SOI), a new technology of MOSFET transistors, helps in miniaturization and decrease of short channel effects. A two dimension device simulation is performed to investigate the kink effect of partially depleted SOI MOSFET using Silvaco TCAD tools.This paper demonstrates a method for reducing the kink effect present in the current-voltage output characteristics of partially depleted SOI MOSFET. In this method, the thickness of gate oxide for the device is reduced. Results obtained through simulations indicate that the proposed method, while still maintaining major advantages obtained by conventional SOI structure, can eliminate the kink effect.*

Key Word*: MOSFET, Silicon on Insulator, PD SOI, Silvaco TCAD, Kink Effect.*

Date of Submission: 06-05-2023 Date of Acceptance: 16-05-2023

I. Introduction

For achieving the objective that Moore's Law diagram reveals, many scientists and engineers engaged to find various methods for linear downscaling silicon devices and to design new technologies respectively. Enormous research have taken place in semiconductor technology ever since, for the development of more complicated circuits on a single semiconductor substrate. To accomplish this purpose, it is essential to reduce the transistor's dimension continuously keeping the quality and the reliability of the devices very high with steady functionality and low power consumption. The probable method of semiconductor industry to improve productivity and performances is device scaling [1]. The MOSFET's size has continually been scaled down [2]. The rapid reduction of dimension will not always permit with device performances and creates problems that are yet to be solved. To solve the problem, a new design of MOSFET such as Silicon-on-Insulator (SOI) has been introduced. SOI refers to placing a thin layer of silicon on top of an insulator, usually silicon dioxide (SiO2) or known as buried oxide layer (BOX). SOI has advantages such as lower threshold voltage ,better sub threshold slope and no latch up[3-4].The reduced area of drain and source regions and reduction of junction capacitance makes SOI a promising candidate for reduced power and voltage applications [5-7]. There are two different types of SOI, which are partially depleted (PD) and fully depleted (FD) determined by the thickness of the top silicon film . Usually, the thickness of top silicon film is between 100nm to 500 nm for PD SOI device. The thickness of top silicon film is less than 100 nm for fully-depleted SOI devices. The threshold voltage can change in fully depleted SOI (FDSOI) MOSFET. The threshold voltage is almost constant in partially depleted SOI (PDSOI) device.

In spite of these advantages, certain undesirable effects such as kink [8] is present in the output current-voltage characteristics in PD-SOI MOSFETs. In these devices, high drain voltages create high electric field near the drain region. As a result, the high electric field causes electrons in the channel to acquire high energy and create electron hole pairs by impact ionization process. The created electrons are collected by the drain and the accumulated holes in the floating body results in an increase in the body potential. The threshold voltage drops as a consequence causing drain current to increase rapidly [9].The increase in drain current results in an increase in the number of holes created. This cumulative process will go on until the body source junction becomes forward biased, permitting the holes to exit the device. The nonlinearity created by the kink effect makes the device not a good choice for linear applications.

A body contact in these devices is a remedy for floating body problem[9]. It can eliminate the kink effect at the cost of die area [9]. These body contacts will result in body charge and discharge time constants. So its success is less pronounced. By controlling the carrier lifetime in the floating body region by high-dose silicon implantation it is possible to reduce the floating body effect of a SOI MOSFET. Amorphization of the silicon is created by ion implantation and generates recombination centers below the channel region. The lifetime of excess carriers created due to impact ionization is reduced due to recombination centers during device operation

and reduce the accumulation of hole in NMOSFET device thus minimizing the kink effect. The lattice damage causes reductions in the channel mobility. So the drive current is decreased [10].

The focus of present work is on the kink behavior of the PD SOI structure. Simulation study of PD SOI devices is performed using TCAD Silvaco software. The present work describes the reduction in kink in the output characteristics that can be obtained by decreasing the thickness of the gate oxide of the PD SOI structure.

II. Methodology

To investigate the output characteristics of SOI MOSFET a schematic cross-sectional view of the SOI MOSFET, shown in Fig.1, is simulated using Silvaco TCAD device simulator. The channel doping concentration used is 1×10^{17} cm^{-3} to avoid degrading of carrier mobility and more threshold voltage variations. The source/drain region doping concentration was kept at 1×10^{20} cm^{-3}. Gate length of the device is 1 µm. Buried oxide thickness and gate oxide (SiO_2) thickness is 0.4 µm and 25 nm respectively. The total device length including channel, drain and source is 3 µm. The silicon film thickness is 0.3 µm above the buried oxide. Lombardi CVT mobility model, Shockley-Read-Hall recombination, bandgap narrowing model and impact ionization model from Selberherr [11] is used for the simulation. Newton methods is used as numeric method for simulation.The device is simulated for different gate oxide thickness and it is an n channel SOI MOSFET.

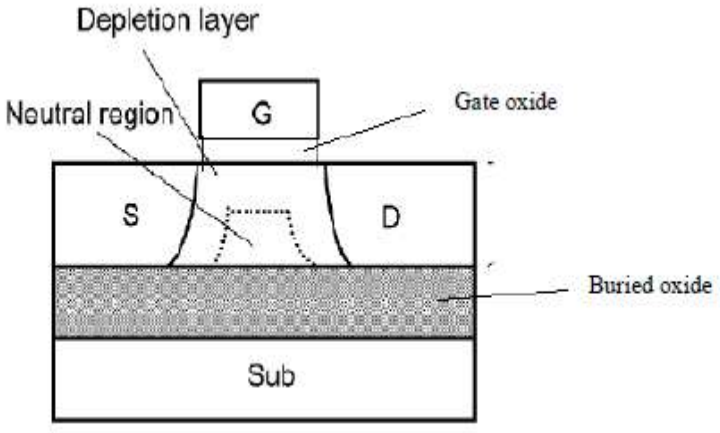

Fig.1. Schematic view of PD SOI MOSFET

III. Results and Discussion

The simulation result of the n-channel PDSOI MOSFET device structure is displayed in TonyPlot. SOI structures are created using Atlas syntax.The thickness and material are defined when specifying the structure region. Fig. 2 shows PD SOI structure and Fig. 3 shows doping profile of PDSOI simulated by Silvaco TCAD. This device has a gate oxide thickness of 25 nm and a gate length of 1 microns. Besides, thickness of silicon film is 0.3 µm and the buried oxide with thickness of 0.4 µm.

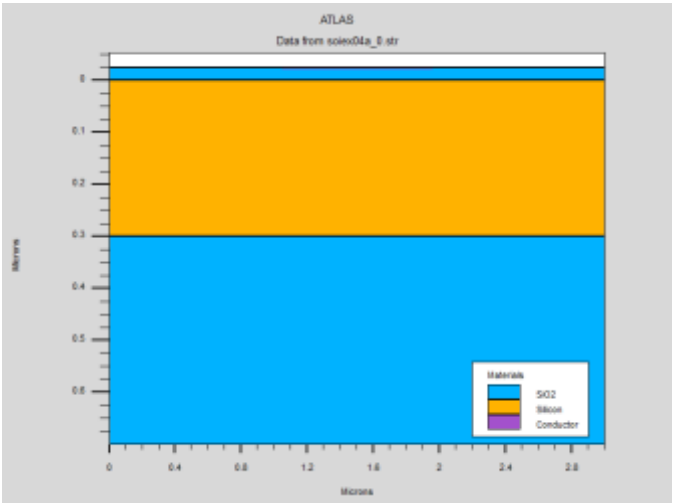

Fig.2. Simulated structure of PD-SOI n-MOSFET

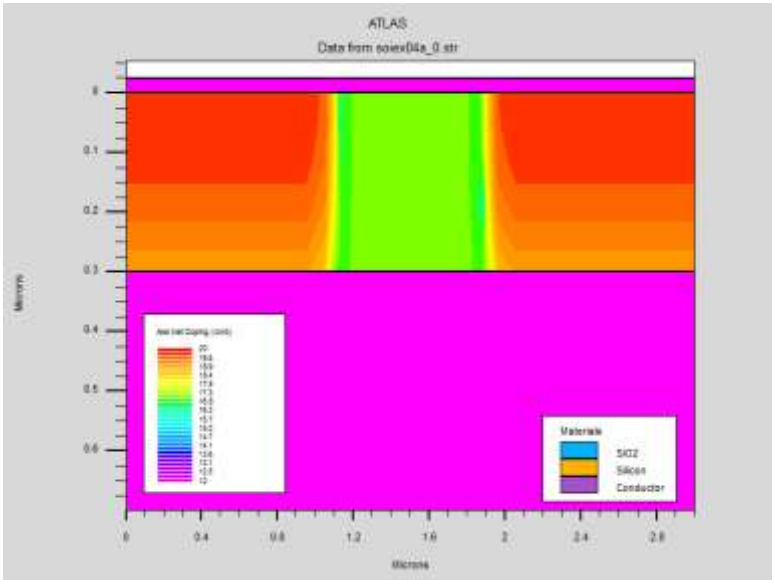

Fig. 3 Doping profile of PDSOI n-MOSFET

Fig. 4 (a),(b),(c),(d),(e) & (f) illustrates the output characteristics in the graph of Ids/Vds characteristics for Vgs=1V, 2V and 3V for channel length L=1μ m and various gate oxide thickness,Tox of PD SOI structure. Presence of kink in the output characteristics for SOI structure is clearly visible for Tox=25 nm.The onset of kink takes place at a kink voltage (Vkink) of 0.75 V,1.125 V and 1.5V for gate-source voltage of 1V,2V and 3V respectively for Tox=25 nm. The kink effect results in an increase in the drain conductance gd and reduction of the transconductance gm, thus degrading the performance of the transistors .To study the effect of gate oxide thickness on the kink voltage, the gate oxide thickness chosen are as 20 nm, 15 nm, 10 nm, 5 nm and 2 nm. The onset of kink increases to 0.875V, 1.25 V and 1.625 V for gate-source voltage of 1V,2V and 3V respectively for gate oxide thickness Tox=20 nm. When gate oxide thickness is decreased to Tox=15 nm the onset of kink takes place at a kink voltage (Vkink) of 1V,1.375 V and 1.75 V for gate-source voltage of 1V,2V and 3V respectively.The onset of kink further increases to a kink voltage (Vkink) of 1.1V,1.5 V and 1.8 V for gate-source voltage of 1V,2V and 3V respectively for Tox=10 nm. The kink voltage is found to be increasing with decrease in the gate oxide thickness for a fixed gate to source voltage. It is noticed that kink completely disappears for gate oxide thickness of 5 nm and below. The simulation results of Fig.4 confirm that for Tox = 2 nm, the current Ids is about 12 times larger than the current Ids obtained for Tox = 25 nm for Vgs=3V.

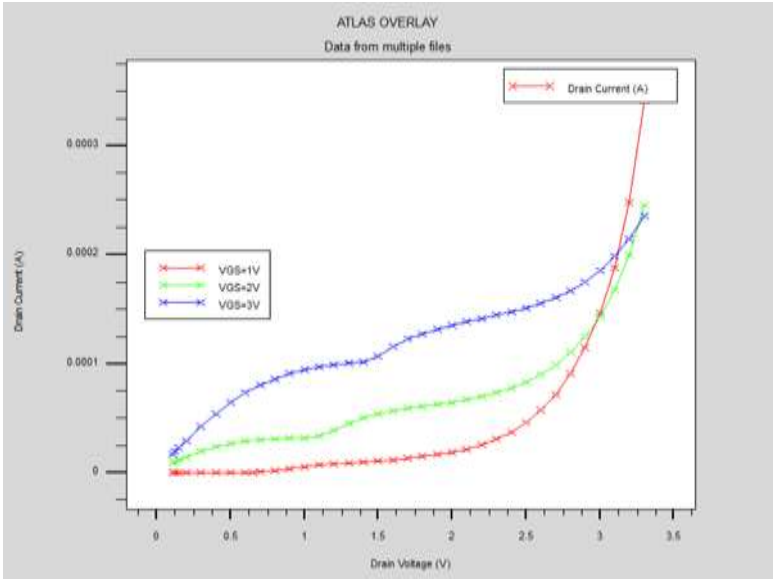

Fig. 4(a) Simulated output characteristics Ids-Vds of PDSOI n-MOSFET with channel length L=1 μm and for gate oxide thickness Tox=25 nm

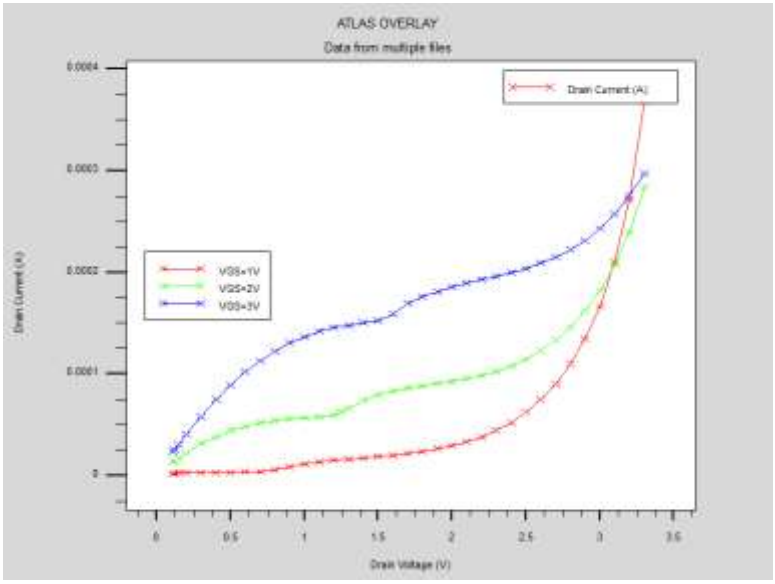

Fig.4(b) Simulated output characteristics Ids-Vds of PDSOI n-MOSFET with channel length L=1 µm and for gate oxide thickness Tox=20 nm.

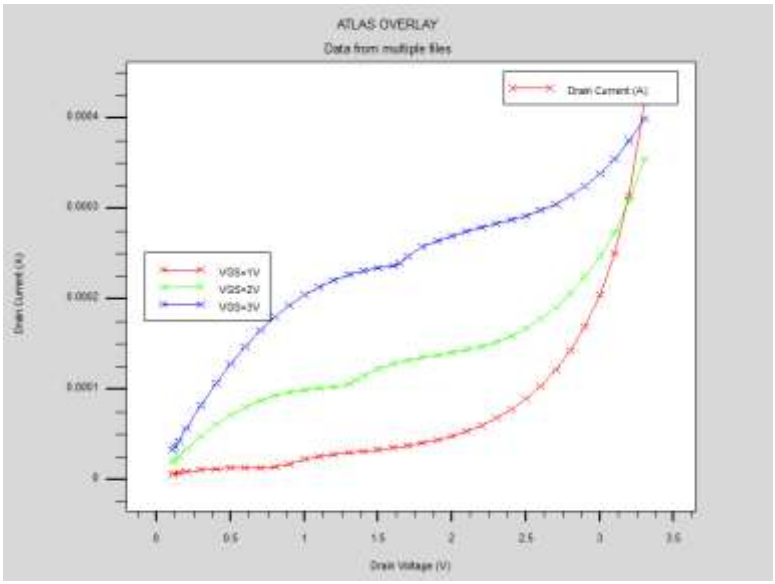

Fig.4(c) Simulated output characteristics Ids-Vds of PDSOI n-MOSFET with channel length L=1 µm and for gate oxide thickness Tox=15 nm.

.

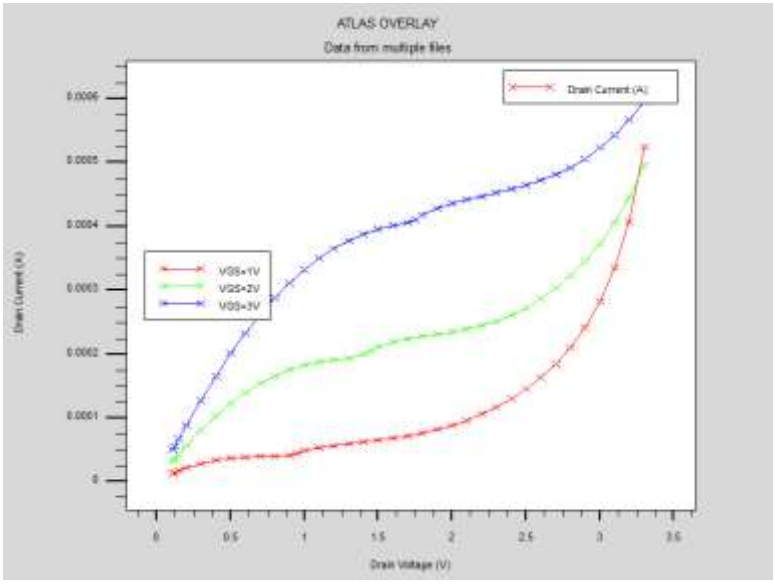

Fig. 4(d) Simulated output characteristics Ids-Vds of PDSOI n-MOSFET with channel length L=1 µm and for gate oxide thickness Tox=10 nm.

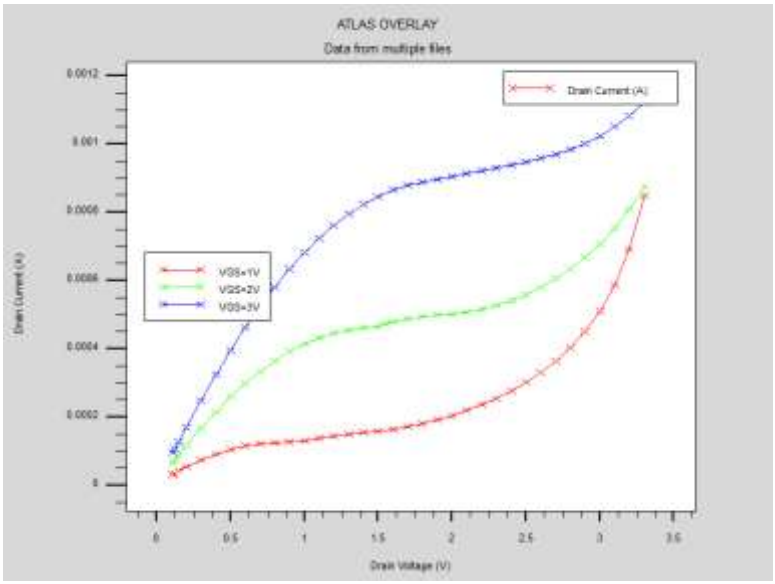

Fig.4(e) Simulated output characteristics Ids-Vds of PDSOI n-MOSFET with channel length L=1 µm and for gate oxide thickness Tox=5 nm.

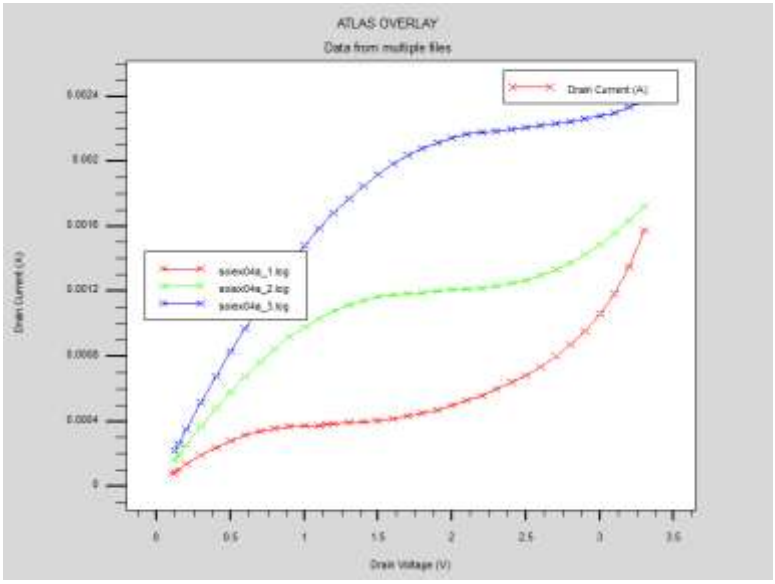

Fig.4(f) Simulated output characteristics Ids-Vds of PDSOI n-MOSFET with channel length L=1 µm and for gate oxide thickness Tox=2 nm.

The transfer characteristics Ids/Vgs for PD SOI n-MOSFET is shown in Fig.5 for various gate oxide thickness. Threshold voltage decreases as gate oxide thickness decreases. Smaller threshold voltage meets high performance of device with scaling of technology [12]. PD SOI MOSFET's threshold voltages are recorded by varying the gate oxide thickness as shown in Table I. MOSFET's gate threshold voltage, Vgs(Vth) is the voltage between the gate and source needed to turn it on [4]. With decrease of gate oxide thickness threshold voltage decreases and kink effect disappears for gate oxide thickness of 5 nm or less for the simulated structure.

Table no 1. Shows threshold voltage of PD SOI n-MOSFET at different gate oxide thickness.

Gate Oxide Thickness,Tox(nm)	Threshold Voltage,Vth(V)
25	1.00312
20	0.780558
15	0.557703
10	0.337042
5	0.121749
2	0.00166292

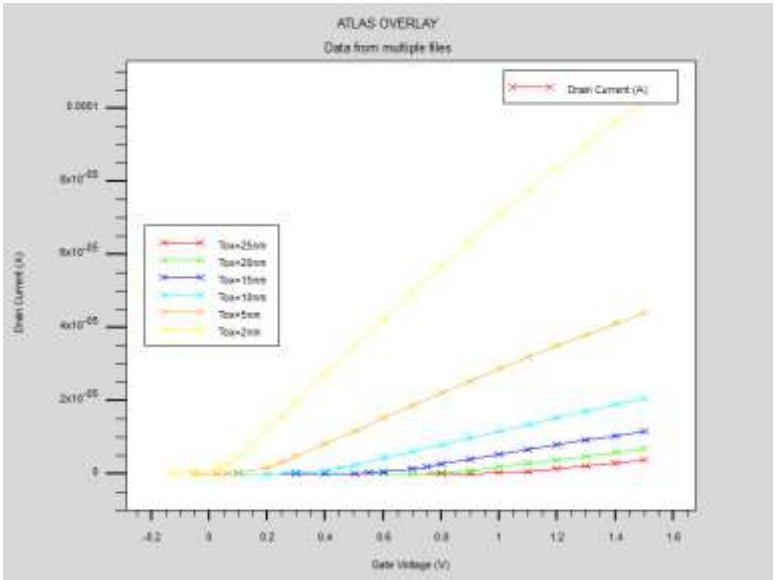

Fig. 5 Simulated transfer characteristics I_{ds}-V_{ds} of PDSOI n-MOSFET with channel length L=1 µm and for various gate oxide thickness Tox.

IV. Conclusion

The PD SOI n-MOSFET is simulated using Atlas-SILVACO tool. Accumulation of holes on the floating body changes the body voltage of the device which results in rapid increase in the drain current in the output current voltage characteristics which is known as kink. If the gate oxide thickness is decreased, threshold voltage decreases and the voltage at which kink occurs increases for a fixed gate to source voltage. When the gate oxide thickness is 5nm or below for the simulated structure, kink effect virtually disappears as seen from simulated results.

References

[1]. F. Z. Rahou, A. Guen-Bouazza and M. Rahou, "Electrical characteristics comparison between fully-depleted SOI MOSFET and partially-depleted SOI MOSFET using Silvaco software," Global Journal of Researches in Engineering Electrical and Electronics Engineering,13(1), 2013.

[2]. Y. Husaini,M.H. Ismail,A.S. Zoolfakar and N. Khairudin, "Electrical characteristics comparison between partially-depleted SOI and n-MOS devices investigation using Silvaco," IEEE 2010 IEEE Symposium on Industrial Electronics and Applications,pp.532-536, October 3-5, 2010.

[3]. N. Gupta, J.K.B. Patel and A.K.Raghav, "Performance and a new 2-D analytical modeling of a Dual-Halo Dual-Dielectric Triple-Material Surrounding-Gate-All-Around (DH-DD-TM-SGAA) MOSFET" ,Journal of Engineering Science and Technology, vol. 13(11), pp.3619-3631,Nov. 2018.

[4]. N.Gupta, J.K.B.Patel and A.K.Raghav,"An accurate 2D Analytical Model for Transconductance-to-Drain Current ratio (gm/Id) for a Dual-Halo Dual-Dielectric Triple-Material Cylindrical-Gate–All-Around (DH-DD-TM-CGAA) MOSFETs,"International Journal of Engineering, vol. 31,no. 07,pp. 1038-1043,July 2018.

[5]. Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," IEEE Transactions on Electron Devices, vol. 48, no. 12, pp. 2861–2869, Dec. 2001.

[6]. N.Gupta, J. Patel and A.K.Raghav, "A Study of Conventional and Junctionless MOSFET Using TCAD Simulations", IEEE International Conference on Advanced Computing & Communication Technologies, pp. 53-56, Haryana,India,2015.

[7]. S. Rewari, S. Haldar, V.Nath, S.S. Deswal, and R.S. Gupta, "Numerical modeling of subthreshold region of Junctionless Double Surrounding Gate MOSFET (JDSG) ," Superlattices and Microstructures, vol. 90, pp 8-19, Feb 2016.

[8]. K. Bernstein and N.J. Rohrer, "SOI Circuit Design Concepts,"Kluwer Academic Publishers, 2000.

[9]. A.Marshall and S. Natarajan, "SOI Design: Analog,Memory and Digital Techniques," Kluwer Academic Publishers, 2001.

[10]. J. Z. Ren and C. A. T. Salama, "1 V SOI NMOSFET with suppressed floating body effects," Solid-State Electronics, vol. 44, (11), pp. 1931–1937, 2000.

[11]. ATLAS User's Manual Device Simulation Software, Silvaco International, Santa Clara, Calif., USA, 2004.

[12]. A. Verma, A. Mishra, A. Singh and A. Agrawal, "Effect of threshold voltage on various CMOS performance parameter," International Journal of Engineering Research and Applications, vol.4(4), pp.21–28, 2014.