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Review of high speed convolutional encoder design using ancient Indian Vedic Sutra

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ABSTRACT : *In mathematics, multiplication is the most commonly used operation such as DSP application. This paper will explores the design approach of a convolution encoder using vedic multiplier and booth multiplier which will lead to improved delay and faster speed. Here, the efficiency of Urdhva Triyagbhyam Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of partial products and eliminates unwanted multiplication steps. This algorithm follows a fast multiplication process and achieves a significantly less computational complexity over its conventional counterparts. Finally, the coding will be done in VHDL and synthesis will be done using Xilinx ISE simulator. Results will be compared with these techniques.*

Keywords - *Convolutional Encoder, Multiplier, Urdhava Tiryakbhyam, Vedic Mathematics.*

I. INTRODUCTION

An encoder is a device that converts information from one format to another, for the purposes of faithful recovery of message bits. The terms encoding is used in reference to the process of analog-to-digital conversion. Convolutional encoding is error correction scheme. This coding scheme is often used in the field of deep space communications and more recently in digital wireless communications. It is very efficient and robust. In most of real time applications like audio and video applications, the Convolutional codes are used for error correction. The cost for the convolutional encoder is expensive for a specified design because of the patent issue. Therefore, to realize an adaptive Convolutional encoder on a field programmable gate array (FPGA) board is very demanding. we concern with designing and implementing a convolutional encoder which is the essential block in digital communication systems using FPGA technology. Convolutional codes offer an alternative to block codes for transmission over a noisy channel. Convolutional coding can be applied to a continuous input stream as well as blocks of data.

The Convolutional encoder encodes the message and then the encoded bits are generated. Convolutional codes are commonly described using two parameters: the code rate and the constraint length. The code rate, k/n, is expressed as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. The constraint length parameter, K, denotes the "length" of the convolutional encoder, i.e. how many k-bit stages are available to feed the combinatorial logic that produces the output symbols. A simple convolutional encoder is shown in Figure 1.

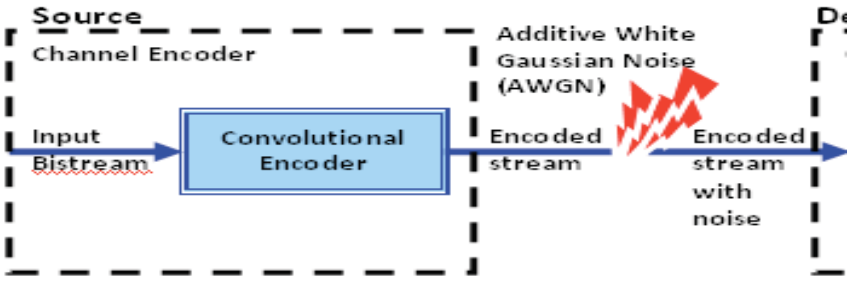

FIGURE1: CONVOLUTIONAL ENCODER [8]

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Multiplication is an important fundamental function in arithmetic operation. Booth's algorithm is a well-known method for 2's complement multiplication. It speeds up the process by analyzing multiple bits of multiplier at a time. This widely used scheme for two's complement multiplication was designed by Andrew D. Booth in 1951. Booth algorithm is an elegant way for this type of multiplication which treats both positive and negative operands uniformly. It allows n-bit multiplication to be done using fewer than n additions or subtractions, thereby making possible faster multiplication. According to Booth's multiplication algorithm among the two input binary numbers the one with minimum number of bit changes is considered as multiplier and the other as a multiplicand in order to reduce the time taken for calculating the multiplication product[9].

Urdhva tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional methods already know to us will require 16 multiplications and 15 additions. An alternative method of multiplication using Urdhva tiryakbhyam Sutra is shown in Fig. 3. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero .

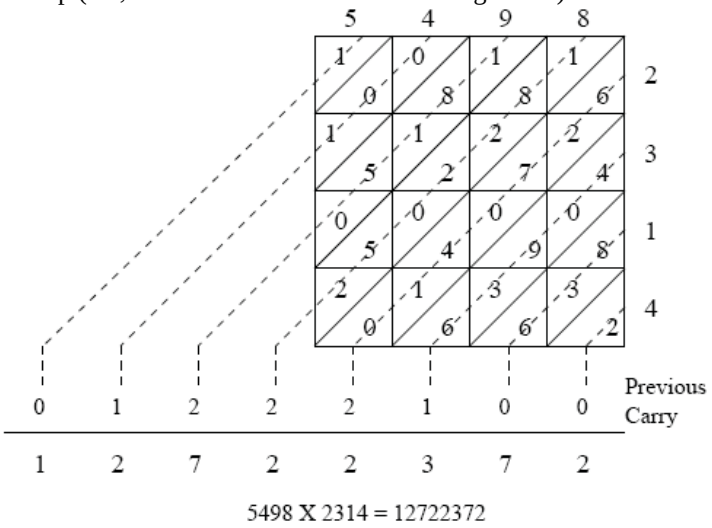

FIGURE 2: ALTERNATIVE WAY OF MULTIPLICATION BY URDHVA TIRYAKBHYAM SUTRA [1].

II. RELATED WORK

Honey Durga Tiwari [1] presents a design implementation on ALTERA Cyclone –II FPGA, shows that the proposed Vedic multiplier and square are faster than array multiplier and Booth multiplier. A new reduced-bit multiplication algorithm based on a formula of ancient Indian Vedic mathematics has been proposed. Both the Vedic multiplication formulae, Urdhva tiryakbhyam and Nikhilam, have been investigated in detail. Urdhva tiryakbhyam, being general mathematical formula, is equally applicable to all cases of multiplication. A multiplier architecture based on this Sutra has been developed and is seen to be similar to the popular array multiplier where an array of adders is required to arrive at the final product. Due to its structure, it

suffers from a high carry propagation delay in case of multiplication of large numbers. This problem has been solved by introducing Nikhilam Sutra which reduces the multiplication of two large numbers to the multiplication of two small numbers. The framework of the proposed algorithm is taken from this Sutra and is further optimized by use of some general arithmetic operations such as expansion and bit shifting to take full advantage of bit-reduction in multiplication. The computational efficiency of the algorithm has been illustrated by reducing a general 4 × 4-bit multiplication to a single 2 × 2- bit multiplication operation. The FPGA implementation result shows that the delay and the area required in proposed design is far less than the conventional booth and array multiplier designs making them efficient for the use in various applications.

Shamim Akhter [2] presents a novel technique for digital multiplication is presented that is quite different from the conventional method of multiplication like add and shift. This also gives chances for modular design where smaller block can be used to design the bigger one. This will help in designing multiplier in VHDL, as its give effective utilization of structural method of modeling. In this paper the general technique for NxN multiplication is proposed. This gives less computation time for calculating the multiplication result for NxN bit. In this paper, a new method of digit multiplication is presented. The design is based on Vedic method of multiplication. This gives us method for hierarchical multiplier design. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased.

Ms.G.S. Suganya [4] focuses on the realization of an efficient logic design of a crypto system. The type of crypto system considered in this paper is convolutional encoder with a constraint length, K of 3 and a code rate (k/n) of 1/2 using field programmable gate array (FPGA) technology. Here, the features of Convolutional encoder architecture are introduced and the way it can be implementable as an ASIC . The system is realized using Verilog HDL. It is simulated and synthesized using Modelsim Altera Starter Edition6.6d and Xilinx 9.1 for RTL Design. In this paper, we have presented the design and implementation of the Convolutional encoder. This design has been simulated in MODELSIM altera 6.6d and synthesized using XILINX-ISE 12.4i for the constraint length of K=7 and code rate of ½ input sequence. The given input sequence has been encoded by using convolutional encoder and it is transmitted through the channel.

V.Kavinilavu [5] presents a Convolutional encoder with a constraint length of 7 and code rate of 1/2. This is realized using Verilog HDL. It is simulated and synthesized using Modelsim PE 10.0e and Xilinx 12.4i. In this paper, we have presented the design and implementation of the Convolutional encoder. This design has been simulated in MODELSIM 10.0e and synthesized using XILINX-ISE 12.4i for the constraint length of K=7 and code rate of ½ input sequence. The given input sequence has been encoded by using convolutional encoder and it is transmitted through the channel.

Anuradha Kulkarni [6] presents a research work which deals with the implementation of convolution encoder using system on programming chip (SOPC). It uses variable constraint length of 7, 8 and 9 bits for 1/2 and 1/3 code rates. The reduced bit error rate with increasing constraint length shows an increase in efficiency and better utilization of resources as bandwidth and power. In this paper, we explore the SOPC based convolution encoder. The convolution encoder is tested for different constraint length of 7, 8 and 9 bits.

Sishir Kalita et.al [7] presents a new method of convolutional encoding is proposed using the general Booth algorithm for multiplication. This algorithm follows a fast multiplication process and achieves a significantly less computational complexity over its conventional counterparts. It can be a useful technique for use in chip design as it provides significant improvements. In this work, the performance of conventional convolutional coding in AWGN channel, is studied and the results show the effectiveness of the work described here. In this paper simulation results are presented on the performance of convolutional codes which are the widely used forward error correcting codes. The studies are made by appropriately modeling different systems for the two PSK modulation schemes and studying the performance of Convolutional Codes with respect to SNR noting the BERs for the cases when the encoder is a conventional one or a Booth multiplier based one. The work offers an insight into the development of a method for generating convolutional codes with faster multiplication and proves effective in arrange of wireless channels. The Booth encoder not only offers a fast multiplication, it also reduces the transmitter power and a less BER value is obtained at a specified SNR compared to the conventional process. A fast and energy-efficient encoder is such an important element which contributes substantially to the total power consumption of the system. On VLSI level, the area also becomes quite important as it is related to packing density and system cost. The Booth multiplication based convolutional encoder is thus designed keeping in mind these aspects.

III. PROPOSED WORK

Since multiplication dominates the execution time, so there is a need of high speed multiplier. Multiplier based on Vedic Mathematics and booth algorithm is one of the fast multiplier. By introducing Vedic multiplication and booth multiplication in design of convolutional encoder improves processing speed and results into improved processing delay. This can be done by using Vedic algorithm and booth algorithm using Boolean logic. Vedic mathematics provides logical ability to the circuit for fast computation. The delays of Vedic multiplier and booth multiplier of convolutional encoder will be compared. Structural modeling will be preferred for designing of convolution encoder.

Convolution encoder consist of combinational logic and memory elements. For designing of convolution encoder, booth multiplier and vedic multiplier as a combinational logic and flip flops as a memory element will be used. The proposed convolution encoder using booth multiplier is as follows;

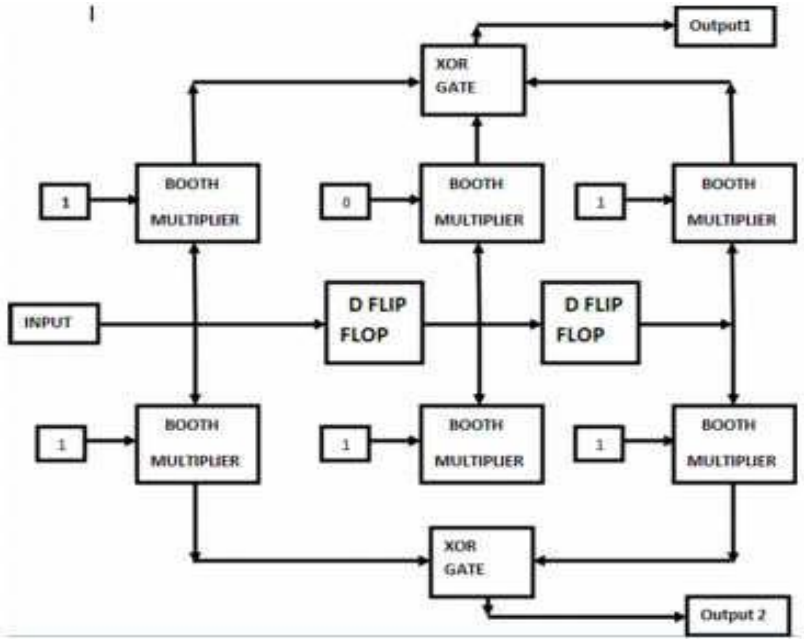

FIGURE 3: THE PROPOSED CONVOLUTION ENCODER USING BOOTH MULTIPLIER [7]

This architecture can be replaced by vedic multiplier rather than booth multiplier.

IV. CONCLUSION AND FUTURE SCOPE

The design complexity gets reduced for inputs of large number of bits and modularity gets increased [2]. The advantages of the proposed architecture is efficient in speed and area and is Flexible in design [3]. Now this paper will present a new method of multiplication. The design will be based on Vedic method of multiplication. Compared to a conventional encoder, the Booth multipler based convolutional encoder will generate on an average 10 to 15% time improvements. This work will achieve the improved delay of convolutional encoder using vedic multiplier than booth multiplier. This gives us method for hierarchical multiplier design. So the design complexity will get reduced for inputs of large number of bits and will a provide faster speed. It will also used to design a PN sequence generator and spread spectrum modulation to improve the utilization of bandwidth.

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