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Review on Performance and Hardware Complexity of Multipliers

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REVIEW ON PERFORMANCE AND HARDWARE COMPLEXITY OF MUTIPLIERS

Abstract:
Multiplier is a key component which is majorly used in Digital electronics and Digital Signal Processing.Multiplier is a component or electronic circuit which gives product of two binary numbers. Multiplier with high speed, low power consumption and less size is preferred in the Digital Electronic field. That's why Multipliers with low power consumption and low hardware complexity got huge demand and it is always challenging to create a multiplier with these specifications. There are different Multipliers but most popular among them are Wallace Multiplier,Braun Multiplier and Dadda Multiplier.These Multipliers are differed according to their respective algorithms.Here we majorly discussed about 90 nm technology. In this paper, we discuss and review on low power multipliers with it's hardware and performance with comparisons.

Keywords:
Multiplier, Wallace Algorithm, Braun Multiplier, Dadda Multiplier, Low Power, Hardware Complexity, Hybrid adders, Complementary pass logic, CMOS.

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I. Introduction

Multipliers are widely used in the applications of digital signal processing. Being an application of digital signal processing, there is necessity for a multiplier to be fast, low power consumption, low area capacity and most important one, the result to be accurate. Now-a-days, multipliers got a huge demand with these parameters.

This literature review is explained in Ⅲ sections. Section Ⅰ describes about multipliers with different algorithms. Section Ⅱ describes about adder circuits for building the multiplier and section Ⅲ gives conclusion.

SECTION Ⅰ

Wallace Multiplier is a tree multiplier which is very efficient and accurate. This tree algorithm describes the multiplication technique to get the product fast and accurate. The partial products which we get from the multiplication of two N-bit unsigned numbers are added in a different manner (like to add up columns, add up three rows at a time) and finally we get the product. Also, there is another technique through Wallace multiplier generates partial product and this partial product is send to a partial product processing module which contains combination of full adders and half adders are used and follows this algorithm,

$T_{(i+1)}=2(T_i/3)+T_i \mod 3$

Where, T_i is the no. of rows in a particular stage.

Dadda Multiplier is also similar to Wallace Multiplier but some changes can be observed. Same as Wallace Multiplier but after generation of partial products, these are arranged in rows and columns and we must make all the partial product in each column are equal. When there are 'i' partial products in column, we use this formula,

$$D(i+1) = 3 * D(i)/2$$

Braun Multiplier is the simplest is all parallel Multiplier. Here all partial products are gathered in parallel form and these are collected through adders(with stages).

From these Multipliers, the hardware complexities and low-power consumption values are given below,

- Wallace and Braun Multipliers uses 550 and 580 transistors as we said Wallace hardware is similar to Dadda Multiplier.
- No. of AND gates used are equal in both Multipliers but, Braun Multiplier uses 12 Full adders whereas Wallace Multiplier only uses 10 adders as we observe from Table 1.
- The Power Consumption of Conventional Multiplier is more than Designed Wallace Multiplier as we observe from Table 2.But Designed Wallace Multiplier consumed some more power compared to Conventional Multiplier.
- In the case of speed, Dadda Multiplier is slightly faster than Wallace Multiplier.

Table 1: No. of AND Gates, Full Adders and Transistors used in Braun and Wallace Multiplier.

Multiplier	Braun Multiplier	Wallace Multiplier
No. of AND gates	16	16
No. of Full Adders	12	10
No. of Transistors	580	550

Table 2: SIMULATION RESULTS FOR NAND,NOR, MUX AND XOR

Type	Power(μW)	Delay (ns)	PDP (fJ)	EDP (zJs)
Conventional	6.75	25	168.75	4.22
Designed Multiplier	7.12	20.7	147.38	3.05

Here PDP is Power Delay Product and EDP is Energy Delay Product.

SECTION Ⅱ

Adder circuits are the deciding factor for Hardware complexity of Multipliers. More Adder circuits, more hardware complexity exists. So, design of adder circuits to cover less area with good accuracy became challenging. Here, we analyse the power and hardware parameters of CMOS, CPL (complementary pass logic) and Hybrid adders.

CMOS full adder circuit has more delay which becomes disadvantage to multiplier. Now, complementary pass logic(CPL) has less delay compared to CMOS full adder but has higher average power, power delay product and in transistor count, this increases hardware complexity and also consumes more power as per our needs in today's technology.But in hybrid adder, parameters like Delay, Average power, power Delay Product and in Transistor count, it's significantly less compared to CMOS Full adder and CPL. But sometimes, by giving more Inout voltage, Delay of Hybrid adder crosses CPL but not as per CMOS Full adder circuit.We can observe these in Table 3.Andfrom Table 4, we can observe the Dynamic and Static Power Dissipations at 1.8 V.Here,dynamic power is the dominant power dissipation component.It's due to charging and discharging of load capacitances.

Table 3.SIMULATION RESULTS of Adder Circuits at 1.8,1.5,1.2 and 1 V.

Power Supply (V)	Adder Circuit	Delay (ps)	Average Power (μW)	PDP (fJ)	Transistor Count
1	CMOS	740.0	1.579	1.168	28
	CPL	476.20	1.770	8.428	38
	Hybrid	86.86	1.217	0.1057	16
1.2	CMOS	507.3	2.366	1.200	28
	CPL	337.5	2.647	0.8934	38
	Hybrid	171.18	1.782	0.3050	16
1.5	CMOS	334.8	3.978	1.332	28
	CPL	238.2	4.351	1.036	38
	Hybrid	201.65	2.854	0.5755	16
1.8	CMOS	251.7	5.542	1.395	28
	CPL	188.0	6.520	1.225	38
	Hybrid	233.64	4.189	0.9787	16

Table 4. Static and Dynamic Power consumption at 1.8 V

Adder circuit	Static Power	Dynamic Power
CMOS	374.0 pW	5.5416 μW
CPL	1.383 nW	6.5186 μW
Hybrid	233.1 pW	4.1887 μW

SECTION Ⅲ

II. Conclusion

This review suggests the best multiplier in terms of low power design with less hardware complexity from the references. This review helps the researchers and students to sort out Multipliers to make the best one.

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