IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.
PP 12-18
www.iosrjournals.org

Performance Analysis Of Multi Carrier CDMA System

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Abstract: *A novel chaotic spreading sequences for Multi-carrier code division multiple access (MC-CDMA) system is proposed. DS-CDMA is a type of spread-spectrum communication system in which multiple signal channels occupy the same frequency band, been distinguished by the use of different spreading codes. Implementation of Multi carrier CDMA transmitter and receiver using pseudo chaotic sequences for spreading digital data using Field Programmable Gate Array (FPGA) has been proposed in this paper. The generated pseudo-chaotic sequences are investigated for auto-correlation, cross-correlation and balance properties. The Bit error rate (BER) performance of the system is evaluated in multi-user environment under AWGN channel and reveals that the MC-CDMA system using pseudo-chaotic sequences as spreading sequences significantly outperforms the conventional PN sequences.*

***Keywords** – MC-CDMA, chaotic sequences, pseudo chaotic sequence generator, FPGA.*

I. INTRODUCTION

MULTI-CARRIER Code Division Multiple Access (MC-CDMA), based on a combination of CDMA and orthogonal frequency division multiplexing (OFDM), is a major candidate for the transmission technology of the forthcoming 4th generation mobile communication system. In MC-CDMA systems, data symbols can be spread in the frequency or time domain by using a given spreading code [1]. It has been reported that time-domain spreading MC-CDMA systems have superior BER performance to frequency-domain spreading MC-CDMA systems, which are degraded by multiple access interference in severe frequency selective fading environments, especially when a lot of multiplexing codes are used [7]. Moreover, the time-domain spreading systems can enjoy

Frequency diversity effect similar to the Frequency-domain spreading systems by applying forward error correction with bit-interleaving in the frequency domain. In time-domain spreading MC-CDMA systems, it is usual to spread data and pilot symbols in the time domain and code-multiplex them [6]. Utilizing those code-multiplexed pilot symbols, we need to realize accurate channel estimation.

For time-domain spreading MC-CDMA systems, considering the code-multiplexed pilot symbols, it is effective to utilize adjacent pilot symbols in both time and frequency domains. To combat the variation in fading correlation among pilot symbols, which is determined by propagation attributes such as the maximum Doppler frequency in the time domain and delay spread in the frequency domain, we introduced a two dimensional method. The impulse response, which is obtained by inversely Fourier transforming the estimated frequency responses, has the path elements only in the guard interval duration. Therefore, by removing elements outside the guard interval duration, another accuracy improvement of channel estimation can be realized [9]. It is important for adaptive channel estimation methods like our proposal to determine the appropriate weight factor for each fading environment.

For OFDM systems, some studies have examined the weight factors for the frequency domain averaging of the channel estimates as in [9] and its references. However, the integration of time-domain averaging, frequency-domain averaging and impulse response-based channel estimation method has not been proposed. The binary pseudo-noise (PN) sequences have been used extensively in spread spectrum (SS) communication systems. One of the most commonly used PN sequences in DS-SS is maximal length sequences (m-sequences). The length of m-sequences depends on the number of shift registers. Good correlation properties can be achieved with m-sequences. The ability to predict future sequence is nevertheless possible though difficult. Therefore transmission is not completely secured.

The number of sequences generated by Linear Feedback Shift Registers (LFSR) may be insufficient for wideband DS-SS with a very large number of users. In addition, LFSR techniques provide limited flexibility in incorporating security into multiple user systems [2]. The generated PN sequence is always periodic with a period of N=2m-1. Where 'm' indicates is the length of the shift register. The use of chaotic sequences as spreading sequences has been proposed in the literature because of its sensitivity to initial conditions and has characteristics similar to random noise. However reliable electronic hardware implementations of chaos-based PN sequence generators based on recursion of maps realized by piecewise linear analogue functions and output quantization have not been possible due to manufacturing process variations among different integrated circuit production lots, transistor mismatches and electronic noise. In this paper PN sequences are replaced by a new kind of sequences called chaotic sequences.

The pseudo-chaotic sequence generators presented in and are in the class of Non Linear Feedback Shift Registers (NLFSR). Many authors have shown that chaotic spreading sequence can be used as an inexpensive alternative to the LFSR sequences such as m-sequences and Gold sequences. The remaining sections of this paper are organized as follows. In section II the generation of pseudo- chaotic sequences and their suitability in multiple access is described. The FPGA implementation of MC-CDMA system along with PCS generator is presented in section III. In section IV a detailed discussion of the performance of the proposed scheme and some experimental results are presented. The paper is concluded with some remarks in section V.

II. GENERATION OF PSEUDO-CHAOTIC SEQUENCES

Pseudo noise (PN) is defined as a coded sequence of 1's and 0's with certain auto-correlation properties [4]. The system of sequences used in spread spectrum communication is usually periodic in that a sequence of 1's and 0's repeats itself exactly with a known period. The m-sequence represents a commonly used periodic PN sequence. Such sequences are long periods and require simple instrumentation in the form of a LFSR. Indeed, they possess the longest possible period for this method of generation. A shift register of length m consists of m flip-flops (two state memory stages) regulated by a single timing clock. At each pulse of the clock, the state of each flip-flop is shifted to the next one down the line that is Ext flip-flop. In a feedback shift register of the linear type, the feedback function is obtained using modulo-2 addition (XORed) of the outputs of the various flips-flops. The generated m-sequence is always periodic with a period of N=2m-1 where m indicates the length of the shift register.

The highlight of this paper is the PCS Generator, which generates a pseudo-chaotic PN sequence with good cross-correlation and auto-correlation properties that is well suited for DS-SS system. Because of long periodicity, it provides very high security and is capable of handling many users. It consists of a cascade of four basic cells with two 8-bit programmable registers each. The output of the last cell i.e. each bit of the last cell output are XORed together to obtain pseudo-chaotic sequence and also this bit is fed back to the system to maintain nonlinearity that's we called as (NLFSR). By increasing number of cells and size of the registers, we can

Increase the number of users and period of the sequence. Since the number of implementation possibilities are very high due to just changing only initial condition programmability, this new system of sequence is inherently more difficult to intercept [6].

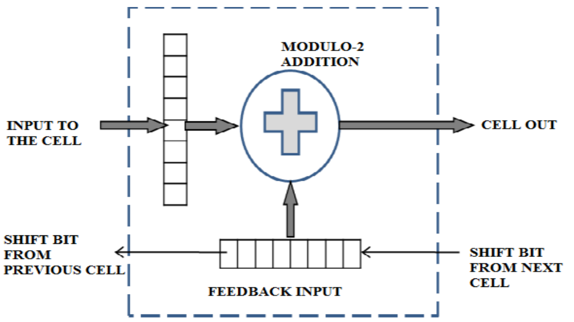

Fig. 1. Basic NLFSR cell structure

Fig. 1. shows a basic NLFSR cell, each cell consists of two 8-bit registers and a XOR function block. Initial conditions are set to both the registers. The contents of the two registers are XORed (modulo-2 addition) to obtain 8- bit output Cell out, which is used as input to the upper register of the next NLFSR cell. The contents of the two registers are altered for the next iterations by shifting the contents of the lower register towards left. The most significant bit that shifts out of the register is loaded into the least significant bit place of the feedback register of the previous cell. Similarly, the shifted bit from the next cell is moved into most significant bit place of the lower (feedback) register. The contents of the upper register are replaced by the 8-bit output of the previous cell. The PCS generator used in this paper consists of four such cells connected in series as shown in Fig. 2.

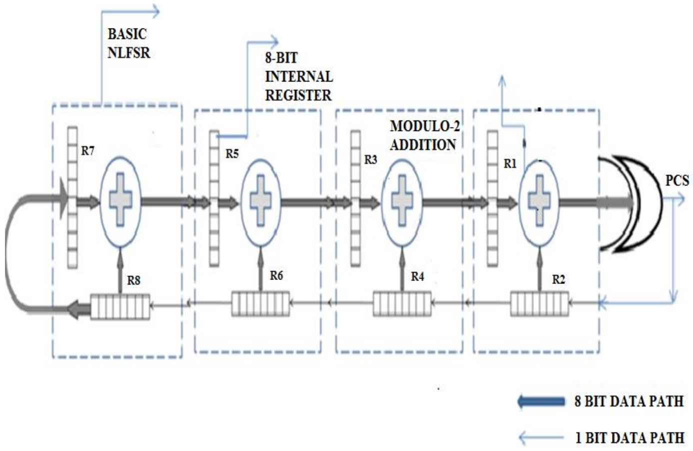

Fig. 2. Pseudo Chaotic Sequence Generator

The two trajectories with very close initial condition have been observed to diverge quickly and remain that way for large number of iterations, indicating the sensitive dependence on initial conditions. Next, to assess the performance of the PCS generator, the output sequences have been characterized with respect to their auto-correlation, cross-correlation and balance properties.

Auto correlation is measure of how well a signal can differentiate between itself and every time-shifted variant of itself. The normalized hamming auto correlation function of a sequence is defined in equation (1).

$$R_{xx}(\iota)= (n_\iota - d_\iota) / N \quad 0 \le \iota \le N-1 \qquad (1)$$

Where n_ι and d_ι are number of agreements and disagreements respectively to a N length sequence for any correlative distance ι.

Cross-correlation is defined as the correlation between two different signals. Cross-correlation is also calculated by subtracting the disagreements from the agreements, between two different sequences as opposed to the time-shifted replicas of the same signal. The normalized hamming cross correlation function of a pair of sequences is defined in equation (2).

$$R_{xy}(\iota) = (n_\iota - d_\iota) / N \,, \quad 0 \le \iota \le N-1 \qquad (2)$$

An exhaustive search was conducted to characterize the length of the sequences generated by the pseudo-chaotic finite state machines. In particular, the four stages cascaded structure in Fig. 2. was studied. The PCS generator contains eight 8-bit registers. These registers provide a total of 64 binary memory elements. Therefore, the PCS generator can be viewed as a Sequential state machine with at most 264 possible states. The initial values to these registers can be initialized individually

III. III. FPGA IMPLEMENTATION OF MC-CDMA SYSTEM ALONG WITH PCS GENERATOR

In this paper, we have replaced the conventional PN sequence by PCS (pseudo-chaotic sequence) for a MC-CDMA system. The block diagram of the implemented MC-CDMA system with transmitter and receiver, and inter connection between them is shown in Fig. 3. In this figure channel is the only connection between transmitter and receiver; assuming clock has been synchronized and channel is ideal.

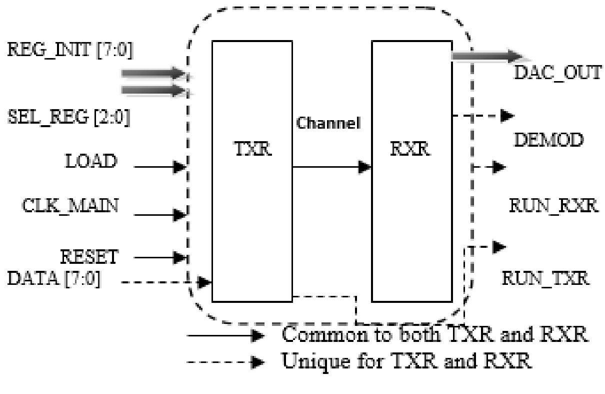

Fig. 3. Block Diagram of MC-CDMA with Transmitter And Receiver

A. **TRANSMITTER**.

The block diagram of the MC-CDMA transmitter is shown in Fig. 4. In MC-CDMA system, the original input data is first converted from serial stream into parallel stream and then modulated by the chaotic phase shift keying (CPSK) modulator. In order to reduce aliasing in D/A conversion, sub-carriers at or near the Nyquist frequency need to be avoided by inserting zeros. Assuming 16 samples, [1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16], are selected to do IFFT calculation, they need to be arranged as [0 2 3 4 5 6 7 0 0 0 11 12 13 14 15 16] before IFFT calculation.

Next the arranged data is processed by Inverse Fast Fourier Transform (IFFT) and converted back to serial data for transmission in time domain. Specifically, the IFFT converts the data in frequency domain into the corresponding representation of this data in time domain with the spectrum of each sub-carrier satisfying orthogonality conditions.

After performing IFFT calculation, interleaving operation is performed and cyclically extended guard interval is applied between symbols to eliminate ISI caused by multi-path distortion. In more details, a periodic extension of each MC-CDMA symbol is inserted and the duration of guard interval.

B.RECEIVER

Multi-carrier CDMA can be implemented using either time domain processing, where it is treated as a special case of direct sequence CDMA (but with non-bipolar codes), or using frequency domain processing. A frequency domain processing multi-carrier CDMA receiver contains two main system blocks, a FFT block to demodulate the OFDM signals and a combiner block, which equalizes the signal and separates out the coded users. The receiver first removes the cyclic prefix and then performs an FFT operation of the received symbols and brings them back to the frequency domain. Then de-interleaving operation is performed. Then dispreading and decoding of the chips in frequency domain are performed. The block diagram of the MC-CDMA receiver is shown in Fig. 5.

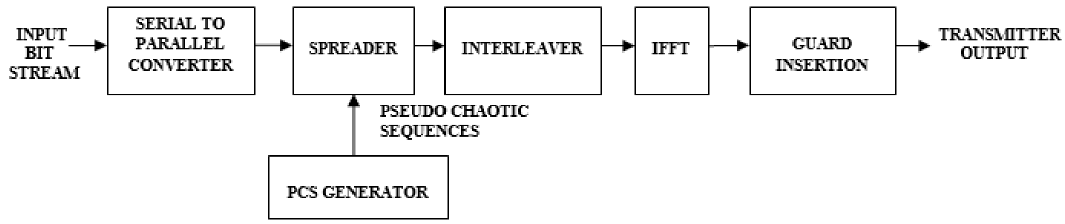

Fig. 4. Block Diagram of MC-CDMA Transmitter Using PCS Generator

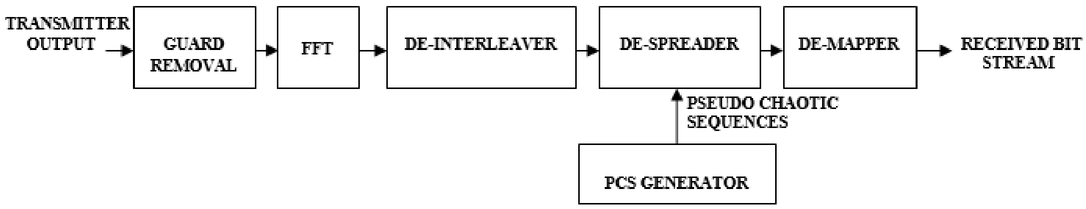

Fig. 5. Block Diagram of MC-CDMA Receiver Using PCS Generator

IV. PERFORMANCE OF THE PROPOSED SCHEME AND EXPERIMENTAL RESULTS

In this paper the prototype was designed and implemented for a spreading sequence of length 32 bits because of hardware limitations. For practical applications the spreading sequence length can be increased to 1024 bits. Hence the performance of the system can be enhanced by increasing the length of the spreading sequence.

Hence increasing the spreading sequence length from 32 bits to 1024 bits naturally achieves better performance. The BER performance of the PCS system will compare with the PN system. MC-CDMA system using chaotic sequences as spreading codes significantly outperforms the conventional system. It offers very high security than traditional system. Then later on the autocorrelation properties and cross correlation properties of PCS will compared with the m-sequences.

The system is implemented using FPGA. First Verilog HDL codes were written for MC-CDMA transmitter and receiver and then simulated the circuit design on MODELSIM and QUARTUS II simulation software tool. Subsequently, MATLAB was used to analyse the BER performance of the implemented system. The MATLAB simulation tests were performed on communication tool box and Simulink programming. The simulation of variable rate transmission with BPSK modulation without forward error correcting code has been carried out in MATLAB. For multipath frequency selective Channel, we have assumed 4-fold correlated Rayleigh fading [9], [10] channel. Generation of correlated fades, for the purpose of simulation, has been discussed in [8]. First we will discuss the results assuming perfect phase synchronization and then the effect of phase jitters is evaluated.

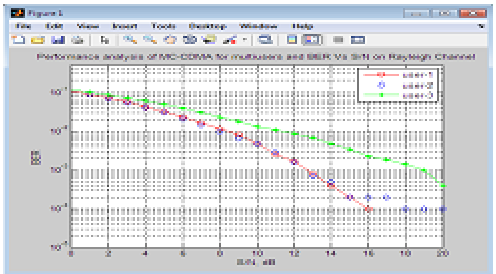

Fig.6. BER Performance Of MC-CDMA System

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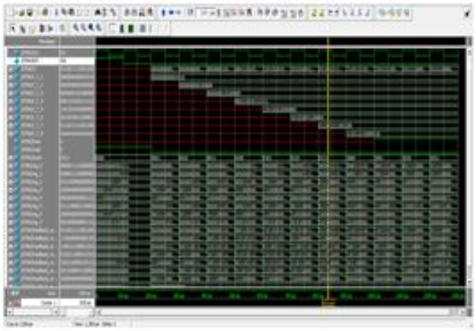

Fig. 7. Simulated Output of PCS Generator

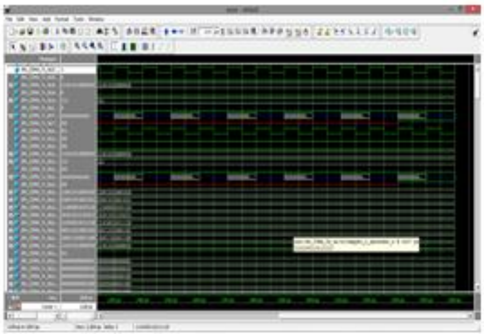

Fig. 8. Simulated Output of MC-CDMA Transmitter

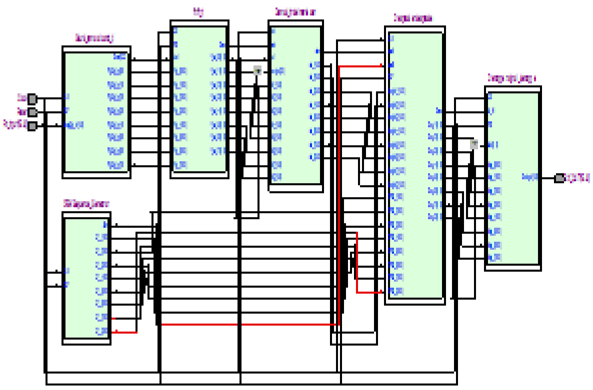

Fig. 10. RTL View of MC-CDMA Transmitter.

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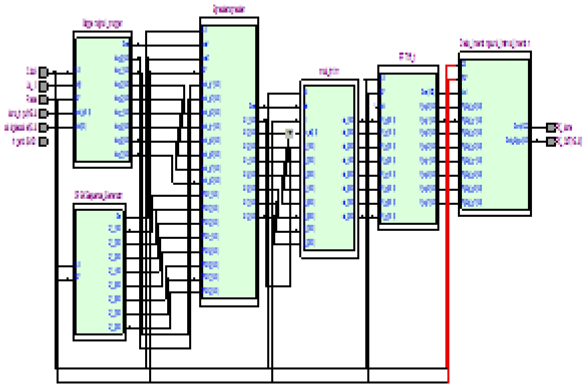

Fig. 11. RTL View of MC-CDMA Receiver

V. CONCLUSION

The PCS generator discussed in this paper is based on the model discussed in [11]. The initial conditions of the PCS sequence generators can be randomly selected to produce pseudo-chaotic sequence with good correlation properties upon exhaustive comparison to be distinct sequences rather than phases of the same sequence. In this paper, we proposed multicarrier code division multiple access (MC-CDMA) multiuser transceiver using pseudo chaotic sequence generator that achieves a data rate of minimum 1Gbps equivalent to the 4G standard of IEEE. The proposed method with chaotic spreading codes performs effectively by reducing the MAI in MC-CDMA system. The application of chaotic codes performs better in the system than the classical codes in terms of exterminating MAI. When the system is occupied by large number of users, it is observed that by initializing chaotic spreading code, the utility performance is improved compared to the traditional system. The family of pseudo-chaotic PN sequences proved good correlation properties than conventional m-sequences and hence it can be useful for MC-CDMA. Tests will have shown that simply using random selections of initial conditions can provide pseudo-chaotic PN sequences that are relatively long with good correlation properties. This flexibility provides an additional level of security on top of the inherent low-probability of intercept characteristics of PN sequences due to the difficulty of identify the underlying structure. Therefore the number of implementation possibilities is very high due to initial condition programmability, can be made software controlled and this new system of sequences is inherently more difficult to detect. Finally we synthesized successfully and verified scheme with MODELSIM and QUARTUS II EDA tool.

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