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Design and Optimization of Low Power VLSI Circuits for Leakage Power Reduction Using GSA

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Abstract: *The Arithmetic Logic Unit (ALU) being a central unit for mathematical and computational tasks, its design is critical, in terms of Low Power and High Performance. The major portion of the total power consumption is Leakage power, as process technologies progress from one generation to next generations. There are several methods to reduce leakage power, both in Active and Standby mode. One such technique is Input Vector Control (IVC), which is independent of Process technology and based on Transistor stacking effect, reduces the leakage power in Standby mode. Gravitational Search Algorithm (GSA) is a search algorithm which locates the Minimum Leakage Vector (MLV). In this research, 16-bit and 32-bit ALU are designed with PSPICE tool with several test circuits. The coding is executed with Verilog HDL and these coded designs are synthesized and simulated using Xilinx vivado platform. In the comparison study, GSA proved its superiority over Genetic Algorithm in terms of number of iterations and low leakage power.*

Keywords: *Arithmetic and Logical Unit (ALU), Genetic Algorithm (GA), Gravitational Search Algorithm (GSA), Input Vector Control (IVC), Minimum Leakage Vector (MLV)*

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I. Introduction

Analog and mixed signal integrated circuits play a significant role in designing integrated circuits. It comprises of both analog and digital signals in a single semiconductor die. It is commonly used as a communication interface among the digital and real world signals. The designing of analog circuitry part is found to be critical because of the immense complexity and size perception[1]. Furthermore, the miniaturization in the circuit design provides special emphasis to the production of the system on chip (SOC) and is dominated by the effects of nanoscale elements. Due to the effect of ever-growing demand and the advancements in terms of miniaturization, the designers are facing scaling issues and also there is an exponential growth in terms of complexity, which influences on the productivity and performance of the analog and mixed mode systems[2]. Furthermore, minimizing the energy consumption rate in modern processors can extend the lifespan of the semiconductor devices and battery, especially in portable devices.

The advancement in VLSI technologies has made the digital and analog circuits to scale down into nanometer range, which results in exponential increase of sub threshold leakage current, threshold voltage and power consumption. The concern in terms of power consumption has increased rapidly due to the design complexity and the structure density[3]. Hence, there exists a requirement of an accurate power modeling technique to address the issues of nanometer processing technologies. Different modeling techniques have been discussed in this paper and the process of Input Vector Control (IVC) is found to be a better alternative in achieving the low power consumption. The design of IVC is based on the effect of transistor stacking and it is highly preferred because of its nature of independency over other technological parameters[4]. The deployment of IVC technique shows that the circuit to be in a minimal leakage state with no performance overhead. Furthermore, the energy consumption can also be reduced by defining a Minimum Leakage Vector (MLV), which represents the minimal leakage state amongst the set of test inputs[5]. It can be forced into the test circuit by using multiplexers to reduce the power consumption at idle state. The leakage power can also be reduced through the selection of input vector and the combination of test circuit is measured through look up table. Several machine learning optimization algorithms have been deployed to reduce the leakage power and found to be effective in solving various problems related to size and power consumption.

The components required for designing analog circuits comprise with oscillators, filters, amplifiers, power sources and arithmetic and logical circuits[6]. Applying effective optimization technique to calculate their design parameters is observed to be a better possible method for reducing power consumption in the system. In

this research, a novel technique comprising gravitational search algorithm is developed to optimize the power of the circuit. Arithmetic Logic Unit (ALU) is designed for 16 bit to evaluate the performance of the system. Furthermore, comparison study of other techniques with GSA elevates the design of ALU in terms of Leakage Power and the time to reach the optimal solution. This research paper is divided into four sections. First section comprises of Introduction which provides an overview of the research topic. Second section describes the proposed method along with the developed technique and the description of the simulation tool is done in the third section. The fourth section consists of results and discussions obtained from the proposed method followed by Conclusion.

II. Research Methodology

The In this research, Arithmetic and Logical Block is designed using PSPICE platform. ALU acts as a logical and control unit in which several mathematical operations are performed to achieve the specific task. 16-bit and 32-bit are considered in this research for designing the circuit, and, the performance is evaluated through the variation of input vectors. The advantage of gravitational search algorithm is forcing the test circuit into the designed ALU to obtain optimal solution and to calculate the leakage power. The detailed description of the proposed methodology will be explained in the following stages.

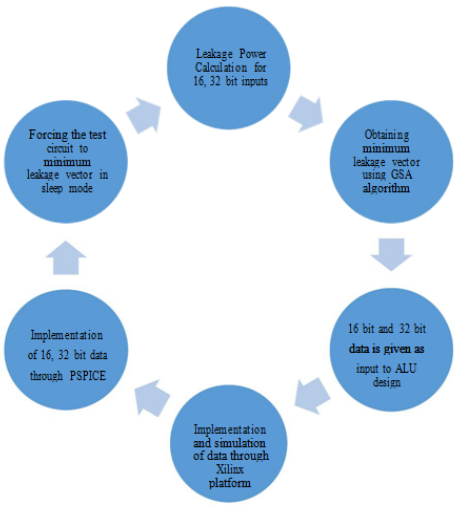

Fig. 1: Block diagram of the proposed Research

The block diagram of the overall research is shown in Fig. 1. Initially, two input NAND gate is designed using PSPICE software and the same is used as a universal gate to develop other circuits. In this research, 16-bit and 32-bit ALU is designed using the combination of NAND gate. The leakage power of the two input NAND gate for all the combinations are computed to calculate the MLV for different operations and to obtain the minimum leakage power. Further, the values obtained will be given as reference to the designed 16 bit ALU and to find the optimal minimum leakage vector from the randomly generated input vectors in Table 2. The selection process along with test vectors and block diagram will be explained in the following stages.

Analog and mixed signal integrated circuits play a significant role in designing integrated circuits. It comprises of both analog and digital signals in a single semiconductor die. It is commonly used as a communication interface among the digital and real world signals. The designing of analog circuitry part is found to be critical because of the immense complexity and size perception. Furthermore, the miniaturization in the circuit design provides special emphasis to the production of the system on chip (SOC) and is dominated by the effects of nanoscale elements. Due to the effect of ever-growing demand and the advancements in terms of miniaturization, the designers are facing scaling issues and also there is an exponential growth in terms of complexity, which influences on the productivity and performance of the analog and mixed mode systems. Furthermore, minimizing the energy consumption rate in modern processors can extend the lifespan of the semiconductor devices and battery, especially in portable devices.

The advancement in VLSI technologies has made the digital and analog circuits to scale down into nanometer range, which results in exponential increase of sub threshold leakage current, threshold voltage and power consumption. The concern in terms of power consumption has increased rapidly due to the design complexity and the structure density. Hence, there exists a requirement of an accurate power modeling technique to address the issues of nanometer processing technologies. Different modeling techniques have been discussed in this paper and the process of Input Vector Control (IVC) is found to be a better alternative in

achieving the low power consumption. The design of IVC is based on the effect of transistor stacking and it is highly preferred because of its nature of independency over other technological parameters. The deployment of IVC technique shows that the circuit to be in a minimal leakage state with no performance overhead. Furthermore, the energy consumption can also be reduced by defining a Minimum Leakage Vector (MLV), which represents the minimal leakage state amongst the set of test inputs. It can be forced into the test circuit by using multiplexers to reduce the power consumption at idle state. The leakage power can also be reduced through the selection of input vector and the combination of test circuit is measured through look up table. Several machine learning optimization algorithms have been deployed to reduce the leakage power and found to be effective in solving various problems related to size and power consumption.

The components required for designing analog circuits comprise with oscillators, filters, amplifiers, power sources and arithmetic and logical circuits. Applying effective optimization technique to calculate their design parameters is observed to be a better possible method for reducing power consumption in the system. In this research, a novel technique comprising gravitational search algorithm is developed to optimize the power of the circuit. Arithmetic Logic Unit (ALU) is designed for 16 bit to evaluate the performance of the system. Furthermore, comparison study of other techniques with GSA elevates the design of ALU in terms of Leakage Power and the time to reach the optimal solution. This research paper is divided into four sections. First section comprises of Introduction which provides an overview of the research topic. Second section describes the proposed method along with the developed technique and the description of the simulation tool is done in the third section. The fourth section consists of results and discussions obtained from the proposed method followed by Conclusion.

2.1. Arithmetic and Logical Unit (ALU)

An Arithmetic and Logic Unit (ALU) is defined as digital circuit used to accomplish numerous arithmetic, logical and bitwise operations in microprocessor and microcontroller. The advancement in the field of digital circuits has led the operation of number of tasks simultaneously through a pipelined process and it results in high computational time and power consumption. By designing an effective ALU circuit with thorough monitoring on performance, operational speed and input vectors namely feed operands and control codes can enhance the performance of ALU. In this research, 16 bit and 32 bit ALU are designed to perform numerous operations in terms of logical and arithmetic operations namely OR, AND, NOT, XOR, XNOR, NAND, Addition, Subtraction, Increment and Decrement.

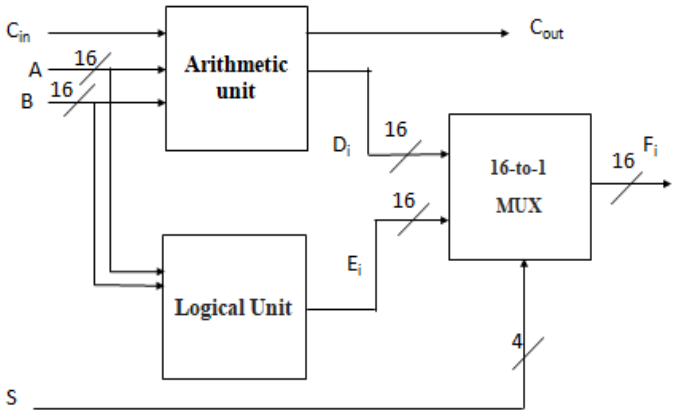

Fig. 2: Architecture of ALU

Fig.2 shows the block diagram and generic structure of ALU. The arithmetic unit is generally used for performing arithmetic operations and the other operations, such as processing and performance operations that eleven different functions are considered for analysis and the ALU is designed by considering the same criteria. The eleven different functions of 16-bit ALU are shown in Table 1. A 32-bit additive operation is also performed with hexadecimal number is tabulated with 32-bit ALU with minimum leakage power (MLP).

A and B define the input dataset and C_{in} is the input carry signal. Control signal is of 4 bit size and is fed into the 16 bit multiplexer to select the particular operation. Output obtained from the multiplexer is of 16 bit size along with C_{out} of single bit.

As shown in Table 1, the mathematical operations are obtained by designing the control signals S_0, S_1, S_2,S_3 through programming. In digital circuits, generally the bits will be defined in the form of logic "1" (High) and logic "0" (Low) and desired output can be achieved by varying the inputs along with control signals. The leakage power consumption is calculated for each input vector combination of Test circuit. The Minimum

Leakage Vectors (MLV) of various test circuits are located by gravitational search algorithm. The IVC technique forces the test circuits of other input vectors into the MLV in sleep mode to reduce the leakage power consumption.

Table 1: Operations of ALU.

OPCODE				
S_0	S_1	S_2	S_3	Operation
0	0	0	1	AND
0	0	1	0	NAND
0	0	1	1	OR
0	1	0	0	NOT
0	1	0	1	NOR
0	1	1	0	XOR
0	1	1	1	XNOR
1	0	0	0	ADD
1	0	0	1	SUB
1	0	1	0	INCREMENT
1	0	1	1	DECREMENT
Default				Default Output = 0

The arithmetic and logical operations are performed by selecting the control signals.

2.2. Genetic Algorithm (GA)[7,8,9]

Genetic algorithms are a particular class of evolutionary algorithms (EA) that follows the process of natural selection to generate high-quality solutions by relying on bio-inspired operations such as mutation, selection and cross-over (also called recombination).

The evaluation usually starts from a population of randomly generated individuals and happens in generations. In each generation, the fitness of every individual (higher the fitness, the higher the chance of being selected) is selected from the current population and modified (recombined and possibly mutated) to form a new generation. The new generation is then used in the next iteration of the algorithm. The algorithm terminates its iterations either at a satisfactory solution (satisfactory fitness level) or at final generation.

The pseudo code for genetic algorithm is given below.

```
Genetic algorithm_mlv()
{
Population_size = n;
Chromosome length = Number of primary inputs Generation = 1;
Initialize a population of chromosomes
do
{
Evaluate fitness of each chromosome in the population Select parent chromosomes
Generate off springs using cross over and mutation
}
While(generation ++ < No. of generations)
}
```

The GA is used in this paper to find Minimum Leakage Vector (MLV) by using Input vector control (IVC) technique[10]. For test circuits, leakage power is calculated for each input combination and compared with the Low leakage state. That minimum leakage vector is enforced to the other combinations in the circuit into MLV to reduce the total leakage power, when the system is in standby mode.

2.3. Gravitational Search Algorithm (GSA)

The gravitational search algorithm is the advanced optimization algorithm designed on the basis of law of gravity and population based stochastic search technique. This algorithm is found to be more accurate in solving the nonlinear problems. The law of gravity is on the basis of Newton's law, which states "the gravitational force amongst two particles is proportional to the product of their masses and inversely proportional to the square of the distance between them". In the developed algorithm, the input vectors are considered as objects and their performance is analyzed in terms of masses. Individual particle is correlated with specifications namely, inertial mass, particle position, passive and active gravitational mass. The particle position determines the optimal solution to the problem whereas fitness function is considered to evaluate the inertial and gravitational masses. Every individual population algorithm comprises of two capabilities namely exploitation and exploration. The capability of exploration is used at the beginning to avoid minimizing the local optimization problem and later exploitation. The global best function reduces linearly with respect to the time and the agent with heavy mass obtained at the final iteration represents the final optimal solution.

In this paper, the input vectors are considered as objects and GSA is applied to reduce the leakage power of the elements. The optimization procedure is based on the number of iterations to locate the sleep mode elements in the VLSI circuit. According to GSA, the force acting from j^{th} mass on i^{th} mass at any instant of time t is:

$F_{ij}^{d}(t) \alpha \frac{Mi(t)*Mj(t)}{Rij}[p_j^{d}(t) - p_i^{d}(t)]$

where, the position of particle i is p_i

$p_i = (p_i^{1}, p_i^{2}, p_i^{3}, \ldots\ldots, p_i^{d}, \ldots\ldots, p_i^{n})$

R_{ij} = distance between two masses

Evaluate the fitness function for all objects in each iteration and also compute the best and worst fitness at each iteration defined below.

Best (t) = $\min_{i\in 1\ldots M} f_i t_i$ (t)

Worst (t) = $\max_{i\in 1\ldots M} f_i t_i$ (t)

where $f_i t_i$ (t) represents the fitness value of the object i at iteration t.

Mass of each object is calculated as below:

$$M(t) = \frac{x_i(t)}{\sum_{k-1}^{N} x_i(t)}$$

where $x_i(t) = \frac{\text{fitness (t) - worst (t)}}{\text{Best (t) - worst (t)}}$

Update the value of particle velocity and position given by following equations

Velocity is given by,

$V_i^d(t+1) = \text{rand} * V_i^d(t) + a_i^d(t)$

Position is given by,

$p_i^d(t+1) = p_j^d(t) + V_i^d(t+1)$

Repeat the process until best optimal function and stopping criteria is reached.

The gravitational search algorithm is programmed using Verilog HDL and implemented through Xilinx platform.

III. Verilog Programming

Verilog is a Hardware Description programming Language (HDL) used for defining and designing several digital systems such as microprocessor and flip-flops.

It usually supports various designing levels of abstraction namely behavioral level, RTL level and the gate level. The major advantage is that the behavior of the system design can be easily studied, modeled and verified through the synthesis tool before it is translated into the real time hardware. Furthermore, the descriptive behavior helps to easily analyze the concurrent system compared to other programming languages. In this research, Verilog language is defined to program the 16 bit and 32 bit ALU and it is synthesized using Xilinx vivado platform to calculate the leakage power.

3.1. PSPICE simulation tool

PSPICE is a simulation programming based integrated circuit framework used to evaluate the circuit design through simulation model and debugging. Prediction of the results is normally done to analyze the effectiveness of the design and its behavior in real time scenario. From the literature, it is observed that more amounts of complexity and time are required for prediction and analysis of designed ALU. In this research, a PSPICE model for 16 bit and 32 bit is designed to overcome the above mentioned limitations and the designed system is evaluated in terms of power consumption.

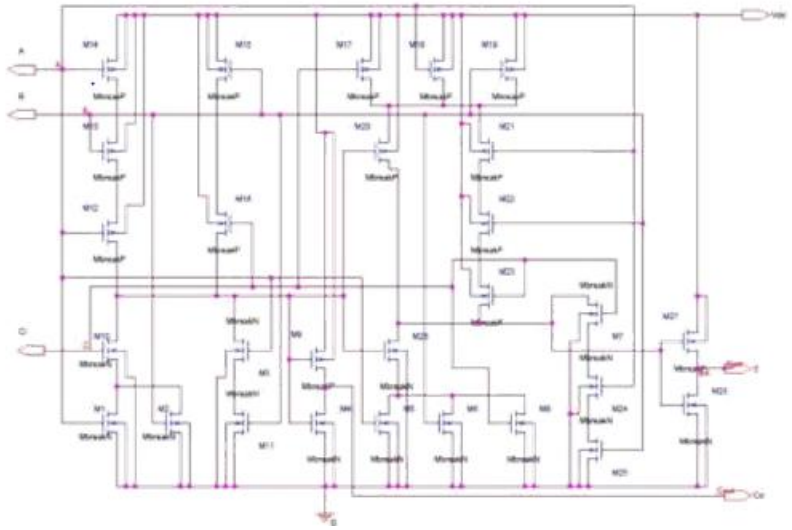

Fig. 3: Schematic structure of ALU transistor model

Fig. 3 shows the CMOS schematic structure of ALU model. The circuit is designed using PSPICE platform and the simulation is carried out for calculating the power consumption rate. Input data considered and the result obtained will be explained in the following section. Further, the model is designed as a sub circuit and the same is connected into number of parallel circuits to obtain 16bit and 32 bit model circuit

IV. Results and Discussion

In this research, ALU circuit is designed using Verilog programming language for 16 bit and 32 bit inputs. The 32-bit input vector is processed through gravitational search algorithm to obtain Input Vector Control and to find the Minimum Leakage Vector. The result obtained from the study is tabulated as shown in Table 2.

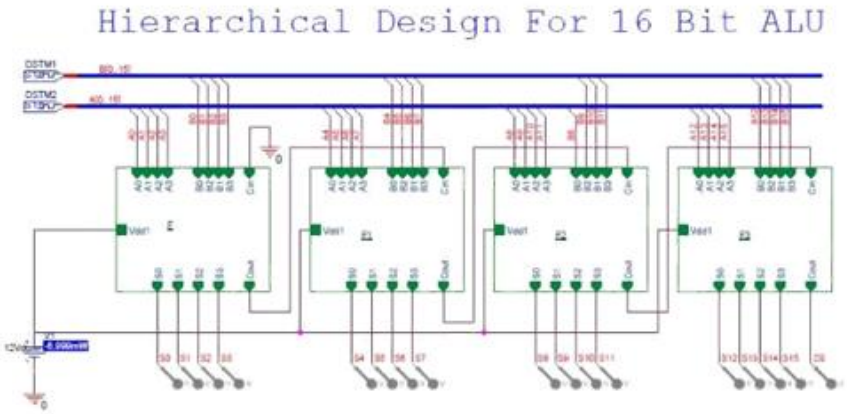

Fig. 4: Schematic structure of 16 bit ALU

The input 16 bit data is processed through the developed ALU circuit model as shown in Table 1 and Fig. 2. Select line, which is given to the multiplexer, selects the operation to be performed on the basis of user requirement and the analysis is done on the same. The evaluation results captured through the proposed model are as follows:

Table 2: Minimum leakage power (MLP) with GSA for 16-bit ALU particular function

Test Circuit	Input Vector in Binary Format	MLP with GSA (pW)	Maximum number of iterations
AND	A= 0110111001000110 B= 0110111001000110	170.16	21
OR	A= 0000000000000000 B= 0000000000000000	172.64	18
Adder	A= 0000000000000000 B= 0000000000000000	871.015	22
NAND	A= 0000000000000000 B= 0000000000000000	2.48	17

Table 2 depicts the results obtained from the 16 bit ALU. Gravitational Search Algorithm is applied for the individual input vector set for the particular operation and minimum leakage power is calculated. From the above table, it is observed that minimum leakage power of 2.48pW is achieved for NAND test circuit with an input vector selection of A=0000000000000000 and B=0000000000000000. So the A and B input vector set stated above is defined as MLV. Furthermore, the number of iterations considered to obtain minimum leakage power for NAND gate is 17.

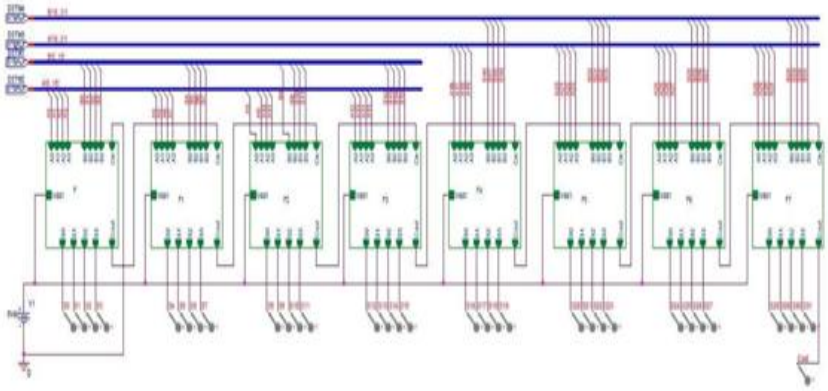

Fig. 5: Schematic structure of 32 bit ALU

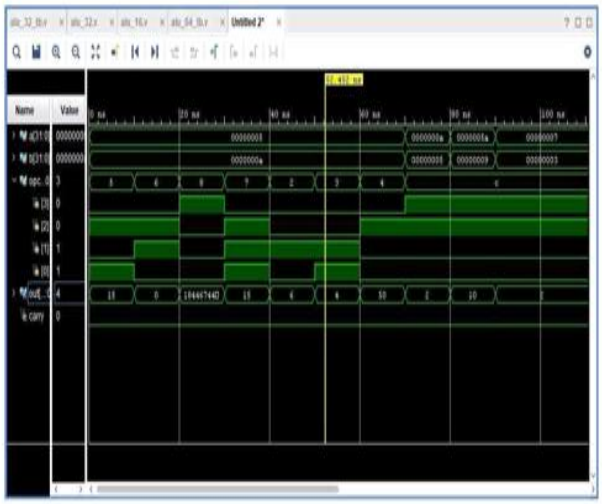

Fig. 6: The output obtained from Xilinx platform

Verilog code for 16 and 32 bit ALU design is programmed and executed through Xilinx vivado platform. The results obtained from the analysis are shown in Fig. 6. Further, PSPICE tool is used to calculate the power and the result obtained through the experimentation are as follows:

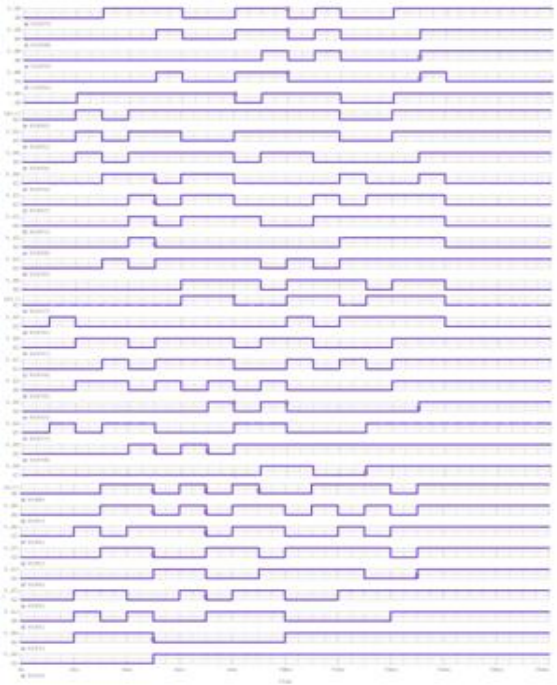

Fig. 7: 32 bit Input "A" data considered for the analysis

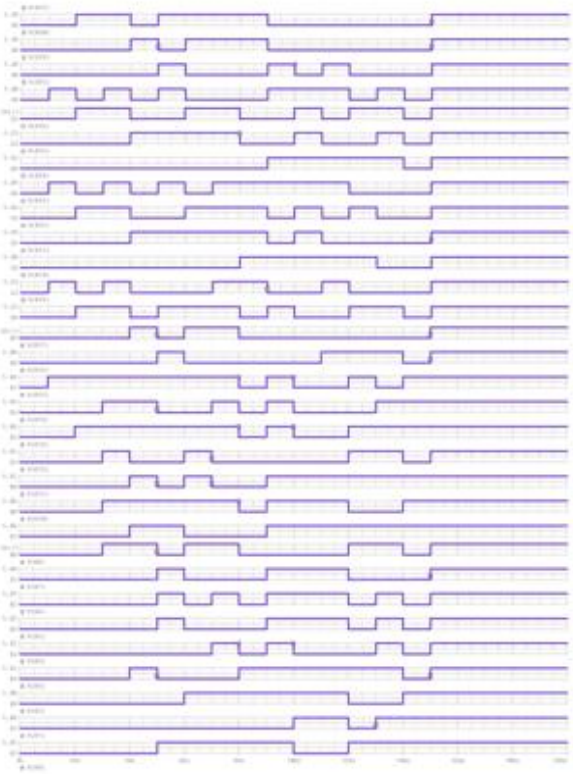

Fig. 8: 32 bit Input "B" data considered for the analysis

Fig. 9: Output data obtained from the analysis

Table 3: MLP vector calculated with respect to time

Time	A Vector	B Vector
0 ms	0x00000000	0x00000000
1 ms	0x00001111	0x00018000
2 ms	0x00005222	0x720500F0
3ms	0x00AF3333	0x55971111
4ms	0x10F74444	0x67B00FF1
5ms	0x8765A55A	0x8A0710FB
6 ms	0xA0BD6666	0x9BA377B0
7ms	0xAAA77767	0xA40F77B0
8ms	0xB0001F07	0xB7B0346B
9ms	0xBF772999	0xBB7D00FF
10ms	0x77700FF0	0xCC63F0F0
11ms	0x77709999	0xCDA06677
12ms	0x90DDAAA0	0xDEA2BD00
13ms	0xDEDEA0F0	0xD5F0DE00
14ms	0xE0770000	0xF277FE71
15ms	0xFFFFFFFF	0xFFFFFFFF

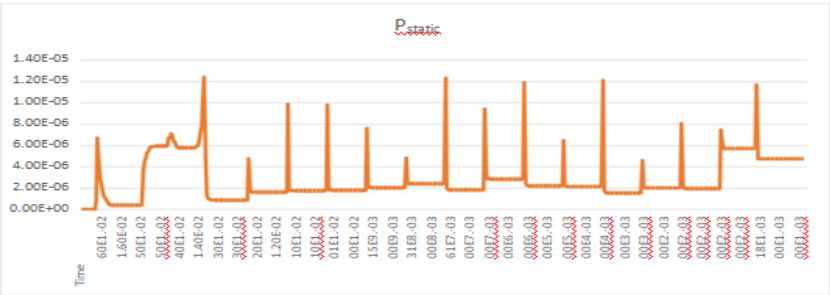

Fig. 10: Static power plot obtained through PSPICE

The 32 bit input data 'A' and 'B' are implemented using PSPICE platform as shown in Fig. 7 and Fig. 8. And the result obtained through the analysis is shown in Fig. 9. Furthermore, the evaluation is carried out through PSPICE platform and the static power obtained at different timings at different input vectors is as shown in Fig. 10. The unpredicted behavior of the static power variations is observed from the Fig.10.

Table 4: Minimum leakage power with GSA in terms of hexadecimal value

Test Circuit	Input Vector	MLP with GSA (□ W)
ADDITION	A=0x00001111 B=0x00018000	0.5

Table 4 depicts the results obtained from the 32-bit ALU. Gravitational Search Algorithm is applied for the individual input vector set and minimum leakage power is calculated. From the above table, it is observed that minimum leakage power of 0.5 μW is achieved for ADDITION test circuit with an initial input vector selection of A=00001111 and B=00018000. So the A and B input vector stated above is defined as MLV. The MLV is achieved at 50th iteration.

V. Comparative Analysis

Table 5: Results obtained from GSA algorithm for different test circuits

Test Circuit	Population Size	MLV	No. of iterations	Leakage Power (pW)
6 input circuit	8	0	1	21.58
	20		1	
	30		1	
8 Input Circuit	8	0	15	21.735
	20		7	
	30		2	
10 Input circuit [Modified Circuit]	8	0	16	48.58
	20		11	
	30		7	
C17 input Circuit	8	101	1	28.56
	20		1	
	30		1	

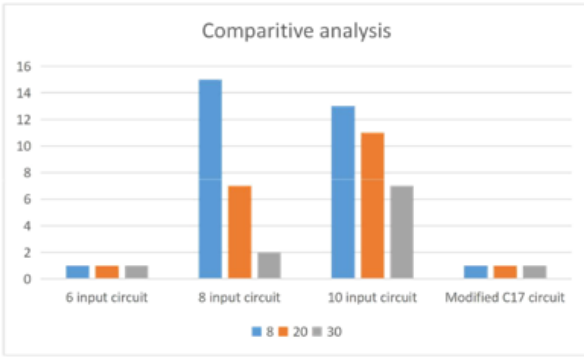

Fig. 11: Comparative analysis in terms of population size and number of iterations of GSA

Table 6: Results obtained from GSA algorithm for different test circuits

Test Circuit	No. of Population	Number of Iterations	
		GA	GSA
C17 circuit	8	1	1
6 input circuit	8	15	1
8 input circuit	8	34	10
10 input circuit	8	96	13

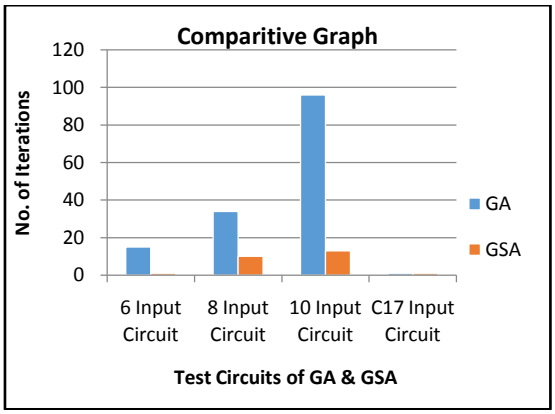

Fig. 12: Comparative Graph in terms of number of iterations of GA & GSA

Fig. 11 shows the comparative analysis with respect to population size and number of iterations of GSA. Fig. 12 shows the comparative graph of the proposed GSA algorithm with genetic algorithm on the basis of number of iterations. The input test is conducted for all the possible test cases (4-bit, 6-bit, 10-bit, NAND gate and C_{17} bench mark circuits) and G_{best} for the final optimal solution for 10 input NAND gate circuit with population size of 8 is observed at the MLV of "0000000000". From the comparative analysis, it is seen that proposed GSA algorithm converges at 13th iterations, whereas Genetic Algorithm converges late at 96th iteration. So, GSA takes less runtime to reach its minimum leakage vector when compared to Genetic Algorithm. The G_{best} value with minimum leakage power is processed through PSPICE simulation platform for calculating leakage power.

VI. Conclusion

The arithmetic and logical unit is a core component of digital circuit design and selecting an appropriate design strategy can reduce the power consumption. In this research, a heuristic approach comprising gravitational search algorithm is proposed to reduce the leakage power in ALU circuits. 16 and 32 bit ALU input test combinations are considered during the design process and programmed using verilog coding language to obtain optimal MLV. From the results obtained, it is concluded that GSA algorithm provides better optimal test function results with minimum leakage power and less number of iterations. Finally, a comparative analysis is conducted to prove the effectiveness of the design and observed that superior results are achieved compared to Genetic Algorithm. In future, the developed technique can be extended to 64 bit input vector set to obtain optimal MLV.

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