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Implementation of Low Power Voltage Level Shifter Using GALEOR Technique for Subthreshold Operation

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Abstract: *The Voltage Level Shifter is widely used in various integrated circuits these days such as in analogue computers, simulation systems and in many electronic applications as filtering, buffering and comparison of signal levels. Basically voltage level shifter converts low levels of input voltages in to high output voltage levels. In this paper various types of voltage level shifters are discussed mainly focus on the power efficient voltage level shifter, before this architecture explain the architecture of high speed voltage level shifter. To reduce the power consumption implement voltage level shifter with GALEOR technique. GALEOR (Gated LEakage TransistOR), reduces the leakage current flowing through the circuits. new static power reduction technique named GALEOR, which reduces the leakage current flowing through the circuit by creating a stack effect using high threshold voltage transistors in between the pull-up and pull-down networks. GALEOR technique achieves on average 25% savings in leakage power. GALEOR Circuit is connected across the input and output terminals. The improved architecture power consumption is 40 percentage less than the high speed voltage level shifter with auxiliary circuit.. In this dual supply architectures are used. Those are low supply voltage VDD_L=0.4V and high supply voltage VDD_H=1V, Input frequency is 1MHz. The circuits presented in this work are analysed by using the backend tool CADENCE.*

Keywords*: level shifter, subthreshold, analog blocks, latch state, auxiliary circuit.*

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I. Introduction

A voltage level shifter has a supply line receiving a supply voltage that varies between a first operating value in a first operating condition and a second high operating value, in a second operating condition [1], [2]. A latch stage is connected to an output branch and to a selection circuit, which receives a selection signal that controls switching of the latch stage. In digital circuits dynamic and short-circuit power consumption is reduced by lowering the value of the power supply voltage .It can be also reduced by increased supply voltage, because of this propagation delay of the circuits was increased. On the other hand minimized headroom in analog circuits decreases signal swings due to this increases the sensitivity to noise. Hence, in moderate-speed mixed signal circuits or in digital circuits where different parts operate at different speeds, dual-supply architectures are introduced in which a low voltage (i.e., *V*DDL) is supplied for the blocks which are in noncritical paths while analog and the high-speed digital blocks are driven by a high supply voltage (i.e., *V*DDH) [3].In a system with dual supply voltages, level-shifting circuits are needed to convert the lower voltage levels into the higher ones to provide correct voltage levels for the succeeding digital blocks. In this manner to alleviate the degradation of the entire performance of the circuit, the required level shifters must be implemented with minimum propagation delay, power consumption, and silicon area.

The remaining of this paper is organized as follows. In Section II, efficient voltage level shifter with auxiliary circuit is reviewed. The proposed circuit is introduced in Section III. Section IV presents the simulation results of the designed circuit verifying the efficiency of the proposed structure. Finally, this brief is concluded in Section V.

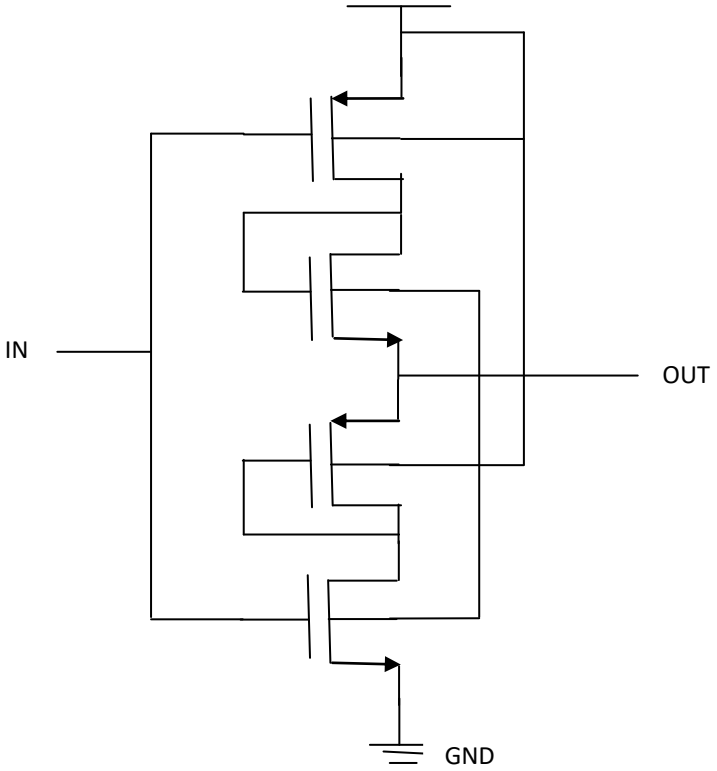

Fig.1. GALEOR Technique

When the Device density is high and threshold voltages of the transistors is low then automatically increase the leakage current dissipation. The proposed static power reduction technique, GALEOR (GAted LEakage TransistOR) is use in high speed power efficient voltage level shifter it results in reduces the leakage currents in the circuits. This leakage power technique is applied to existing level shifter , in this circuitry one of the gated leakage transistors is connected bellow the pull-up transistor and another gated leakage transistor is connected above the pull-down transistor of the existing circuit such that gates of the gated leakage transistors are connected to their drain regions sequentially. GALEOR technique was first tested on standard cell gates and memory elements the researches shows by use of control logic to switch Area overhead is minimised. Because of the reduced output voltage swing Performance overhead is increased.

II. Efficient Voltage Level Shifter With Auxiliary Circuit

High speed voltage level shifter gives the better output response and better delay, but this circuit consumes more power. To overcome this drawback designed the efficient voltage level shifter with auxiliary circuit. This circuit have an auxiliary circuit with that of efficient voltage level shifter[4]. The main purpose of the auxiliary circuit is it turns on only in the high to low transition simultaneously QC is charged to the value higher than the VDDL.

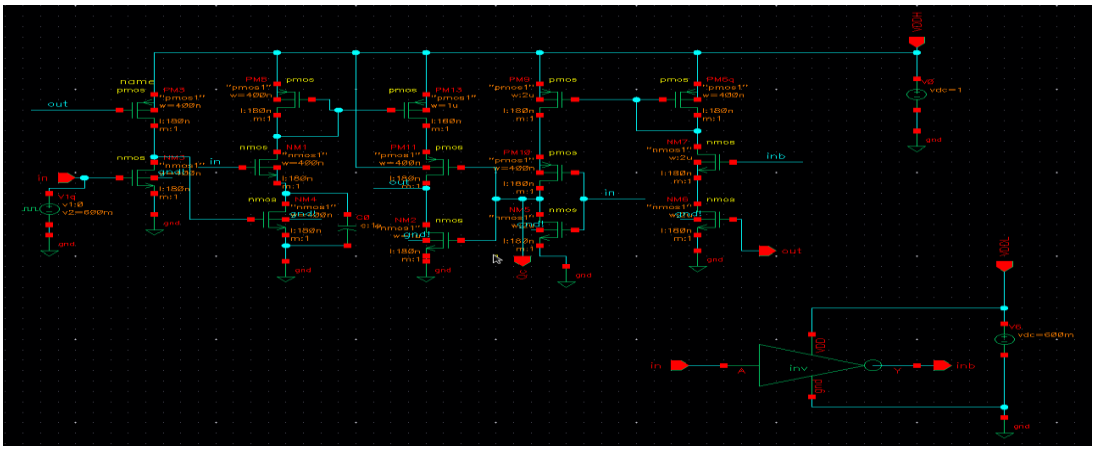

Fig.2. Efficient Voltage Level Shifter with Auxiliary Circuit .

The operation circuit is as follows. When IN value from "High" to "Low" in this time of action OUT is related to the previous input logic level so MN6, MN7, and MP6 are going to be saturated and MN5 is cut off. Therefore, a transition current flows through MN6,MN7, MP6, this circuit have mirror structure at the MP6 then same amount of current mirrored at MP7 (i.e., IP7) at particular time MP7 is pulling up the node *QC*. It shows that MP4 I in cut off and MP2 is turn on with a value higher than the VDDL. After this OUT voltage is decreased completely simultaneously MN6 turned off then current flows through the MN6, MN7, and MP6 are zero[5]. The whole operation states that auxiliary circuit is turns off in the low to high transition. It minimizes the power consumption only when the input range is from in high to low.

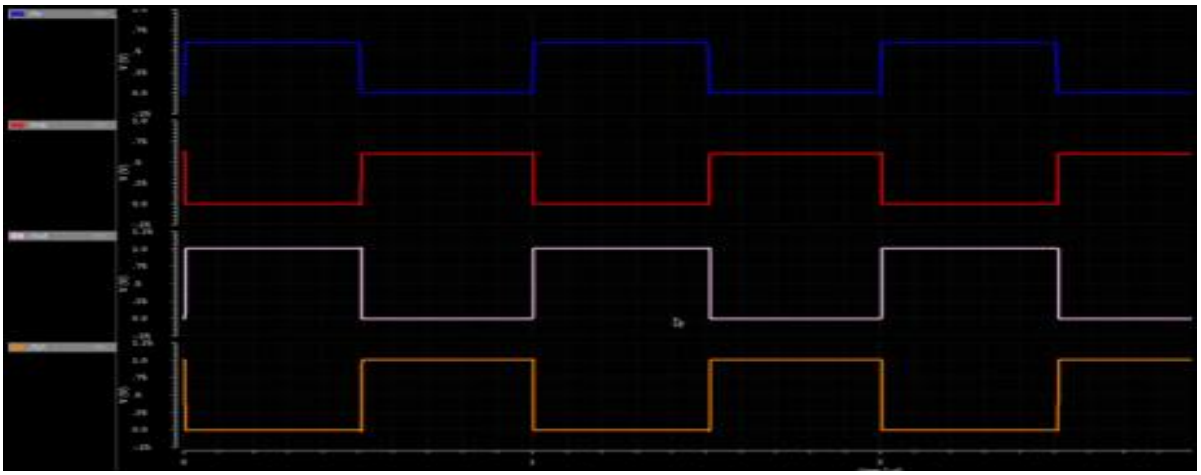

Fig.3. Simulation Results of Efficient Voltage Level Shifter with Auxiliary Circuit

Fig. 3. Shows the simulation results of efficient voltage level shifter when applied input IN is high, INB is low then output voltage is low and Qc is high. It shows the voltage levels in this particular circuit it drastically lowering the power consumption, So in order to reduce the power consumption in low to high a circuit was designed that is Low Power Voltage Level Shifter With GALEOR Technique For Subthreshold Operation .

III. Low Power Voltage Level Shifter With Galeor Technique For Subthreshold Operation

High performance and computational capability in the current generation processors are made possible by small feature sizes and high device density. To maintain the current drive strength and control the power dissipation in these processors, simultaneous scaling down of supply and threshold voltages is performed[6]. As the name implies that the circuit operated in subthreshold region, in this region also low power voltage level shifter effectively converts low level of input voltage levels on to high output voltage levels voltage with the help of GALEOR (Gated LEakage TransistOR),Circuit. In this design of implementation have two high V_t gated leakage transistors NMOS and PMOS transistors, these are placed between the middle of pull-up transistor and pull-down transistor. Because of this arrangement stack effect is induced because of this stack effect leakage current reduced and the resistance of the leakage path is increased. When the resistance of the leakage path is increases leakage currents in the circuit was reduced. It means the power consumption of the entire circuit was reduced. The performance of the circuit depends on the power consumption so the performance of the circuit was increased.

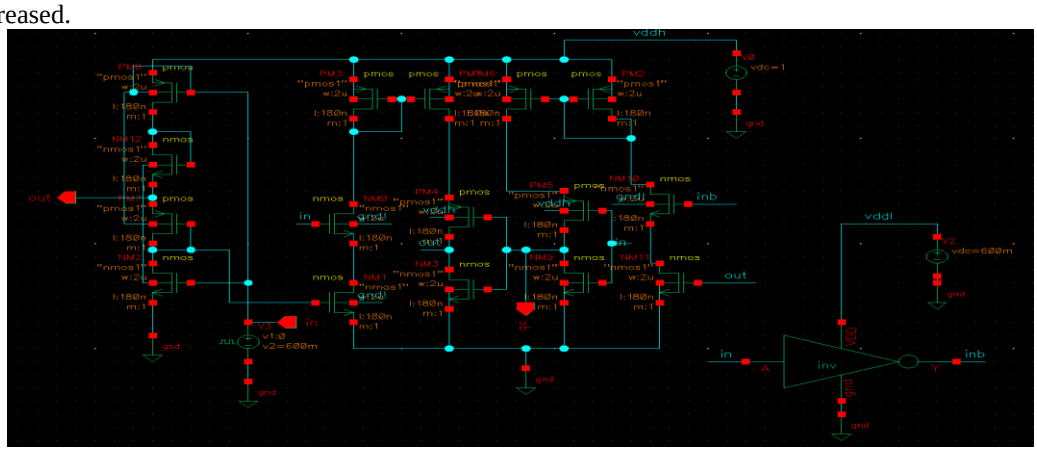

Fig.4. Low Power Voltage Level Shifter with GALEOR Technique

Input pattern of the each gate shows some effects on subthreshold voltages as well as leakage currents. The leakage current of transistor in a stack is a function of number of transistors and input patterns. The entire circuit was constructed in cadence virtuoso[4]. Operation of this circuit is same as the before circuit i.e efficient voltage level shifter, it conducts both transitions those are high to low and low to high transition .But this low power voltage level shifter with GALEOR technique conducts only in high to low transition in this manner the total power consumed by the circuit was reduced. In this circuit also inverter driven with low input voltage and it gives high output voltage to drive the the next digital block in the circuit. The circuit with GALEOR technique have reduced power and increased speed by shutting off the some transistors in the time of working ,the circuit was operated in subthreshold range but it is also have working condition in above threshold range. High device density and low threshold voltages result in an increase in the leakage current dissipation[5]. Large on chip caches are integrated onto the current generation processors which are becoming a major contributor to total leakage power. The proposed static power reduction technique, GALEOR (GAted LEakage TransistOR), reduces the leakage current flowing through the circuits. Area overhead is minimized by eliminating the use of control logic to switch between the active and standby states. Performance overhead is increased due to the reduced output voltage swing.

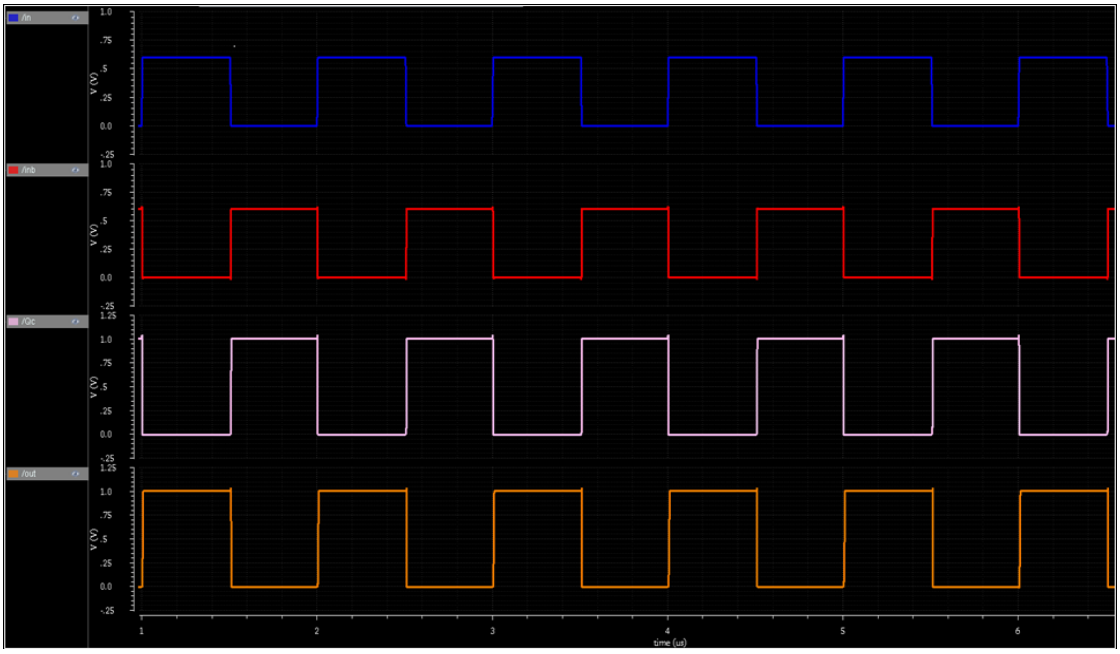

Fig.5. simulation results of low power voltage level shifter with GALEOR technique

When the IN voltage range is from high to low and INB is from low to high in this time of operation the transistors conduction is same as the efficient voltage level shifter but in GALEOR circuit it balances the power consumption so it results the overall power consumption was reduced. The out voltage is same phase as compared to IN but it reaches the value higher than the input voltage at the same manner Qc value us also reached certain value same as the output but the two signals output and Qc are in opposite phase.

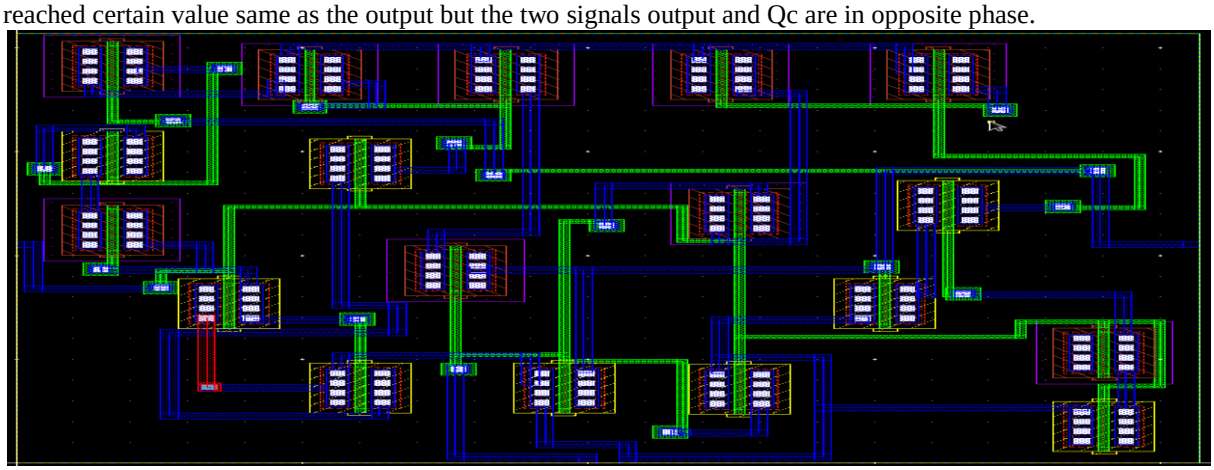

Fig.6. Layout of High Speed and Power efficient Voltage Level Shifter

IV. Simulation Results

The proposed voltage level shifter was verified by using Cadence virtuoso in standard TSMC 0.18µm CMOS technology. The bend results have reduced power-delay product (PDP).

Table.1. power, delay and transistor count reports in 180nm Technology

Circuit	Power	Delay	Transistor Count
Efficient voltage level shifter with auxiliary circuit	247nW	3.23ns	14
Low power voltage level shifter with GALEOR Technique	137nW	2.24ns	16

The given table contains the values at different frequencies and for various values of V_{ddl}, The delay and power are observed, the contention between devices is observed in sub-threshold region. Due to lower temperature the time required to generate signals will be increased and also produce less current.

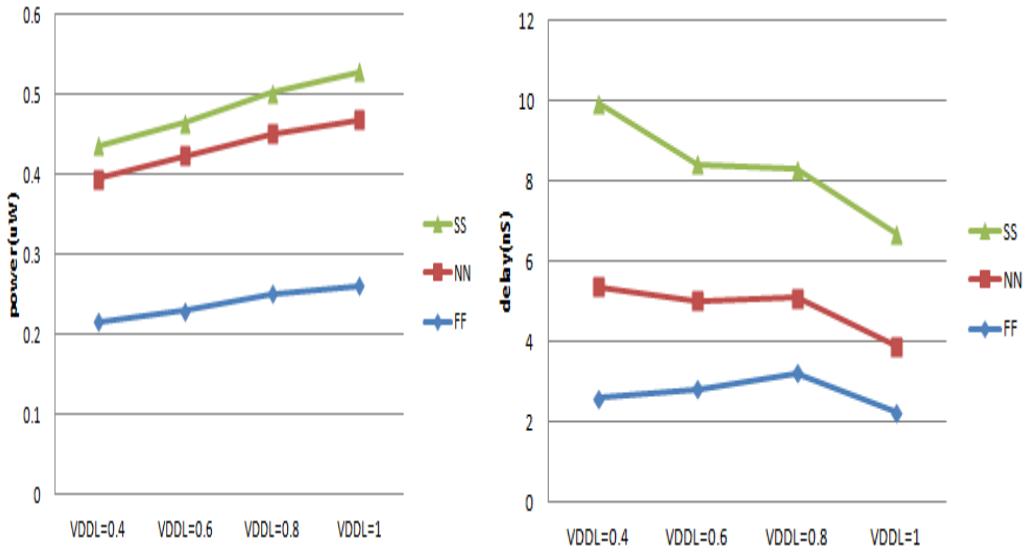

Fig. 7. Graph for Delay and power report at different Values of VDDL, on various corners.

This graphs shows the simulated output values of power and delay at different values of VDDL when supply voltage increases then power consumption increases and delay was reduced. In Fig. 6 shows the delay and the power report of the entire circuit.

V. Conclusion

In this paper the proposed circuit and existing circuit both are implemented in cadence virtuoso and observed the output functioning at different voltages to know the power levels at every point. The experimental resultsshows the circuit with GALEOR circuit minimizes the power consumption and increase the speed by the help of GALEOR technique. The overall circuit achieves on average 25% savings in leakage power by connecting GALEOR Circuit across the input and output terminals.

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