Design And Implementation Of Arithmetic Logic Unit Using Modified Quasi Static Energy Recovery Adiabatic Logic

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Abstract: This paper presents implementation of Arithmetic Logic Unit as it is fundamental building block of various computing circuits. 4 bit ALU is designed using Modified Quasi State Energy Recovery Logic (MQSERL) and CMOS logic. For implementing ALU, circuits which are needed are Multiplexer, Full adder and various basic gates such as Inverter, XOR, AND and OR are designed using both logic style. Comparative power analysis has been done to validate the Proposed MQSERL logic style which gives less power dissipation compared to conventional logic. The Arithmetic and Logic Unit designed using proposed MQSERL logic is 24.14 % and 33.28% power efficient than CMOS logic. The operating voltages for all the circuits are 1.8V and simulated using 180nm TANNER technology. For MQSERL circuits, two sinusoidal power clock which are 180° phase shifted with each other are used by maintaining frequency at 100Mhz and frequency of the input signal maintained at 50 Mhz.

Keywords: Low power VLSI, Quasi static energy recovery logic, Energy efficiency circuits, adiabatic computing, and Arithmetic logic unit.

I. Introduction

In today’s digital systems, the low energy operation is must. To achieve low power operations the approaches are to reduce supply voltage of circuit, loading capacitances of gates and to reduce switching activity. The alternative approach for energy reduction is Adiabatic circuits which has been examined in recent years [1-13]. Adiabatic logic works with the concept of reducing the power by giving stored energy back to the supply and this can be achieved by using an AC power supply called the power clock. Various Adiabatic logic families have been investigated which are reversible[7-8] and irreversible in nature. Reversible circuits have control signal coming from next stage, the design complexity is considerable but irreversible circuits have higher switching activity and use of multiphase power clock make them unfavourable for design. In order to overcome the disadvantages of irreversible logic circuits, Quasi Static Energy Recovery Logic (QSERL) has been proposed in literature [9] which resembled the static behavior and reduces the switching activity and design complexity. It utilizes two complementary sinusoidal power clocks. QSERL reduces energy dissipation. Operation of QSERL is performed in two phases Hold and Evaluate. But QSERL suffers from alternate hold phases due to which output is in floating condition which causes inrobutness. Modified quasi static energy recovery logic (MQSERL) is presented in order to eliminate the disadvantages of QSERL. The proposed logic style is a good alternative to conventional CMOS logic style. The paper presents implementation of multiplexer, full adder and basic gates using MQSERL logic style and CMOS logic style. Finally 4 bit Arithmetic unit and Logic Unit is designed and Performance of ALU is determined using both logic style by computing power dissipation and the number of NMOS and PMOS required for its implementation. All the circuits are operated at clock frequency of 100Mhz and voltage of 1.8V.

II. Modified Quasi Static Energy Recovery Logic Circuit

The Modified Quasi Static Energy Recovery Logic circuit is shown in fig 1. [9][11-12] consists of PMOS transistor which controls the charging path and NMOS transistor at bottom controls the discharging path .PMOS transistor is connected to clock signal and NMOS transistor at the bottom is connected to clock signal which is 180° phase shifted with upper clock signal. The proposed circuit offers less complexity in terms of wiring and design compared to Quasi Static Energy Recovery Logic (QSERL).
The clock signals are sinusoidal in nature as it offers less power dissipations compared to triangular and trapezoidal power clock. The sinusoidal clock charges and discharges the load capacitance slowly. The two clock signals are complementary to each other and height of clock signal is 1.8V peak to peak. The circuit operates in two phases evaluation and hold. During evaluation phase clock signal goes high and complementary clock signal goes low while in hold phase operation clock signal goes low and complementary clock signal goes high. Capacitor is charged through pmos transistor when output is low and pmos transistor is on during evaluation period, and output logic reaches at high level. When output is high and nmos transistor is on, capacitor discharges through nmos transistor and recycling of charges takes place reaching output logic at low level. The impact of leakage is less significant due to swinging and complementary clock signal.

III. Design of Mux and Full Adder
A. Design of 4:1 Mux using MQSERL
The structure for MQSERL 4:1 Mux is shown in fig.2. A multiplexer is combinational circuit that selects several input signal and forward the selected input to output line depending on status of select line. It consists of 14 pmos transistor in charging path and 14 nmos transistor in discharging path.

Fig 2. Design of 4:1 MQSERL MUX
The clock signal frequency is maintained at 100 MHz. Two clock signals are 180° phase shifted and offset is set at 0.9v. The circuit is simulated by setting the W/L ratio at 1. The input signal frequency is 50Mhz and logic 1 level is set at 1.8v and logic 0 at 0v. Though number of transistor required for the MQSERL Mux is more compared to CMOS Mux but 51.45% power is saved in MQSERL Mux. Comparative analysis is shown in Table I.

### Table I. Comparative Analysis between CMOS and MQSERL 4:1 MUX

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>Number of Transistor required</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Power Dissipated in watt</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS 4:1 MUX</td>
<td>26</td>
<td>13</td>
<td>13</td>
<td>5.718</td>
</tr>
<tr>
<td>MQSERL 4:1 MUX</td>
<td>28</td>
<td>14</td>
<td>14</td>
<td>2.776</td>
</tr>
</tbody>
</table>

#### B. Design of Full Adder using MQSERL

The Full Adder circuit is designed using MQSERL logic is shown in Fig.4. An adder is a digital circuit and used in Arithmetic logic unit. There are three inputs A,B, and Cin and two outputs sum and carry.
Full adder is designed using two XOR, two AND and one OR circuit using both logic style. The Fig. 5 shows simulation waveform for Full Adder circuit. Table II gives comparative analysis. MQSERL Full Adder is 19.02% power efficient than CMOS full adder though number of transistors required for implementation is more compared to CMOS logic.

**TABLE II.** Comparative Analysis between CMOS and MQSERL Full Adder

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>Number of Transistor required</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Power Dissipated in uwatt</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Full Adder</td>
<td>38</td>
<td>19</td>
<td>19</td>
<td>61.88</td>
</tr>
<tr>
<td>MQSERL Full Adder</td>
<td>44</td>
<td>22</td>
<td>22</td>
<td>50.11</td>
</tr>
</tbody>
</table>

**IV. Design of 4 Bit ALU**

The Arithmetic Logic Unit is a digital circuit used to perform arithmetic and logic operations. It represents fundamental building block of central processing unit. Truth table for 4 BIT ALU is shown in table III. A 2:1 multiplexer is used to select the arithmetic and logic operation. When M=0, Logic operations are performed and for M=1, arithmetic operations are performed.
A. Mqserl Logic Circuit

The logic circuit performs the basic logic micro operations such as NOT, OR, AND and XOR. From these four micro operations all known logic micro operations can be derived. Figure 7 shows the logic diagram for one stage of logic circuit. The four gates generate the four logic operations and the multiplexer select the desired operation as shown in Fig.9.

![Fig.7. Design of Logic Unit](image-url)
The arithmetic circuit performs typical arithmetic operations such as addition, subtraction and increment or decrement by one and transfer. The basic component of an arithmetic circuit is the Full adder. By using a multiplexer to control the data inputs to the adder, it is possible to obtain different types of arithmetic operations. The circuit diagram for 4-bit arithmetic is shown in Figure 10.
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TABLE V. Comparative Analysis between CMOS and MQSERL Arithmetic unit

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>Number of Transistor required</th>
<th>NMOS</th>
<th>PMOS</th>
<th>Power Dissipated in uwatt</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS ARITHMETIC UNIT</td>
<td>266</td>
<td>133</td>
<td>133</td>
<td>283.69</td>
</tr>
<tr>
<td>MQSERL ARITHMETIC UNIT</td>
<td>308</td>
<td>154</td>
<td>154</td>
<td>215.18</td>
</tr>
</tbody>
</table>

V. Experimental Results

Power dissipation analysis of two logic styles i.e. CMOS logic and MQSERL logic for various digital circuits are summarized in the table below. The W/L ratio was set at 1 and circuits are simulated using 180nm technology file. The operating voltage was 1.8V and complementary sinusoidal power clock of 100Mhz and input signal frequency of 50Mhz are used for all circuits.

TABLE VI. Power Dissipation Analysis

<table>
<thead>
<tr>
<th>DESIGN</th>
<th>Power Dissipated in uwatt</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>MOSERL</td>
</tr>
<tr>
<td>4:1 Mux</td>
<td>5.718</td>
</tr>
<tr>
<td>Full Adder</td>
<td>61.88</td>
</tr>
<tr>
<td>Logic unit</td>
<td>38.45</td>
</tr>
<tr>
<td>Arithmetic Unit</td>
<td>283.69</td>
</tr>
</tbody>
</table>
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VI. Conclusion

The comparative analysis and results indicate that the proposed Modified Quasi Static Energy Recovery Logic (MQSERL) is better approach for design of digital circuits than CMOS circuits. The design of Arithmetic Unit using the proposed logic is 24.14% and Logic unit is 33.28% efficient compared with CMOS logic. While comparing the designs of two logic styles, the same environment is maintained such as clock frequency, input signal frequency to compute power dissipation.

References


Fig.12. Comparative Power Analysis.