Implementation of High Speed Low Power Combinational and Sequential Circuits using Reversible logic

Krishna Naik Dungavath¹; Dr V.Vijayalakshmi ²

Ph.D. Scholar, Dept. of ECE, Pondicherry Engineering College, Pondicherry University Puducherry India.
Assistant Professor, Dept. of ECE, Pondicherry Engineering College, Pondicherry University Puducherry India.
Email: krishnad421@gmail.com...vvijizai@pec.edu

Abstract - Reversible logic has presented itself as a prominent technology which plays an imperative role in Quantum Computing. Quantum Computing devices theoretically operate at ultra high speed and consume infinitesimally less power. Research done in this paper aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realize Quantum computing devices. To authenticate this research, various combinational and sequential circuits are implemented such as a 4-bit Ripple-carry Adder, (8- bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of an 8-bit GCD processor using Reversible gates. The power and speed parameters for the circuits have been indicated, and compared with their conventional non-reversible counterparts. The comparative statistical study proves that circuits employing Reversible logic thus are faster and power efficient. The designs presented in this paper were simulated using Xilinx 9.2 software.

Key Terms - Reversible logic, Quantum computing, high-speed, less power, speed-power trade-off, Ripple carry adder.

I. Introduction

Reversible logic is widely used in low power VLSI. Reversible circuits are capable of back-computation and reduction in dissipated power, as there is no loss of information [1]. Basic reversible gates are employed to achieve the required functionality of a reversible circuit. The uniqueness of reversible logic is that, there is no loss of information since there is one-to-one correspondence between inputs and outputs. This enables the system to run backwards and while doing so, any intermediate design stage can be thoroughly examined. The fan-out of each block in the circuit has to be one. This research paper focuses on implementation of reversible logic circuits in which main aim is to optimize speed of the design. A Reversible adder is designed using basic reversible gates. Using this adder, an 8-bit reversible ripple-carry adder is devised and then compared with the conventional 8-bit adder in terms of speed, critical paths, hardware used. Then using the same reversible adder, a Wallace tree multiplier has been implemented, and compared with the conventional Wallace tree multiplier [3]. With the known fact that sequential circuits are the heart of digital designing, the design for the control unit of a reversible GCD processor has been proposed using Reversible logic gates [2].

II. Reversible Logic

Boolean logic is said to be reversible if the set of inputs mapped have an equal number of outputs mapped i.e. they have one-to-one correspondence. This is realized employing reversible gates in the designs. Any circuit having only reversible gates is capable of dissipating no power.

Goals of Reversible Logic:

A. Quantum Cost: Quantum cost of a circuit is the measure of implementation cost of quantum circuits. More precisely, quantum cost is defined as the number of elementary quantum operations needed to realize a gate.

B. Speed of Computation: The time delay of the circuit should be as low as possible as there are numerous computations that have to be done in a system involving quantum processor; hence speed of computation is a very important parameter while examining such systems.

C. Garbage Outputs: Garbage outputs are those output signals which do not contribute in driving further blocks in the design. These outputs become redundant as they are not required for computation at a later stage. The garbage outputs make the system slower; hence for better efficiency it is necessary to minimize the number of garbage outputs [5].

D. Feedback: Looping is strictly prohibited when designing reversible circuits.

E. Fan-out: The output of a certain block in the design can only drive at most one block in the design. Hence it can be said that the Fan-out is restricted to 1
III. Major Several Reversible Logic

3.1 Feynman Gate

It is a 2*2 Feynman gate [13]. The input vector is I (A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=AÅB. Quantum cost of a Feynman gate is 1. Figure 1 shows a 2*2 Feynman gate.

![Feynman gate](image1)

3.2 Double Feynman Gate (F2G)

It is a 3*3 Double Feynman gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q = AÅB, R = AÅC. Quantum cost of double Feynman gate is 2. Figure 2 shows a 3*3 Double Feynman gate.

![Double Feynman gate](image2)

3.3 Toffoli Gate

It is a 3*3 Toffoli gate [6]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q = B, R = ABÅC. Quantum cost of a Toffoli gate is 5. Figure 3 shows a 3*3 Toffoli gate.

![Toffoli gate](image3)

3.4 Fredkin Gate

It is a 3*3 Fredkin gate [7]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = AÅ BÅC and R = AÅ CÅB. Quantum cost of a Fredkin gate is 5. Figure 4 shows a 3*3 Fredkin gate.

![Fredkin gate](image4)
3.5 Peres Gate

It is a 3*3 Peres gate [5]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = AÅB and R=ABÅC. Quantum cost of a Peres gate is 4. Figure 5 shows a 3*3 Peres gate.

![Peres gate diagram](image1)

Fig 5: Peres gates

3.6 Double Peres gate

It is a 4*4 Double Peres Gate [6]. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S). The output is defined by P=A, Q=AÅB, R=ABÅD and S=(AÅB)DÅABÅC. Figure 6 shows a 4*4 Double Peres gate.

![Double Peres gate diagram](image2)

Fig 6: DPG gate.

IV. Reversible 4-Bit Full Adder

The gate used in implementing a reversible ripple-carry full adder is the TSG gate [4]. The TSG gate functions like a full adder. A reversible ripple-carry adder is faster than the non-reversible adder, since the computation of carry in a reversible adder does not require the computation of previous stage carry (as indicated in the critical paths). When previous stage carry is being forwarded in the reversible adder, the computation of previous stage carry and computation regarding sum is done simultaneously whereas in an irreversible adder the next stage carry cannot start any computation till previous stage carry is fully generated. The critical paths of 4bit reversible and irreversible ripple-carry adders are as shown in fig.7 and fig.8.[6].

![Critical Path of 4-bit reversible adder](image3)

Fig. 7: Critical Path of 4-bit reversible adder

![Critical Path of 4 bit irreversible adder](image4)

Fig. 8: Critical Path of 4 bit irreversible adder
Furthermore, various parameters of reversible and non-reversible adders were observed and compared and are tabulated in Table 1.

Table 1: Comparison of Reversible and Irreversible RCA

<table>
<thead>
<tr>
<th>Parameter (Virtex5 XC5VLX30 family)</th>
<th>8bit Reversible Ripple Carry Adder</th>
<th>8bit Irreversible Ripple Carry Adder</th>
<th>Improvement For Reversible Circuit (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time delay</td>
<td>5.062 ns</td>
<td>5.547 ns</td>
<td>8.74%</td>
</tr>
<tr>
<td>Power</td>
<td>267.18 mW</td>
<td>290 mW</td>
<td>7.87%</td>
</tr>
<tr>
<td>Area (No. of LUTs)</td>
<td>11</td>
<td>13</td>
<td>15.38%</td>
</tr>
</tbody>
</table>

V. Wallace Tree Multiplier

A Wallace tree is an efficient hardwired implementation of a digital circuit that multiplies two integers [5]. The Wallace tree has three steps:
1. Every bit of the multiplicand is multiplied (i.e. AND) by every bit of multiplier, thus yielding n^2 results (for n X n multiplication). Depending on position of the multiplied bits, the wires carry different weights, i.e. weight of bit carrying result of a5b6 is 65.

Fig. 9: 8X8 reversible Wallace tree Multiplier

2. The number of partial products is reduced to 2 by layers of full and half adders.
3. The wires are grouped in two numbers, and added using a conventional adder. The circuit diagram of Wallace tree multiplier using reversible gates is shown in Fig. 9. 8-bit Wallace tree multipliers were done and the comparison is as shown in Table 2.

Table 2: Comparison of Reversible and Irreversible Wallace Tree Multiplier

<table>
<thead>
<tr>
<th>Parameter (Virtex5 XC5VLX30 family)</th>
<th>8-bit Reversible Wallace tree multiplier</th>
<th>8-bit Irreversible Wallace tree multiplier</th>
<th>Percentage Improvement For Reversible multiplier</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time delay</td>
<td>9.548 ns</td>
<td>11.162 ns</td>
<td>14.46%</td>
</tr>
<tr>
<td>Power</td>
<td>266.84 mW</td>
<td>380.86 mW</td>
<td>29.94%</td>
</tr>
<tr>
<td>Area (no. of LUTs)</td>
<td>103</td>
<td>117</td>
<td>11.97%</td>
</tr>
</tbody>
</table>

VI. Design Of Control Unit For Gcd Processor

To illustrate the classical and reversible approaches to the Sequential Control Unit Design, reversible logic is employed for a special purpose processor that computes the GCD of two numbers. This GCD processor incorporates standard Euclid’s Algorithm involving Subtract-Compare-Swap operation of two numbers. The
basic principle is to subtract smaller of the two numbers repeatedly from the other number until we get the number that divides another

A. Control Unit

Control unit of GCD processor generates the control signals to manipulate the operations in Data-path. Fig. 9: Block diagram of GCD Control Unit.

Fig. 10: Block diagram of GCD Control Unit

B. Block Diagram Description:

1) Flip-flop Module:
The control unit for GCD processor requires two Flip-flops as binary state encoding is used for FSM. In this design reversible edge-triggered D Flip-flop is employed for state transitions [7]. Two D-latches are connected in Master-Slave mode to act as an edge-triggered D Flip-flop. Reversible D-latch is designed using Feynman and Fredkin gates. RTL schematic of reversible D flip-flop obtained is shown in fig. 11

Fig. 11: RTL schematic of Reversible D flip-flop

2) Regeneration Module

To avoid multiple fan-out condition in the design, it is necessary to duplicate signals used for computation of output and next state. The duplication of input signals is achieved using Feynman gates.

3) Output Module

The computation of the outputs and Next-state signals is done using reversible Fredkin gates. The functioning of output signal is driven by the algorithm.

4. Final RTL Schematic:
The complete RTL schematic of GCD control unit is shown in fig. 12.
Implementation of High Speed Low Power Combinational and Sequential Circuits using Reversible Logic

Fig 12: RTL schematic Diagram of GCD Control Unit

5. Speed and power analysis:

<table>
<thead>
<tr>
<th>Parameter (spartan3 xc3s50 family)</th>
<th>Irreversible GCD control unit</th>
<th>Reversible GCD control unit</th>
<th>Percentage Improvement for reversible circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speed (Max Clock freq)</td>
<td>434.33MHz</td>
<td>456.09MHz</td>
<td>5.01%</td>
</tr>
<tr>
<td>Power</td>
<td>25.02mW</td>
<td>24.19mW</td>
<td>3.31%</td>
</tr>
</tbody>
</table>

VII. Conclusion

In this paper, it can be seen that the performance of digital circuits can be enhanced using reversible gates and have compared 8-bit ripple carry reversible adder with an irreversible adder in terms of speed and power; there by concluding that reversible designs are faster and power efficient. Furthermore, this concept is extended to combinational circuits such as a Wallace tree multiplier using reversible gates, which were simulated and respective results validate prior interferences. Then a reversible sequential control unit of a GCD processor was designed. Thus, all the designs implemented were compared with their irreversible counterparts, and the speed and power parameters for the reversible designs were observed to have improved significantly.

References

Authors Profile

First Author -- Krishna Naik Dungavath is native of K.K Thanda a remote Tribal village of Anantapur district of Andhra Pradesh State, India. He studied his schooling from A.P.Residential School for BC’S at Srisailam Kurnool district, A.P and Intermediate from Sanjeevani Junior College, Venkatchelam of Nellore district, A.P. He received B.Tech degree in Electronics and Communication Engineering from Sri Venkateswara University, Tirupati, Andhra Pradesh, India. M.E., degree in Digital Systems Engineering from University College of Engineering (A), Osmania University, Hyderabad, India and Pursuing PhD at R&D cell Pondicherry Engineering College. Affiliated to Pondicherry Central University, Puducherry, India in the area of Low power VLSI. He is currently working as Associate Professor in Department of Electronics & Communication Engineering at P.V.K.K Institute of Technology, Anantapur, Andhra Pradesh, India. His research areas are VLSI Design, Digital systems, Wireless communications,

Second Author – Dr. V. Vijayalakshmi, M.Tech, Ph.D, Asst. Professor in the Department of Electronics and Communication Engineering, in Pondicherry Engineering College (PEC), Puducherry INDIA. Areas of interests are Cryptography, Information and Network Security, VLSI , ASIC.
Email id: vvijizai@pec.edu
Contact us on: (+91)-9440238727, (+91)-9443958141