

A Study of JK and T Flip Flops with and without Delay Using QCA

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Abstract: As transistors decrease in size, more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The use of quantum dots instead of CMOS transistors for implementing digital system at nanolevel is becoming more and more popular because of its faster speed, smaller size and low power consumption. Many interesting QCA-based logic circuits with smaller feature size, higher operating frequency, and lower power consumption than CMOS have been presented, even though the design of logic modules in QCA is not always straightforward. In this paper, the basic sequential logic structures-JK and T flip-flops are discussed based on QCA design, with comparatively less number of cells and area. Such devices are expected to function with ultra low power consumption and very high speed. Along with it, a design for T flip-flop with a delay is compared with a T flip-flop without any delay. The simulation result clearly testifies the validity of T flip-flop with delay.

Additional Key Words and Phrases: CMOS, flip-flops, QCA

I. Introduction

In the past few decades, CMOS technology has consistently played a vital role in implementing high density, high speed and low power VLSI systems. However, several studies have predicted that these technologies are approaching their physical limits. QCA can prove to be an attractive alternative. It is expected to achieve high device density, extremely low power consumption and very high switching speed. QCA structures are built as an array of quantum cells within which each cell has an electrostatic interaction with all its neighboring cells. In QCA, polarization, instead of traditional current contains the digital information. Though there are numerous advantages provided by QCA there are some challenges identified by Kogge[7]. One of them is the lack of feed- back. The 4-phase clocking scheme flows data in one direction. Physical feedback is essential in designing sequential circuits as the next state is dependent on the present state. Inclusion of feedback loops in QCA designs may result in complex clocking zone structure and floor planning. By introducing a delay, the global synchronization re- mains intact but a local asynchronous system can be introduced between cells and thus the feedback path functions accurately. The basic logic elements used in this technology are the inverter and the majority gate. The other logical structures are designed using these basic elements[4; 5; 10].

1.1. QCA Basics

QCA[2; 8] is a new device architecture that is amenable to nanometer scale. The QCA stores logic states not as voltage levels but rather based on the position of individual electrons. A quantum cell[3] can be viewed as a set of four charge containers or dots that are positioned at the corners of a square cell. Computation is realized by the Coulombic interaction of extra electrons in the quantum dots[6]. Each quantum dot is a nanometer-scaled square with wells at each corner of the cell. The two extra electrons that are present in each cell can quantum-mechanically tunnel between wells, but they cannot tunnel out of the cell. Provided that the electrons will always tend to occupy antipodal sites, there are two possible configurations as shown in the figure 1.

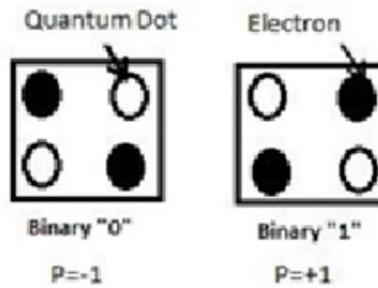


Fig. 1. Basic QCA cell and Two Possible Polarizations

1.2. QCA Clocks

The traditional CMOS clock and QCA clock[15; 16; 17] are quite different. In CMOS the circuit with a clock is known as sequential circuit. But in QCA the clock is provided to ensure the flow of data even it is a combinational circuit[14; 22; 24; 18; 19; 20; 21; 23; 1]. The fundamental QCA logical circuit is the three-input majority gate[11; 12; 13] (figure 2). Computation is performed with the majority gate by driving the device

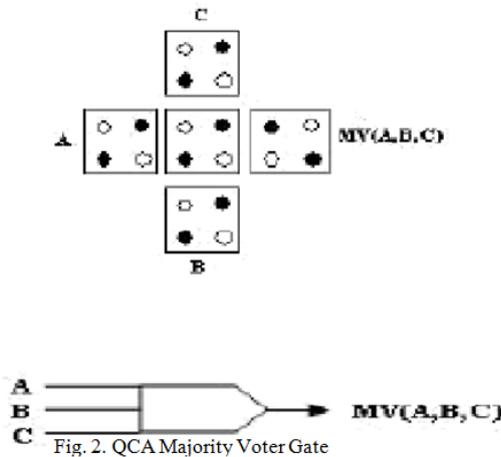


Fig. 2. QCA Majority Voter Gate

Cell to its lowest energy state. This occurs when it assumes the polarization of the majority of the three input cells. Clock zones are a tricky challenge of QCA. They avoid random adjustments of QCA cells and "guide" the information flow, in particular the data propagation, through QCA circuits. In contrast to transistor-based circuits, one clock cycle consists of four clock signals, which are delayed by of the whole clock cycle among each other, as depicted in figure 3. To ensure QCA circuits close to a ground state, a widely adopted clocking scheme is adiabatic switching which utilizes an adiabatic periodic signal with four different phases: switch, hold, release, and relax. When the potential is low the electron wave functions become delocalized resulting in no definite cell polarization. Raising the potential barrier decreases the tunneling rate, and thus, the electrons begin to localize. As the electrons localize, the cell gains a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched. Latched cells act as virtual inputs and as a result, the actual inputs can start to feed in new values. With the barriers lowering slowly, the electrons gradually become free and the cell starts to lose its polarization. During the relax

phase, the barriers are low, the electrons are free to tunnel and delocalize, and the cell has no polarization, i.e., $P=0$.

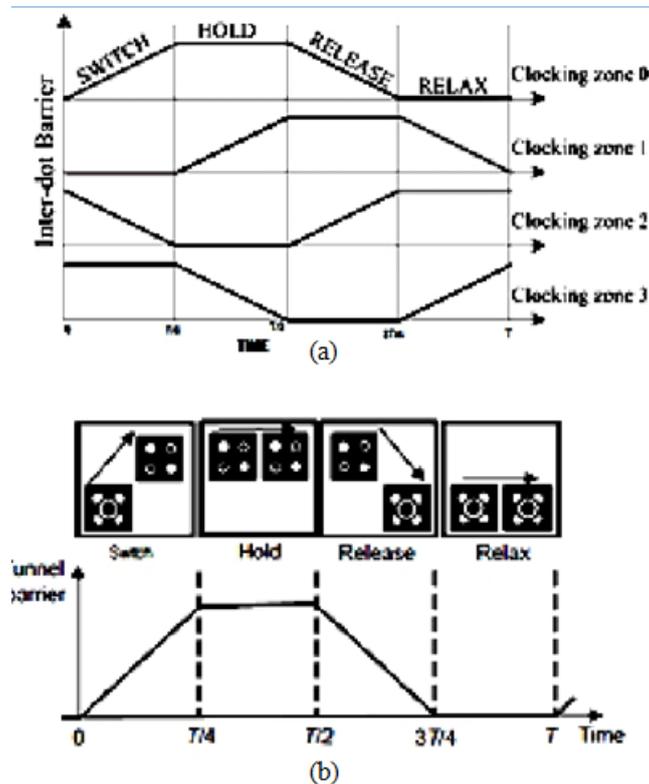


Fig. 3. QCA Clock

II. Flip-Flops

Flip-flops and latches are fundamental building blocks of sequential digital circuits where clock playing an important role to control the output[9]. In QCA we don't have any control over clock pulse.

2.1. JK Flip-flop

The JK flip-flop is a refinement of the RS flip-flop in that the indeterminate state of the RS type is defined in JK type. Only when inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state i.e. if $Q=1$, it switches to $Q=0$ and vice-versa. Because of the feedback connection in the JK flip-flop, the clock signal CP which remains at 1 after the outputs have been complemented once will cause repeated and continuous transitions of the outputs. To avoid this undesirable operation, the clock pulse must have a time duration which is shorter than the propagation delay through the flip-flop. In the proposed design, clock is considered in the characteristic equation so that it can have a definite impact. Not only the clock pulse but also the preset input is also considered to get the initial output. The new characteristic equation is obtained from the following table.

Table I. Truth table of JK Flip-flop

P	CP	Q	J	K	Q(t+1)
0	x	x	x	x	1
1	0	0	x	x	0
1	0	1	x	x	1
1	1	0	0	0	0
1	1	0	0	1	0
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	0
1	1	1	1	0	1
1	1	1	1	1	1

To simplify it, Karnaugh map is used and we get

$$Q(t + 1) = P \cdot Q' + CP \cdot Q + K' \cdot Q + CP \cdot Q' \cdot J \tag{1}$$

The circuit diagram of JK flip-flop using basic QCA gates is shown below.

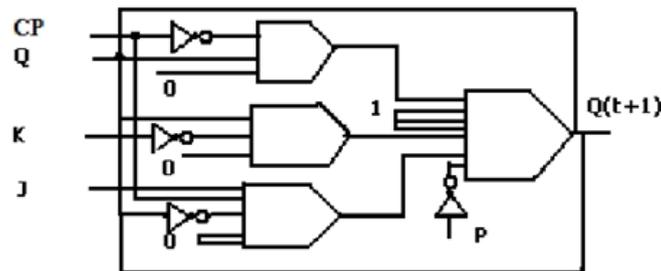


Fig. 4. Circuit Diagram of JK flip-flop

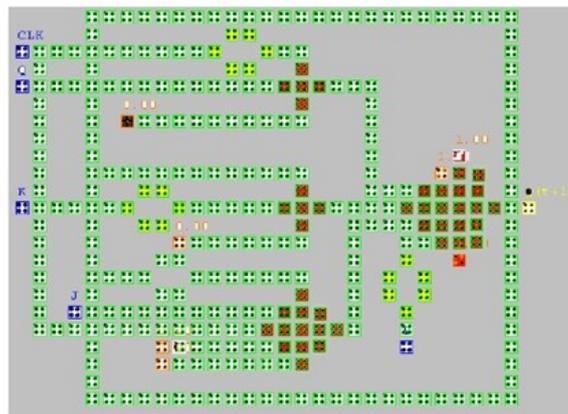


Fig. 5. Layout Diagram of JK flip-flop

2.2. T Flip-flop

The T flip-flop is a single-input version of the JK flip-flop. The t flip-flop is obtained from a JK type if both inputs are tied together. The designation T comes from the ability of the flip-flop to "toggle" or change state. Regardless of the present state of the flip-flop, it assumes the complement state when the clock pulse occurs while input T is logic 1. The traditional T flip flop has the following characteristic equation as given by.

$$Q(t + 1) = T \oplus Q + T' Q' = T \oplus Q. \tag{2}$$

The QCA cannot follow the traditional T flip flop design as to provide a feedback path is a major challenge. The truth table, taking the clock pulse and the preset input into consideration is shown below.

Table II. Truth table of T Flip-flop

P	CP	Q	T	Q(t+1)
0	x	x	x	1
1	0	0	x	0
1	0	1	x	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

The logical expression for T flip-flop is reduced to

$$Q(t + 1) = P \oplus CP \oplus Q + Q' T + CP \cdot Q \cdot T' \tag{3}$$

The circuit diagram of T flip-flop using basic QCA gates is shown below.

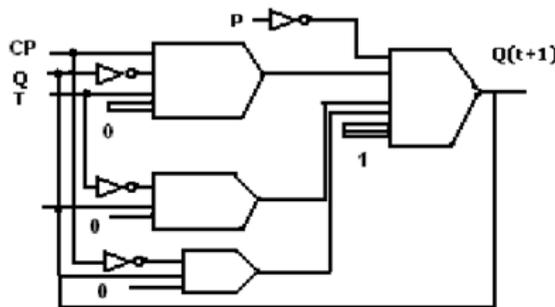


Fig. 6. Circuit Diagram of T flip-flop

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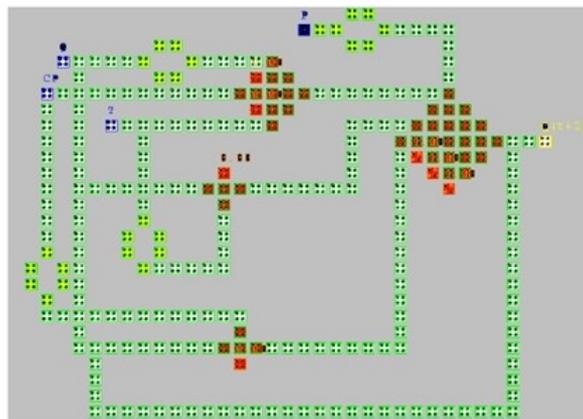


Fig. 7. Layout Diagram of T flip-flop

III. Result Analysis

In the proposed design, clock is considered in the characteristic equation so that it can have a definite impact. The advantage of introducing independent CP is that the design of QCA sequential circuits may be simplified by reducing the attention to timing constraints. Not only the clock pulse but also the preset input is also considered to get the initial output. At first the proposed T flip flop is designed which is synchronous to the global clock provided by the QCA designer. From the output of T flip flop it is very

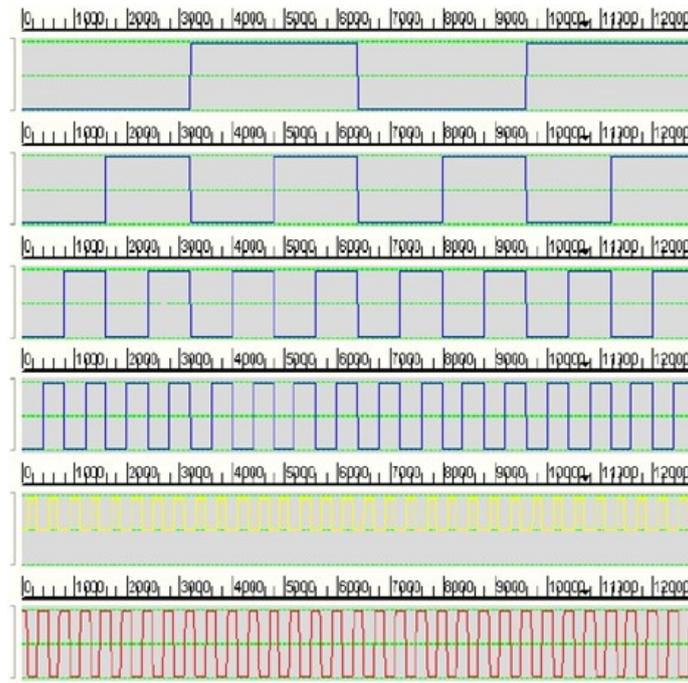


Fig. 8. Output of T flip-flop without delay

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Clear that the flip flop cannot hold a value. To overcome the latching problem an OR gate is introduced where the local cell clock is considered as clock 3 if QCA designer whereas the initial state is provided with clock 0. This setup provides a 3/4th delay to the output in compare to the input.

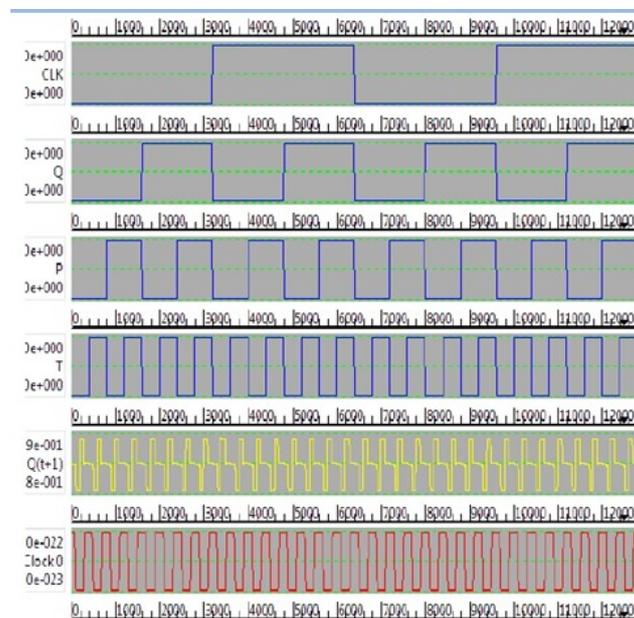


Fig. 9. Output of T flip-flop with delay

IV. Conclusion

In the case of current driven circuits, when have a feedback loop, the current gives the needed directionality. It ensures the fact that to start at the input and end at the output going through a series of voltage changes along the way. However, in this case, there is no current and no directionality. It is a system which waits to settle in a stable ground state. This means that the concept of feeding output back into the input is equivalent to actually feeding the input into the output since there is no question of direction. From the simulated output it is very much clear that the T flip flop without a delay cannot hold the value. Where as if we introduce a extra OR gate with a global clock with 3/4th T lagging with the starting clock to asynchronize the charge flow the output is convincing. By introducing another OR gate may increase number of cell count but looking at the output it may be considered.

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