

Design and Implementation of Flash ADC for Low Power Applications

Ram Prasad J M, Dr. B.S Kariyappa, Ravishankar Holla
R.V. College of Engineering, Bangalore

Abstract: Flash ADC is one of the most preferred architectures for high speed analog-to-digital data conversion applications. The comparator is a building block of virtually all analog-to-digital converter architecture. The kickback noise in the comparator is one of the important factor which leads to power dissipation. Hence the objective of this project is to design and implement a 4 bit Flash ADC by using effective comparator which reduces the kick back noise. Reduction of the kickback noise makes it possible to drive the ADC with higher impedance, which in turn reduces the power dissipation. Here the design of different types of comparators such as Preamplifier based, Double Tail Latch Type Voltage, Dynamic comparator and Double Tail Dual Rail Dynamic Latched comparators are analyzed. The Dynamic comparator without kickback noise is proposed for the flash ADC due its less power consumption. The proposed ADC offers a low-power solution with reduced Kickback noise. This design is simulated and analyzed in 90nm technology in Cadence virtuoso. Simulation results are tabulated and analysis has been done with graphical representation. The proposed flash ADC consumes 7.846mW power at sampling rate of 0.8 GS/s. When compared with previous work, this architecture showed 21.54% reduction in power consumption.

Index Terms: Analog to digital conversion (ADC), CMOS, comparator, kickback noise, and priority encoder.

I. Introduction

A Flash ADC is a type of *analog-to-digital converter* that uses a linear voltage ladder with a comparator to compare the input voltage to successive reference voltages [1]. The output of these comparators is generally fed into a digital encoder which converts the inputs into a binary value. A Flash converter requires a huge number of comparators compared to other ADCs, especially as the precision increases. A Flash converter requires $2^n - 1$ comparators for an n-bit conversion which increases the power consumption [2]. Therefore the power consumed by the comparator should be reduced. In this paper kickback noise reduction technique is proposed. Figure.1 shows a common structure of a latched comparator. In the reset phase, the switch is closed and the currents in the transistors of the differential pair depend on the input voltage. There will be a small differential output voltage because the switch has non-zero resistance, the circuit is operating as an amplifier. When the regeneration phase starts, the switch opens and the two cross-coupled inverters implement a positive feedback; this makes the output voltages go towards

0 and V_{DD} , according to the small output voltage found at the end of the reset phase. The large voltage variations on the regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the input of the comparator. Since the circuit preceding it does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is called *kickback noise* [3].

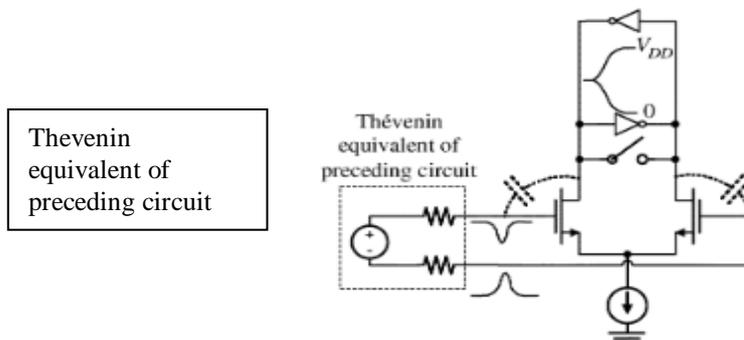


Figure.1 Kickback noise generation.

II. Design Of Flash Adc

One of the key advantages of the Flash topology is that it has a potential latency of only one clock cycle – that is the digital output is available within one clock cycle of the input being sampled. The block diagram of the proposed flash ADC is shown in figure.2.

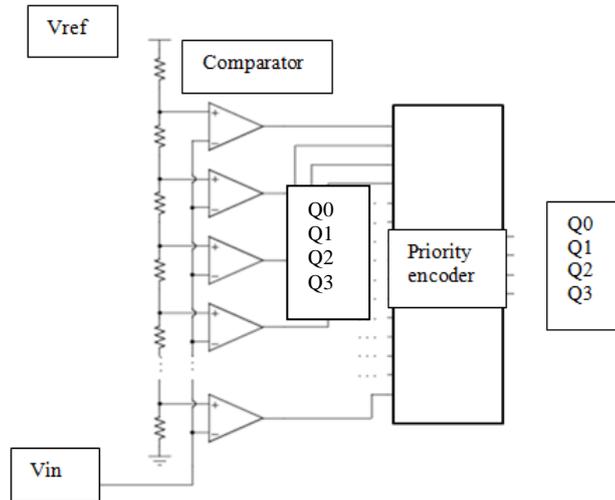


Figure.2 Block diagram of 4-bit Flash ADC

A. Comparator

For high speed, low resolution ADCs, the flash architecture is a promising approach. The proposed ADC offers a low-power solution with reduced Kickback noise. The different comparators used in the ADC have a built-in threshold. Owing to the difference in gate-drain capacitors of transistors M_{n2} and M_{n3} in figure.3 memory effect is introduced. During the reset phase of the comparator (when the sample clock is going from logic high to logic low), the nodes X_L and X_R are pulled up to the supply voltage. Assuming the output code was '1' ($V_{out+} = \text{high}$, $V_{out-} = \text{low}$), node X_R would initially be charged through M_{p6} in parallel with the series connection of M_{n5} and M_{p3} . Node X_L will only be charged through transistor M_{p1} . This results in a different time constants for the charging of the two branches, which includes different charges stored on the drain – gate capacitance of M_{n2} and M_{n3} . Different charges mean different voltages at the input nodes.

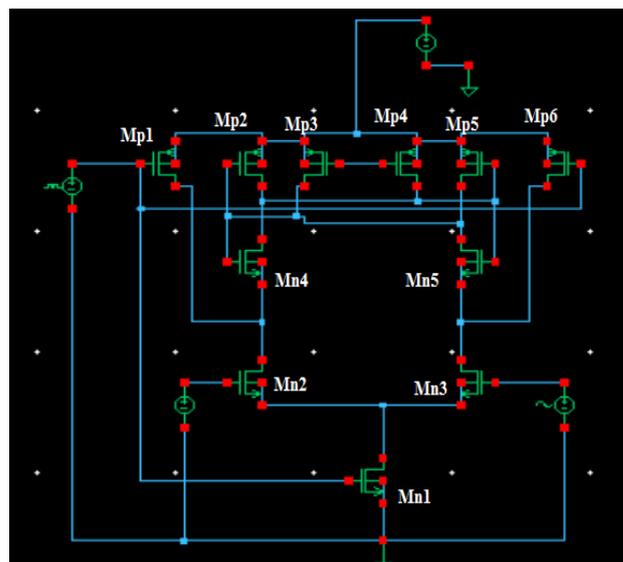


Figure.3 Conventional Comparator Schematic

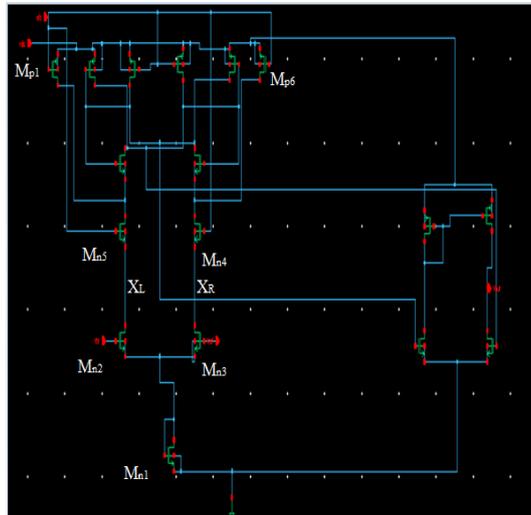


Figure.4 Proposed Comparator Schematic

By adding transistors M_{n4} and M_{n5} as shown in figure.4, the input transistors and their gate capacitance are disconnected from the nodes X_L and X_R and they are discharged more or less symmetrically during the reset phase via transistor M_{n1} . With the addition of the extra transistors, M_{n1} can be biased to reduce the current consumption of the comparator which slows down the slewing inside the comparator, which will further reduce the kickback noise.

B. Priority encoder design

A priority encoder is a circuit that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interrupt requests by acting on the highest priority request. If two or more inputs are given at the same time, the input having the highest priority will take precedence. The output indicates if the input is valid.

Priority encoder has $15(I_{14} - I_0)$ inputs and $4(Q_3 Q_2 Q_1 Q_0)$ outputs as shown in figure.5. Each input of priority encoder is driven by the comparator output, since at a time there are one or more output of the comparators are high, therefore the function of the priority encoder is to assign priority to each input. According to the priority assigned, the outputs of the encoder are driven.

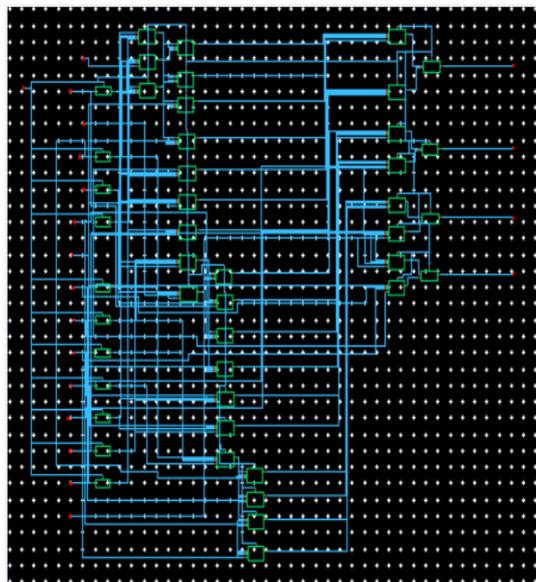


Figure.5 Schematic of priority encoder

The outputs of the comparator is connected to the inputs of the priority encoder as shown in figure.6. Based on the output logic value of the comparator the priority is assigned to each input and specific output signals are driven by the encoder.

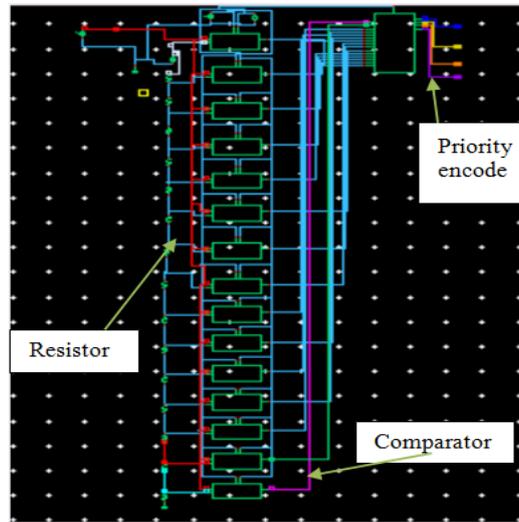


Figure.6 Schematic of 4-bit Flash ADC

From the analysis it can be shown that the dynamic comparator consumes less power, hence in this flash ADC design dynamic comparator is preferred.

B. Transient analysis of proposed flash ADC

The simulation is done using Cadence virtuoso tool. The different values of analog input voltage are shown in figure.8.

III. Simulation Results And Discussions

The Flash ADC is designed in 90nm CMOS technology with a 1.8 V supply in Cadence virtuoso tool.

C. Analysis of different types of comparators

The comparison of different comparators with respect to number of transistor, offset voltage, power consumption, propagation delay and speed is shown in figure.7.

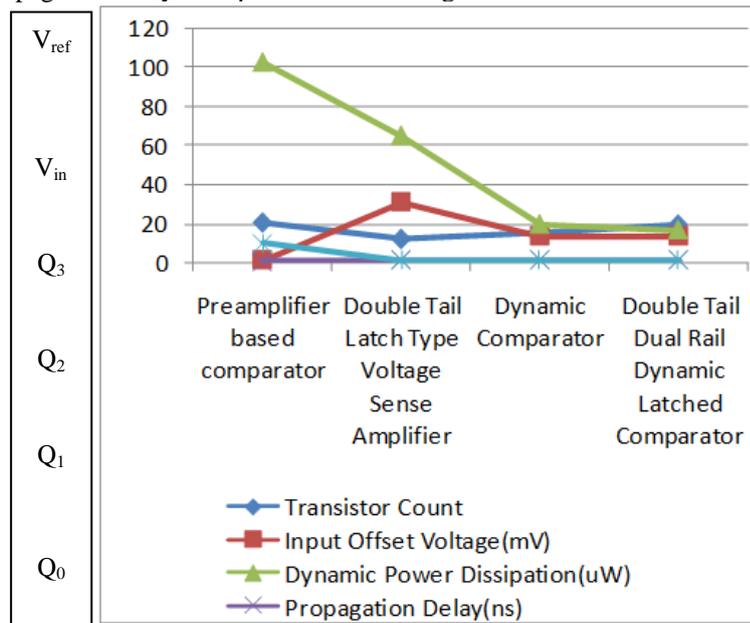


Figure.7 Analysis of different types of comparators
Time (ns)

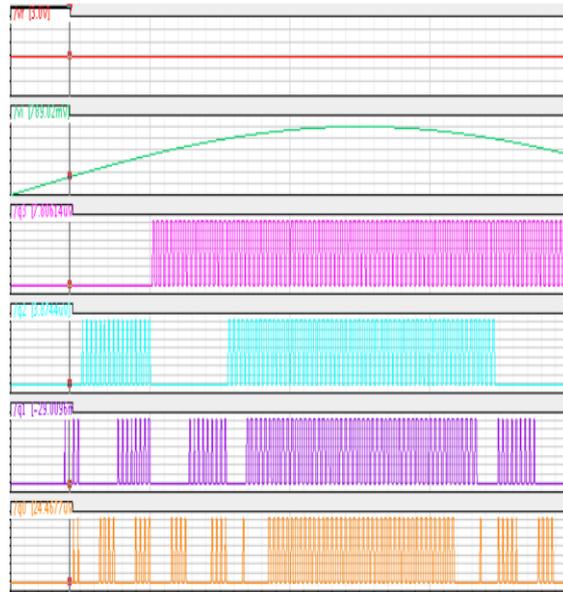


Figure.8 Simulation Waveforms of 4-bit Flash ADC

C. INL and DNL

The DNL and INL of the proposed Flash ADC are shown in figure.8 and figure.9 respectively. The DNL and INL for all output codes are shown, the maximum DNL is found to be 0.1669LSB and maximum INL is 0.314LSB.

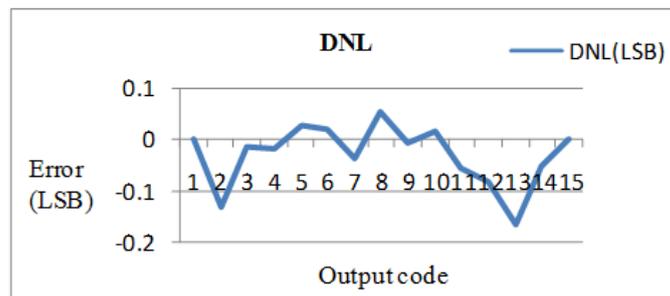


Figure.9 DNL plot of Flash ADC

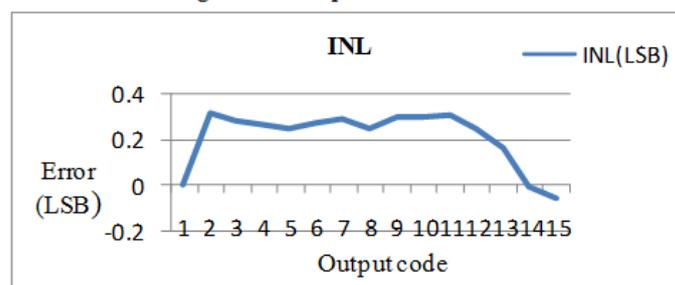


Figure.10 INL plot of Flash ADC

D. Comparison with previous work

The proposed Flash ADC is compared with the previous architectures [1] and analysis of different parameters is done and is tabulated in table I. From the analysis it can be shown that 21.54% of power is consumed at 1.8V supply voltage. At V_{dd} 1.2V, 67.22% of power is consumed and at V_{dd} 1V, 78.42% of power is consumed but speed decreases. Therefore there must be speed and power trade-off.

TABLE I. Comparison with previous work

Year	V _{dd} (V)	Bit (N)	Speed (GS/s)	Power (mW)	Tech(nm)
2010	1	5	3	36	65
2011	1.2	7	1.5	204	90
2012	0.5	6	0.05	0.3	180
2013	1.8	4	1.2	10	180
Proposed Flash ADC	1	4	0.7	2.158	90
	1.2	4	0.8	3.278	90
	1.8	4	0.8	7.846	90

IV. Conclusion

The Low power 4-bit Flash ADC is designed & simulated using cadence virtuoso tool successfully. The different types of comparators are designed and analysed. Among different types of comparators, due to the less power consumption, the dynamic comparator with reduced kickback noise is used in the design of flash ADC.

The DNL and INL are calculated for the designed flash ADC, the maximum DNL and INL are found to be 0.1669LSB and 0.314LSB respectively. It has been shown that by reducing the kickback noise of the individual comparators, the power consumption of comparator is reduced. In 4-bit Flash ADC there are 16 comparators which account for the large amount of power consumed. The proposed flash ADC consumes 7.846mW power at sampling rate of 0.8 GS/s. The overall power consumption of the flash ADC is reduced by 21.54% at 1.8V supply voltage in 90nm CMOS technology.

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