Performance Analysis of Low Power Bypassing-Based Multiplier

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Abstract: In the recent year growth of the portable electronics is forcing the designers to optimize the existing design for better performance. Multiplication is the most commonly used arithmetic operation in various applications like, DSP processor, math processor and in various scientific applications. In this paper a low power bypassing -based multiplier design is present, in which reduction in power is to be achieved in changed partial products of column bypassing multiplier as compared to column bypassing multiplier by exchange NOR gates with AND gates in the conventional multiplier i.e. in the design of conventional multiplier rather than AND gate, NOR gate is employed victimization DeMorgan’s theorem. Compare with 32x32 bits typical (parallel array) multiplier and column bypassing multiplier, this planned system consume less power.

Keywords: changed column bypassing multiplier, conventional multiplier.

I. INTRODUCTION

Multiplication is a necessary operation in DSP application. For the multiplication of 2 unsigned n-bit numbers, the number \( A=a_{n-1}a_{n-2}...a_0 \) and also the multiplier factor, \( B=b_{n-1}b_{n-2}...b_0 \) the product, \( P=P_{2n-1}P_{2n}...P_0 \) is depicted as the following equation:

\[
P = P_{2n-1}P_{2n}...P_0 = \sum_{j=0}^{n-1} \sum_{j=0}^{n-1} (a_j b_j) 2^{j}.
\]

To achieve the superior demand in DSP application, the structure of parallel array multiplier factor is wide used and also the typical implementation of such Associate in nursing array multiplier factor is Braun style. In n×n Braun multiplier[1],the multiplier factor array consists of (n-1) rows of carry-save adders(CSAs) and a (n-1) bit ripple carry adder within the last row, within which every row contains (n-1) Full adders(FAs). Multipliers square measure one among the foremost necessary arithmetic units in microprocessors and additionally a significant supply of power dissipation. Reducing the facility dissipation of multipliers is essential to satisfy the general power budged of varied digital circuits and system. Power consumed by multipliers is lowered at numerous levels of the planning hierarchy, from algorithmic rule to architectures to circuits, and devices.

II. PRELIMINARIES

A. Parallel Array Multiplier(Braun Multiplier)

Multipler factor circuit relies on add and shift algorithmic rule. Every partial product is generated by the multiplication of the number with one multiplier factor bit. The partial product square measure shifted in line with their bit orders so else. The addition may be performed with traditional carry propagated adder. N-1 adders square measure needed wherever N is that the multiplier factor length. The implementation of parallel array multiplier factor is additionally known as Braun design[5] as shown in figure1(b).
B. Low Power Bypassing Based Multiplier

- Column bypassing multiplier:
  
  For a low-power column-bypassing multiplier[3], the addition operations in the (i+1)th column can be bypassed if the bit, a_i in the multiplicand is 0. In the multiplier design shown in Fig(2), the modified FA is simpler than that in the row bypassing multiplier. Each modified FA in the CSA array is only attached by two tri-state buffers and one 2-to-1 multiplexer. As the bit, a_i in the multiplicand is 0, their inputs in the (i+1)th column will be disabled and the carry output in the column must be set to be 0 to produce the correct output. Hence, the protecting process can be done by adding an AND gate at the outputs of the last row of CSAs.

  The column bypassing multiplier (CBM) only needs two tri-state gates and one multiplexer in a adder cell. When y_j is 0 then the corresponding diagonal cells are functioning unnecessarily. In all these cells the partial products x_i × y_j and the carry inputs are zero for i = 0,1,…,n-1 and this chain does not contribute to the formation of the product. Consequently, the sum output of the above cell can bypass this unimportant diagonal with the use of transmission gates. To achieve all of the above we can replace the Full Adder cell shown in Figure 2(a) with the cell in Figure 2(b) called the Full Adder Bypassing (FAB) cell. The transmission gates in the FAB cell lock the inputs of the full adder to prevent any transitions when y = 0, and a multiplexer propagates the sum input to the sum output. When y = 1, the sum output of the full adder is passed.
Multiplier Design

The column bypassing multiplier is shown in Fig (1). Note that we only need two tri-state gates and one multiplexer in a modified adder cell. If $a_j=0$, the FA will be disabled. We do not need a tri-state gate for the carry input ($C_{i-1, j}$), and the reason is given as follows. For a Braun multiplier, there are only two inputs for each FA in the first row (i.e., row 0). Therefore, when $a_j=0$, the two inputs of FA0, j are disabled, and thus its output carry bit will not be changed. In the bottom of the CSA array, we need to set the carry outputs to be 0. Otherwise, the corresponding FAs may not produce the correct outputs since their inputs are disabled. This is done by adding an AND gate at the outputs of the last-row CSA adders. To understand the column bypassing technique, let’s take an example of $4 \times 4$ multiplication as shown in Figure 2(c), which executes $1010 \times 1111$.

III. THE PROPOSED DESIGN

- Modified column bypassing multiplier:

We propose a multiplier design in which partial products of column bypassing multiplier is modified. In the column bypassing multiplier, column can be disabled if the corresponding bit in the multiplicand is 0. There are two advantages to this approach. First, it eliminates the extra correcting circuit as shown in Fig. 2. Secondly, the modified FA is simpler than that used in the row-bypassing multiplier [2]. In the Proposed multiplier design instead of using AND gates we used NOR gates. The basic process of binary array multiplication involves the AND operation of multiplicand and multiplier bits and subsequent addition. NOR gates are used instead of AND in accordance with the De Morgan’s Law: $AB = (A' + B')'$

- Hardware Modification:

To design $4 \times 4$ bit multiplier we have a tendency to need sixteen AND gates, of that every AND gate consists of 6 transistor. A similar hardware will replace by NOR gate that consists of solely four transistors. This reduction in hardware results into less power consumption.
Thus, for a $m \times n$ multiplier factor, the projected technique introduces $m + n$ further inverters beside dynamic
$m \times n$ AND gates to $m \times n$ NOR gates, effectively saving $(m \times n - (m + n))$ inverters or $2(m \times n - (m+n))$
transistors. Figure (3) shows projected multiplier factor style with the replacement of AND gate with a NOR
gate in partial product of column bypassing multiplier, ensuing into demand of less no. of transistor than the
traditional style. The inputs are given in inverted form i.e. using NOT gate as shown in table I below:

Table I: Circuit Analysis of hardware modified for 32 bit multiplier

<table>
<thead>
<tr>
<th></th>
<th>No. of AND gates($n^2$)</th>
<th>No of transistors</th>
<th>No of NOR and NOT gates($n^2$)</th>
<th>No of transistors for</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>NOR gate</td>
</tr>
<tr>
<td>For 32-bit</td>
<td>$32^2=1024$</td>
<td>$1024 \times 6=6144$</td>
<td>$1024 &amp; 64$</td>
<td>$1024 \times 4=4096$</td>
</tr>
<tr>
<td>multiplication</td>
<td></td>
<td></td>
<td></td>
<td>$64 \times 2=128$</td>
</tr>
<tr>
<td>Total transistor</td>
<td></td>
<td>$6144$</td>
<td></td>
<td>$4096 + 128 = 4224$</td>
</tr>
</tbody>
</table>

IV. RESULT

The performance analysis has been carried out on the proposed multiplier by performing simulations on
Quartus II(8.1) and compared with the existing multipliers i.e Braun multiplier and column bypassing multiplier.
Simulations are performed for $32 \times 32$ bit multiplier. Results shown in figure 4,5,6 are for particular inputs
$22222222 \times FFFFFFFF$. Similar result can also be obtain for other inputs. The power analysis and actual time is
listed in Table II.
Performance Analysis of Low Power Bypassing-Based Multiplier

Figure 4: Simulation and power analysis of 32×32 bit Braun multiplier

Figure 5: Simulation result and power analysis of 32×32 bit column bypassing multiplier

Figure 6: Simulation result and power analysis of 32×32 bit modified column bypassing multiplier (Proposed design)
Performance Analysis of Low Power Bypassing-Based Multiplier

Comparison between Power and Actual time of three different multiplier

Table II: power comparison between Braun, column-bypassing and modified column-bypassing multiplier

<table>
<thead>
<tr>
<th>Multipliers</th>
<th>Power</th>
<th>Actual Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Braun multiplier</td>
<td>124.65mW</td>
<td>70.56nS</td>
</tr>
<tr>
<td>Column-bypassing multiplier</td>
<td>108.26mW</td>
<td>69.72nS</td>
</tr>
<tr>
<td>Modi-column-bypassing multiplier</td>
<td>93.52mW</td>
<td>62.52nS</td>
</tr>
</tbody>
</table>

IV. CONCLUSION

In this paper, a new approach for the design of partial product in column bypassing multiplier has been suggested. AND gates in the existing designs have been replaced with NOR gates. Where inputs are given in the inverted form. Results of simulation and power analysis show that the proposed (modified column bypassing) multiplier performs better than the existing system.

V. REFERENCES