Design Modulo-4 and Galois Field Adder, Subtractor and Multiplier Using Quaternary Logic

Miss. Rajashri R. Korde, Asst.Prof. Dinesh Rotake

Abstract: Arithmetic circuits play a very necessary role in every general and application specific procedure circuits. Multiple Valued Logic (MVL) provides the key smart factor concerning future density per circuit area compared to ancient two valued binary logic. Quaternary (Four-valued) logic jointly offers the nice factor concerning easy interfacing to binary logic as a results of base four (=22) permits for the use of easy encoding/decoding circuits. The purposeful completeness is proved with a set of basic quaternary cells. The library of cells supported the Supplementary Symmetrical Logic Circuit Structure (SUSLOC) unit of measurement designed, simulated, and accustomed build several quaternary fixed-point arithmetic circuits like adders, multipliers. These SUSLOC circuit cells unit of measurement valid practice SPICE models and additionally the arithmetic architectures unit of measurement valid practice System Verilog models for purposeful correctness. Quaternary (radix-4) twin amount secret writing principles unit of measurement applied to optimize power and performance of adder circuits practice common place cmos gate technologies.

Index Terms: Multiple-valued logic, Quaternary logic, Modulo-n addition, subtraction and multiplication, Galois. Addition and multiplication.

I. Introduction

The outstanding increase inside the density of very large Scale Integrated (VLSI) circuits is that the results of advanced Integrated Circuits (IC) fabrication processes and so the event of machine-driven vogue tools. As a result of the vary of devices accommodated on VLSI chips can increase, many problems in addition arise. For instance, the interconnection between devices inside and out of doors a chip becomes significantly subtle and so the area occupied by interconnections can increase hurriedly. Aggressive interconnect scaling following Moore's law introduces many challenges in integration, performance and responsibility. Inappropriate routing winds up in a very larger chip size and cause temporal property and cross-talk problems. In deep submicron designs these problems unit of measurement of outstanding importance. The partial solutions to the current draw back in today's VLSI circuits unit of measurement to use several metal layers, flip-chips and other ways, although improvement in metal stack material have enabled business to scale back interconnect resistance in slim lines and at an analogous time changes in layer stuff (ILD) material have down the road to line capacitance resulting in Resistor-Capacitor (RC) delay improvement so interconnect power consumption, however, deep submicron technology introduces formidable integration and responsibility challenges like higher slim conductor line resistance, higher current density and inferior thermo-mechanical properties that ought to be overcome. It's acknowledge that the positional representation system of numeration is that the leading various for normal voltage-mode variety of digital systems. However, in a very typical positional representation system of numeration based VLSI circuit concerning seventy p.c of chip area is occupied by interconnections that occupy associate degree outsized portion of physical area even once it isn't in use, so the interconnections square measure attending to be extra economical if several levels of logic unit of measurement injected into one wire, as in multiple valued logics. Dissimilar to binary logic, multiple valued logics want quite two distinct levels of logic signals and allow quite two logical concepts to exist in a very logic system. Thus, the direct sensible factor regarding such logics is that the improved overall information efficiency. It's as a results of each r-valued signal can carry times extra information than a binary signal can. As a result the routing area is reduced on a exponent scale-as r can increase. This reduction in vary of interconnections and area of a chip is understood by regarding Figure one.1. As is seen, the routing area of a 4-valued logic vogue is two times smaller than the corresponding binary logic system. 2 log r log r2 the choice of the foremost favorable logic range in term of implementation value has been in addition studied by some researchers. The circuit implementation value is decreasing with increasing logic range and in step with C.M. Allen and D. Givorn, the optimum range is larger than Euler constant. Since in apply the amount r is Associate in Nursing integer, it comprehends that the extra advantageous range ought to be a minimum of 3 or in numerous words ternary logic. On the other hand conversion with binary is best if special radices unit of measurement chosen in such however that no information Is lost or left unused e = 2.7
II. Objective

1) Use of deep metric long measure technology for quaternary arithmetic circuit vogue.
2) Low power has to be done.
3) Static power and dynamic power is main objective of fashion.
4) Quaternary arithmetic circuit vogue are through with modulo logic and mathematician field logic. style of gates required for mathematician field are less as compared to modulo.
5) Use of single pin to induce a quaternary logic levels.
6) Three DLC with mux are required for quaternary to binary conversion and one DLC is required for binary to quaternary conversion.
7) Totally different industrial plant file has to be designed for varied DLC.

III. Literature Survey

Vasundara Patel & Gurumurthy projected a low-power, high-speed, minimum area. They designed quaternary full adder pattern binary logic gates and range converter. Simulation done by pattern HSPICE and COSMOS tools. They used 180nm technology.[1]

In M. Thoidis paper[11], the projected circuits were static and operate in voltage mode. The reported no static power dissipation as a result of the circuits were static in nature[11].

Economist designed a netruly full adder quaternary circuit pattern 3 power provide lines and multi-Vt transistors .Ricardo has designed quaternary device (MUX) 4:1 with 4quaternary inputs and one quaternary output and used this MUX as a building block to construct full adder projectected technique blessings big scale circuits since the teeming power dissipation with increased speed can cause the event of very low energy circuits whereas sustaining the high Performance required for many applications[7].

The implementation of Quaternary Signed Digit addition was given in paper[5] . The take a glance at confirms the superior performance of the QSD adder implementation over different adders. as a result of the carry – free addition theme. The quality of the QSD adder was linearly proportional to the number of digits, that ar of an analogous order as a result of the only adder, the ripple carry adder. This QSD adder is employed as a building block for different arithmetic operations such Multiplication, division, root, etc. With the QSD addition theme, some well-known arithmetic algorithms is directly enforced[5].

IV. Implementation

Implementation of binary to quaternary conversion:-

Fig: circuit diagram of binary to quaternary conversion

A basic binary to quaternary circuit consists a pair of PMOS and a couple of NMOS transistors that kind 2 inverters and a couple of DLC one circuits. LSB and savings bank a pair of bit binary varitets area unit provide to 2 DLC1 circuits and output of two inverters will give quaternary variety.
Implementation of quaternary to binary conversion:

A basic Quaternary to binary convertor uses 3 down literal circuits DLC1, DLC2, DLC3 and 2:1 electronic device. Latter is that the quaternary input variable as zero, 1, a pair of and three that is given to 3 DLC circuits. The binary out puts therefore obtained are in complemented type and area unit needed to labor under inverters to urge actual binary numbers.
Modulo-4 addition circuit is shown in figure 5. Throughout this circuit, to induce input and output in quaternary kind, quaternary to binary circuit is connected to the input of the modulo-4 addition circuit and binary to quaternary circuit is connected to the output of the modulo-4 addition circuit. Here throughout this figure giving input in quaternary kind and getting output in quaternary kind. This output satisfies the modulo-4 addition table as shown in table 3. Minimal functions area unit obtained from the Karnaugh diagrams for the addition table shown in table so simplified the utmost quantity as possible victimization all possible gate varieties. Minimal functions obtained from the minimal polynomials extracted from the Karnaugh diagrams area unit shown below. Let \( x_1 \) \( x_2 \) and \( y_1 \) \( y_2 \) be the binary illustration of quaternary numbers that ought to be a lot of.

For addition:

\[
a_1 = (x_1 \oplus y_1) \oplus (x_2 y_2) \quad (3)
\]

\[
a_2 = (x_2 \oplus y_2)
\]
Implementation of Galois field adder:

Fig: circuit diagram of Galois field adder
Galois addition table in Figure is utilized in Karnaugh diagrams to induce minimum operate. Stripped functions obtained from the stripped polynomials extracted from the Karnaugh diagrams for GF (4) addition is shown below. Let x1 x2 and y1 y2 be the binary illustration of two quaternary numbers that have to be compelled to be compelled to be accessorial. a 1 and a 2 square measure the two bit results of addition between x1x2 and y1y2.

\[
a_1 = x_1y_1 \\
a_2 = x_2y_2
\]

Above equation shows that addition in GF (4) needs solely 2 gates and depth of web is reduced to a minimum of one. Usually this can be often a extremely smart vogue among four circuits. Logical implementation of the circuit is shown in figure.

Implementstion of modulo-4 subtractor:-

<table>
<thead>
<tr>
<th>x1</th>
<th>x2</th>
<th>y1</th>
<th>y2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>2</td>
<td>3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>2</td>
<td>0</td>
</tr>
</tbody>
</table>
Modulo-4 subtractor circuit is shown in figure 9. Throughout this Circuit, to induce input and output in quaternary kind, quaternary to binary circuit is connected to the input of the modulo-4 subtractor circuit and binary to quaternary circuit is connected to the output of the modulo-4 subtractor circuit. Here throughout this figure giving input in quaternary kind and getting output in quaternary kind. Modulo-4 subtractor circuit is that the combination of 3 xor and one AND circuit and generate the distinction and barrow within the output that is given to the binary to quaternary device. This output satisfies the modulo-4 subtractor table.
Implementation of Galois field subtractor:

![Fig: circuit diagram of Galois field subtractor](image1)

![Fig11: schematic of Galois field subtractor](image2)  
Galois subtractor circuit is shown in figure11. Throughout this circuit, to induce input and output in quaternary kind. 1st quaternary to binary circuit is connected to the input of mathematician field subtractor circuit. This circuit contains 2 gates one is xor and another one is logic gate. This circuit cut back the no. of gate as compare to modulo- four subtractor. This cut back the depth of interconnection. The output of mathematician field subtractor circuit connected to binary to quaternary converter, output is within the style of quaternary kind.

![Fig12: waveform of Galois field subtractor](image3)  

Implementation of modulo-4 multiplier:

![Table: modulo-4 multiplication](image4)
Fig: circuit diagram of modulo-4 multiplier

Fig 13: schematic of modulo-4 multiplier

Fig 13 shows the modulo-4 multiplier circuit. This circuit requires 4 gates to perform operation and then obtain binary output converted to quaternary kind.

Fig 14: waveform of modulo-4 multiplier

Implementation of Galois field multiplier:-

Fig: circuit diagram of Galois field multiplier
Fig 15: schematic of Galois field multiplier

Fig 15 shows the Evariste Galois field multiplier factor circuit. During circuit, no would like of quaternary to binary and binary to quaternary conversion. This circuit is that the combination of 3:4:1 mux. The output happy the Evariste Galois field multiplier factor table.

Fig 16: waveform of Galois field multiplier

Implementation of max application :-

Fig 17: schematic of max application

Fig shows the application. There in schematic totally different inputs are given and at output facet offers the utmost output. Fig 18 shows the output wave shape.
TSPICE transient analysis simulation is finished to verify the practicality of the circuits. 50nm technology files are used for simulations. Simulation results of quaternary to binary and binary to quaternary are shown in figure1 and figure3 severally. Simulation results of Modulo-4 addition, modulo-4 subtraction, modulo-4 multiplication and Galois Field addition, Galois field subtraction and Galois field multiplier factor and conjointly one application max are shown on top of.

The below table shows the comparison between modulo-4 and Galois field through power, semiconductor device and current.

<table>
<thead>
<tr>
<th>NAME</th>
<th>VOLTAGE</th>
<th>NO.OF MOSFET</th>
<th>POWER</th>
<th>CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODULO ADDER</td>
<td>3V</td>
<td>94</td>
<td>845.91nW</td>
<td>281.33nA</td>
</tr>
<tr>
<td>GALOIS ADDER</td>
<td>3V</td>
<td>76</td>
<td>270.63nW</td>
<td>89.47nA</td>
</tr>
<tr>
<td>BINARY TO QUATERNARY</td>
<td>3V</td>
<td>8</td>
<td>420.90nW</td>
<td>140.3032nA</td>
</tr>
<tr>
<td>QUATERNARY TO BINARY</td>
<td>3V</td>
<td>22</td>
<td>210.89nW</td>
<td>70.2991nA</td>
</tr>
<tr>
<td>MODULO SUBTRACTOR</td>
<td>3V</td>
<td>108</td>
<td>1.0872uW</td>
<td>286.1056nA</td>
</tr>
<tr>
<td>GALOIS SUBTRACTOR</td>
<td>3V</td>
<td>72</td>
<td>845.8627nW</td>
<td>281.954nA</td>
</tr>
<tr>
<td>MODULO MULTIPLIER</td>
<td>3V</td>
<td>82</td>
<td>1.0872uW</td>
<td>286.1909nA</td>
</tr>
<tr>
<td>GALOIS MULTIPLIER</td>
<td>3V</td>
<td>40</td>
<td>9pW</td>
<td>3pA</td>
</tr>
<tr>
<td>APPLICATION MIN MAX</td>
<td>3V</td>
<td>39</td>
<td>9.33nW</td>
<td>3.113mA</td>
</tr>
</tbody>
</table>
VI. Conclusion

Binary to quaternary and quaternary to binary converters square measure designed exploitation down literal circuits. Implementation of the circuit shows higher performance than circuits exploitation 2 variable representations. Circuits for Modulo-4 addition, subtraction, multiplication need solely four gates. Evariste Galois addition, subtraction needs 2 gates that is most optimized one in all different circuits where as implementing in VLSI.

With the assistance of quaternary logic levels, we’ve got reduced the interconnections. we’ve got conjointly used less range of gates and therefore less space for Evariste Galois and modulo-4 arithmetic operations. Projected circuits square measure appropriate for implementing in VLSI with less range of interconnections and fewer space.

References


