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Power Efficient Successive Approximation Registers

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Abstract: *In recent years, there has been a growing need for Successive Approximation Register (SAR) Analog-to-Digital Converter in medical application such as pacemaker. The demand for long battery life-time in these applications poses the requirement for designing ultra-low power SAR ADCs. The project involves custom design and implementation of 8 bit successive approximation ADC for low power and low frequency signals. The ADC would comprise of a SAR Logic, DAC, a comparator and a sample and hold circuit. The DAC would be designed to reduce the systematic and the symmetric errors using the hierarchical symmetrical switching. The main motivation is to implement design of capacitor array DAC and achieve high speed with medium resolution using 60nm technology. The advantage is matching of capacitor can be achieved better then resistor. The market and cost analysis says current SAR ADC has better future. Here we are using spice backend design Tool.*

Keywords: *SAR ADC, SAR Logic, Comparator, Low Power, high speed.*

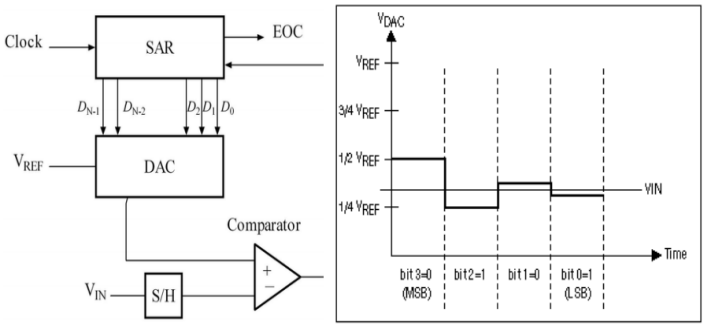
I. Introduction

The growing trend in wireless communication has lead to crowding of the available frequency bands. With a vast increase in digital media transfer, the focus has shifted towards designing multi-gigabit subsystems in silicon. In order to provide a cost effective solution, circuits designed in CMOS are implemented in a single system on chip. The 90nm ST Microelectronics Digital CMOS process, optimized for digital circuit design requires a lot of internal compensation for analog circuits to meet the expectation. The three major causes for concern is process, temperature and supply voltage variation. The focus of this thesis is on the design of a feedback control loop, which uses temperature as the sensing element to control output power variation and the design of 3.5 GHz transmitter which acts as a feeder for multiband transmitter systems. The focus is on two aspects of integrated circuit design. First one is on the challenges faced in the design of the various components of the feedback control loop Successive approximation ADC, Encoder & Temperature sensor, while the second one is on the design of high linearity, low noise figure mixer and system level simulation leading to optimizing various components to achieve the target specifications. Successive approximation ADC operates with medium conversion speed, moderate circuit complexity and high conversion accuracy. SAR ADC is one of the most popular Nyquist rate data converters. The terms "Divided reference algorithm" and "Binary search algorithm" can be used to best describe the basic principles of SAR data converter.

Successive approximation employs a binary search algorithm in a feedback loop including a 1 bit A/D converter. This architecture which consists of a front end track & hold circuit, comparator, DAC and SAR logic. SAR logic is basically a shift register combined with decision logic and decision register. The pointer points to the last bit changed in the decision register and the data stored in this register is the result of all comparisons performed during conversion period. During binary search, the circuit halves the difference between the sampled signal (V_{IN}) and DAC output (V_{DAC}). The conversion first sets MSB as 1 so that the DAC produces midscale at analog output. The comparator is then strobe to determine the polarity of V_{IN}-V_{DAC}. The pointer and the decision logic direct to logical output of the comparator to the MSB. If V_{IN}>V_{DAC} the MSB of the register is maintained at 1 or else set to 0. Subsequently the pointer is set to choose the bit penultimate to MSB as 1. After the DAC output has settled to its new value, the comparator is strobe once again and the above sequence is repeated.

For a resolution of M bits, the successive approximation architecture is at least M times slower than the full-flash configurations, but it offers several advantages. The comparator offset voltage does not affect the overall linearity of the converter because it can be represented as a voltage source in series with Sample & hold output, indicating that offset voltage simply adds to analog input and hence appears as an offset in the overall characteristics. Consequently the comparator can be designed for high speed operation in high resolution systems. This architecture does not require an explicit subtractor which is an important advantage for high resolution applications. The circuit complexity and power dissipation are in general less than

that of the other architectures. If the Sample & hold circuit provides the required linearity, speed and comparator input referred noise is small enough, and then the converter performance depends primarily on the DAC. In particular differential and integral non linearity of the converter are given by those of the DAC, and the maximum conversion rate is limited by its output settling time. In the first conversion cycle, the DAC output must settle to maximum resolution of the system so that the comparator determines the MSB correctly. If the clock period is constant, the following conversion cycles will be as long as the first one, implying that the conversion rate is constrained by the speed of the DAC.



Block diagram of SAR ADC & DAC Output Waveform

II. Low Power Techniques In Digital Design

2.1. Supply Voltage Reduction

In digital circuit design, one of the main strategies for lowering power consumption is supply voltage scaling, since dynamic power consumption is proportional to the square of operating voltage. On one hand, lowering the supply voltage will reduce the dynamic power consumption, but on the other it reduces the speed, and thus there should be a tradeoff in reducing the supply voltage to maintain the system at the desired speed. The trends of voltage scaling in three different design targets of over the period of 15 years as predicted by International Technology Roadmap for Semiconductors (ITRS) . The low power digital circuits have the lowest supply voltage. In some applications, such as biomedical devices and sensor networks, low power design is the main concern while the speed has a secondary importance. Sub-threshold design as a very promising method for ultra-low power applications has been widely used until now. Since the maximum achievable speed in the circuits that are designed in the sub-threshold area is limited, these circuits are used in ultra-low power applications that need low to medium speed. The supply voltage in this area is below the threshold voltage of transistors (V_{dd}<Vth). Since the threshold voltage changes in different design technology, the operating region of a transistor in sub-threshold designs is not fixed. Operating current in the sub threshold region is the leakage current, which is significantly smaller than the operating current in the super-threshold area, and as such the speed in the sub-threshold designs is lower. Sub-threshold area in digital designs is defined as a region where the gate source voltage of all transistors is below the threshold voltage while the drain current remains positive. SAR as a digital part of the SA-ADC will be designed in a sub-threshold region to reduce the power consumption of the entire ADC.

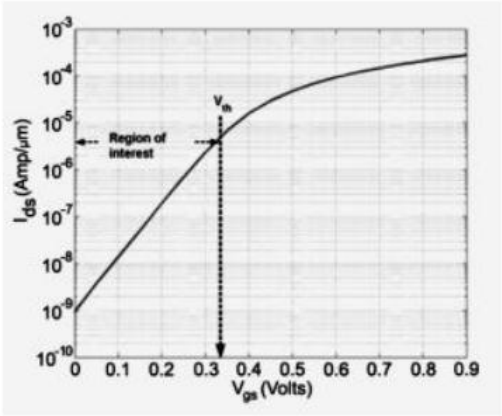
2.2. Leakage Power Reduction

With technology scaling, there should be a tradeoff between the switching speed and leakage power consumption. For the purpose of lowering the power consumption, the main strategy is to reduce the supply voltage which leads in an undesirable speed reduction. To compensate for the speed reduction, one way is reducing the threshold voltage which increases the leakage current and therefore the leakage power is increased. Other techniques such as dual-threshold voltage schemes, sleep transistors, body biasing, and clock gating may compensate for this increase in the leakage power consumption. The leakage current in digital designs increases exponentially as the threshold voltage decreases, where Vs. is the gate-source voltage, VDS is the drain-source voltage, Vth is the threshold voltage, n is the sub-threshold slope Coefficient which depends on the fabrication process and has a value between 1.3 and 1.5 in new CMOS processes.

$$I_{sub} = I_0 e^{\frac{V_{gs}-V_{th}}{n.V_T}}$$

The current I0 is shown in below eq, where μ0 is the Carrier mobility, Cox is the gate oxide capacitance, $_{Vt\ is}$ the thermal voltage (V_t≈26 mv at 300K), and W/L is the aspect ratio of the transistor.

$$I_0 = \mu_0 C_{ox} \frac{W}{L} (n-1) {V_T}^2$$



Region of operation of digital sub-threshold logic.

In dual threshold voltage design techniques, critical paths of the circuit that have a main effect on the circuit speed are implemented with the nominal (lower) threshold voltage devices while higher threshold voltage devices are used in non-critical paths. The problem with this technique is that it causes delays between different parts of the design. In sleep transistor techniques, extra transistors are used to connect the circuit to the supply voltage and ground, thus providing virtual supply and ground for the circuit. These transistors disconnect the circuit from the supply lines when the circuit is not in an active mode which precludes the direct leakage current between the power supply lines and ground lines. In clock gating techniques, the clock signal is Deactivated when the system is in standby mode. In addition, if a digital element in the circuit is inactive. for a while (i.e., its output is not used by other logic gates), the clock signal provide to the input of the element is deactivated through an additional digital gate. The power consumption of the clock circuitry is usually 30-35% of the power consumption of the entire system [4]. It should be noted that the digital circuits used to gate the clock should require a small amount of power to make this technique efficient. Usually, AND gates or OR gates are used to gate the clock in practice; however, other gates such as XOR gates may be used with equal success.

III. Low Power SAR Design

Recently, most research has focused on increasing the sampling rate and bit resolution in analog to digital converters, however in some applications such as biomedical devices ultra-low power design is desired. Successive Approximation Analog-to-Digital Converter (SA-ADC) has been widely used for its low power consumption in these particular applications. In an SA-ADC structure, the output of the comparator has to be sampled by SAR, thus for an SA-ADC with N bit resolution, N registers are needed. As mentioned before, with technology scaling the leakage power is increased and the power consumption of the digital part of the circuit will be comparable to the total power consumption.

3.1. SAR Structure: System Level

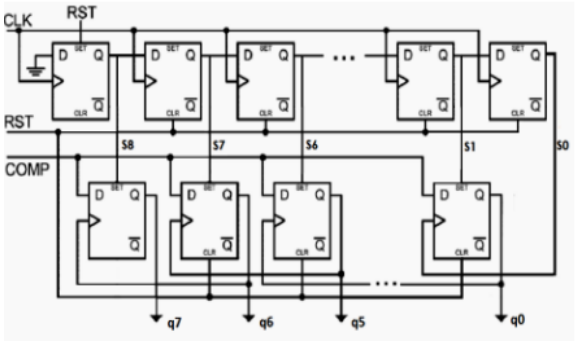
So far, two different structures have been proposed for SAR. One is the Sequencer Code register structure and the other one is non-redundant SAR. Both are composed of a particular number of registers to determine and save the value of the bits in a digital word produced by SA-ADC. In this work, these two structures with the goal of reducing their power consumption are considered. Both of these structures work based on the binary search algorithm. At the beginning (initial time t0), the first register which is responsible for determining the value of the Most Significant Bit (MSB) is set to '1', and puts its value on a bus. The value after converting to its analog equivalent goes to a comparator to be compared with the sampled input of SA-ADC. The output of the comparator works as a control bus to determine whether the MSB should be left as '1' or if it should be reset to '0' (during time t 1). Then, the second register is also set to '1' during time t 1and the same procedure is repeated. Therefore each flip flop is active only for two clock pulses in each conversion. These registers are in an order from the Most Significant Bit to the Least Significant Bit and after the bit value is determined, this value is saved in its related register.

3.1.1. Sequencer Code Register Structure

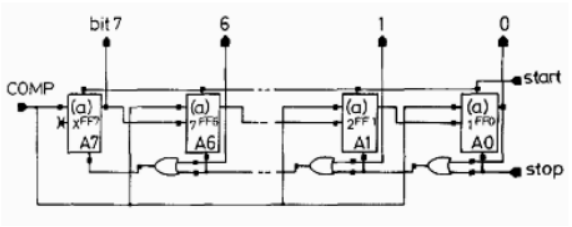
This structure has two sets of registers. The set of sequencer registers is in charge of providing the sequence and the registers of code register section are responsible for saving the value of bits. To reduce the delay, the non-inverted outputs of the shift registers in the sequencer circuit are used to set the registers of the code register circuit.

3.1.2. Non-Redundant SAR Structure

The non-redundant SAR structure has a lower number of registers than sequencer/code register structures. It only has N shift registers for an SAADC with N bit resolution and thus the leakage power is reduced with respect to the other SAR structure. This means that each shift register in the non-redundant structure is responsible for both determining and saving the bit values. The non-redundant structure. In this structure, at the beginning of the conversion (similar to the sequencer/code register structure) it is assumed that the MSB is set to '1' and other bits are set to '0', and this digital word is applied to the D/A converter to convert to an equivalent analog signal (0.5 Vref). This value is then compared to the sampled input signal. Based on the output of the comparator the value of the MSB is decided and this procedure is repeated for all other bits. However, to reduce the number of clock cycles, instead of loading '1' in each shift register, '1' is shifted in the shift registers. Each shift register has three modes of operation .



Sequencer/Code register structure with lower delay



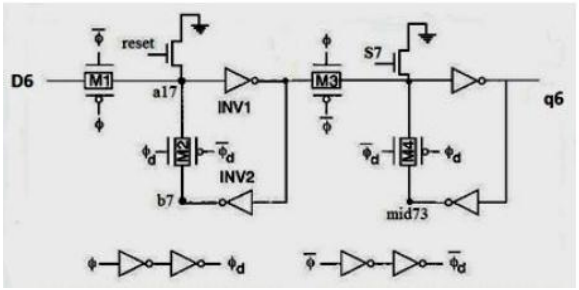
Non-redundant SAR structure

Shift mode: '1' from the shift register for higher bit values is shifted to the next shift register and '0' is shifted through other shift registers. The outputs of the shift registers are called q7, q6… q0 from MSB to LSB respectively. Data load mode: in this mode, based on the output of the comparator, the value of the related bit is determined. Memorization mode: In this mode, the value of the bit which has been decided by the output of the comparator is stored. For choosing the proper mode, a decoder and a multiplexer are used for each register to convert it to a shift register.

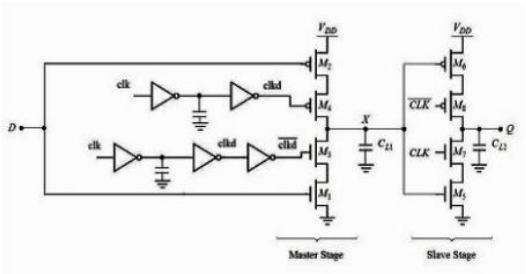
3.2. SAR Structure: Circuit Level

In this work, static and dynamic registers have been used for both structures and benefits and weaknesses of each of them have been considered. This register is sensitive to the positive edge of the clock. It should be noted that the clock signal has to be slow enough to allow sufficient set up time for the register. Otherwise, the register may not work properly. The dynamic register which is used for the purpose of comparison. It should be noted that the important issue with this dynamic register is the clock overlap problem. This problem may cause a direct path between the 'D' input and 'Q' output of the register and thus the performance of the circuit may be affected by this overlap. This overlap causes the voltage drop at the output of the registers. To solve the clock overlap problem, a buffered clock is used in the master stage. A level restorer can also be used at the output of the dynamic register. As mentioned before, clock gating is one of the techniques to reduce the power consumption of a system. In the sequencer/code register structure, the clock design in the code register circuits is such that the power is obviously saved. In

addition, only two clock pulses are needed for each shift register in the sequencer circuit, i.e. the output of each shift register after shifting the '1' to the next shift register remains '0' up to the end of the conversion. Therefore, after the decision for bit value of the related register in the code register has been finalized, no permanent clock is needed for the shift register in the sequencer/code register circuit. However, applying only two clock pulses to the shift registers in the sequencer/code register structure may cause a timing problem. To solve this problem, a buffer insertion is needed which imposes additional power consumption to the system. Hence, the clock gating is not a useful technique to reduce the power of the sequencer/code register structure (i.e., this technique may need complicated logics to save the power). Dual threshold technique as another common method in reducing the power consumption of a digital system is not suitable for the sequencer/code register implementations either since it may cause undesired delays.



Static register circuit



Dynamic register circuit

IV. Results

The power consumptions of the two SAR structures operating at different frequencies are shown in TABLE I and II. As a comparison between the two structures, the non-redundant structure has lower power consumption than the sequencer/code register structure due to a lower number of registers and reduced leakage power. As opposed to the sequencer/code register structure, the non-redundant SAR structure is less sensitive to the timing problems and thus the clock gating and dual threshold techniques have a significant role in reducing the power. The result of applying leakage reduction techniques to the non-redundant structure is shown in TABLE III. Applying the low power techniques has resulted in a power reduction of 69% at10 kHz, 41% at100 kHz and 44.6% at 1 MHz In ultra-low power applications in which the speed is the secondary important goal of the design, supply voltage reduction (especially sub-threshold design) is a significant method of power reduction. In the 130nm TSMC technology used in all circuit level simulations in this work, the threshold voltage of the normal oxide NMOS transistor is 0.326 V. It should be noted that in ultra-low voltage applications, since the Drain Induced Barrier Lowering (DIBL) effect is reduced, the threshold voltage is increased. TABLE IV illustrates the power consumption of the two SAR structures operating in the sub threshold regime and the results of applying a combination of the sub-threshold operating method with other low power techniques such as clock gating and dual threshold for non-redundant structure is drawn in TABLE V. As it comes through the TABLE V the power consumption of the non redundant structure is reduced by 76.8% at 100 kHz clock frequency as opposed to non-optimized case.

Table I: Power consumption of the sequencer/code register structure at different operating frequencies

Register Structure	Power Consumption(Frequency) (W)		
	P(10KHz)	P(100KHz)	P(1MHz)
Dynamic	-	6.7615E-07	8.0675E-07
Static	1.00475E-07	1.0669E-07	3.35815E-07

Table II: Power consumption of the non-redundant structure at different operating frequencies

Register Structure	Power Consumption(Frequency) (W)		
	P(10KHz)	P(100KHz)	P(1MHz)
Dynamic	-	1.8679E-07	3.85255E-07
Static	2.95605E-08	4.13525E-08	3.18615E-07

Table III: Power consumption in non-redundant structure at different operating frequencies after applying leakage reduction techniques

Techniques	Power Consumption(Frequency) (W)		
	P(10KHz)	P(100KHz)	P(1MHz)
Clock-gating	1.3545E-08	2.90235E-08	1.83575E-07
Dual threshold	8.719E-09	2.6917E-08	2.08615E-07
Clock-gating + Dual threshold	9.122E-09	2.4366E-08	1.7639E-07
Without any power reduction technique	2.95605E-08	4.13525E-08	3.18615E-07

Table IV: Comparison of power consumption in two SAR structures in different frequencies in sub-threshold region

Structure	Power Consumption(Frequency) (W)		
	P(10KHz)	P(100KHz)	P(1MHz)
Sequencer/Code register (Dynamic register)	—	—	—
Sequencer/Code register (Static register)	4.5036E-09	1.1179E-08	6.4302E-08
Non-redundant (Dynamic register)	6.2688E-09	1.4031E-08	—
Non-redundant (Static register)	5.7858E-09	1.2213E-08	8.1093E-08

Table V: Power consumption in non-redundant structure at different operating frequencies after applying low power techniques in combination with the sub-threshold design methods

Techniques	Power Consumption(Frequency)		
	P(10KHz)	P(100KHz)	P(1MHz)
Clock-gating	6.2751E-09	1.1711E-08	6.7062E-08
Dual threshold	3.8373E-09	1.0563E-08	—
Clock-gating + Dual threshold	4.0584E-09	9.5964E-09	—

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