NBTI and Process Variation Circuit Design Using Adaptive Body Biasing

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Abstract: VLSI circuits are increasingly affected by process variations as well as aging effects has become inevitable. Overcoming the variations inevitably requires additional power expense, which in turn aggravates the power and heat problem. The IC designed without consideration of process variation fails to do operation correctly Numbers of techniques has proposed to mitigate the effect of process and NBTI effect but have limitation Adaptive Body Bias technique is proposed which mitigate the effect of NBTI and process variation. **Index Terms:** Adaptive Body Bias (ABB), Forward Body Bias (FBB), Negative Bias Temperature Instability (NBTI), Process Variation, VLSI.

I. Introduction

AS VLSI technology scales, manufacturing process variations and aging effects [2] cause remarkable uncertainty, which must be considered in designs. A straightforward approach for this ABB is considered. To increase the chip density the size of the transistor has to be scale down which causes process variation. The process variation become severe as technology is scaled.Process variation occurs due to the limitation of fabrication process.

A.Process Variations

As technology scales further we will face new challenges, such as variability, single-event upsets (soft errors), and device (transistor performance) degradation as technology scaling continues, the impact of these issues increases, and we need to devise techniques to effectively deal with them.[3]

B. Source of Variation

There are three major sources that cause variations in transistor behaviour. The first source is called random dopant fluctuations, which results from discreteness of dopant atoms in the channel of a transistor. Transistor channels are doped with dopant atoms to control their threshold voltage. The decrease in transistor size each technology generation reduces its area by half, and thus the number of dopant atoms in the channel decreases exponentially over generations.

C. NBTI

In particular, temporal reliability issue NBTI is the primary reliability concern for Nano-scale transistors. NBTI is a result of continuous trap generation in Si-SiO2 interface of pMOS transistors. In bulk-MOSFETs, dangling Si bonds exists due to structural mismatch at the Si-SiO2 interface which acts as charged interfacial traps[1].

II. Proposed Adaptive Body Bias Circuit

Lot of research has been done to overcome the effect of process variation at different level of abstraction. Numbers of techniques has proposed to mitigate the effect of process and NBTI effect but have limitation. Here we will be focus about body biasing techniques. Adaptive body bias (ABB) permits the alteration of the transistor threshold voltage by governing the transistor body-to-source voltage. [4]

A forward body bias (FBB) (i.e.,VSB>0) reduces threshold voltage Vt, increasing the device speed at the expense of increased leakage power. Alternatively, a reverse body bias (RBB) (i.e.,VSB<0) increases, reducing the leakage power but slowing the device [4]. Therefore, the effect of process variations is mitigated by ABB circuit. A novel direct ABB (D-ABB) circuit is proposed. It is based on estimation circuits and direct adaptive control of the body bias, accomplished by an controller circuit. This goal is achieved by using a direct controller circuit which exhibit slow area overhead compared to other ABB circuits

In the proposed D-ABB circuit Fig 1, the effect of NBTI on VTP is compensated by estimating the actual value of VTP, which is impacted by NBTI, by using an estimation circuit. Then, the analog controller generates the appropriate body-bias voltage VSB, to mitigate the NBTI impact. The analog controller is a direct implementation of the relationship between VTP and VSB for a pMOS transistor is given by

 $|VTP| = |Vtpo| + \Delta |Vt|_{BB}$

And Δ | Vtp | _{BB}= $\gamma [(\phi F - VSB)^{\frac{1}{2}} - (2\phi F)^{\frac{1}{2}}]$ (1)

Where $|V_{\text{tp}}|$ is the pMOS transistor threshold voltage at zero body bias (i.e., when $V_{\text{SB}} = 0$), $\Delta |V_{\text{tp}}|_{\text{BB}}$ is the body-bias effect on $|V_{\text{TP}}|$, γ is the body effect coefficient, and ϕF is the Fermi potential with respect to the midgap in the Body.



A. Sensing Circuit

The sensing circuit for the pMOS transistor shown in Fig 2, this is used to estimate the actual value of pMOS transistor threshold voltage. In this circuit, the pMOS transistor is sized with the same sizing as the pMOS transistor in the test circuit and then MOS transistor is a native transistor[5], by using the α power law model, introduced in, and equating the dc currents of the nMOS and pMOS transistors, The output voltage of Sensing circuit, Vout, is expressed as

The output voltage of Sensing circuit, Vout, is expressed as Vout= Vtn+r (VDD - |Vtpstressed|) (2) \approx r (VDD - |Vtpstressed|) (3) $\swarrow v_{out} = r(v_{DD} - v_{tpst})$

B. Amplifier Circuit

For D-ABB circuit is shown in Fig.1, several amplifiers with various gains and a large output voltage swing is required. Therefore, the two-stage configuration amplifier circuit, shown in Fig.3, is used. The advantage of this configuration is that it isolates the gain and the output voltage swing requirements. The first stage is configured in a differential pair topology to provide the high gain requirements. Naturally, the second stage is configured as a common source stage to allow maximum output voltage swings [6]. Assuming that the following transistors pairs, (NM1 and NM2), (PM1 and PM2) and (NM3and NM5) are matched. The mismatch between these transistors threshold voltages is inversely proportional to the square root of the channel area (WL).

Fig. 2 Sensing circuit



Fig.3 Proposed Amplifier Circuit

C. Squaring Circuit

One of the essential building blocks in the ABB circuit, is the squaring circuit. Several squaring circuits are reported in the literature. Fig.4 depicts the squaring circuit used in the proposed ABB circuit. The proposed squaring circuit a utilized to adjust the squaring circuit output voltage dc offset and the squaring circuit gain. Assuming long channel transistor operation, all transistors are operating in the pinch-off saturation region, and the transistors (PM6 and PM7), (PM9, PM10), PM11, and PM12), (PM1, PM3, and PM4), (NM2 and NM3), and (NM1 and NM4), are matched. The small signal current flowing through PM6 is gm6Vin/2 that is equal to the small signal current flowing through NM3, which is gm9Vo1/2 due to the current mirror action between these transistors.

Therefore, Vo1 = (gm1/gm6)Vin. (4)



III. NBTI-induced PMOS Transistor Aging.

Transistors age over time this can have significant impact on performance of future circuits. NBTI is a dominant aging mechanism causing PMOS threshold voltage degradation over time, resulting in degraded drive current and increased delay.

IV. Sensor Design for Transistor Aging Failure Prediction

Our sensor design approach is to modify a standard latch or flip-flop by inserting a "monitoring" circuit block which detects any 'significant' shifts in delay of the combinational logic whose output is connected to the data input of that latch or flipflop. Here, we focus on rising-edge-triggered flip-flopbased designs – however, the presented techniques are applicable for falling-edge-triggered flip-flops and latches as well. The monitoring circuit block is based on the concept of *stability checking* during the guardband interval by detecting signal transitions during the guardband interval, also referred to as *guardband violation*. Figure 5, illustrates this point[7].

Guardband violation at the combinational logic output means that the combinational logic input stimulus exercises one or more paths that have aged enough to creep into the guardband interval and is now very close to turning into a delay fault. Note that, the flip-flop will still continue to capture correct logic values from the combinational logic – that is the basic difference from error detection. Figure 6 shows the block diagram of a design consisting of a flip-flop with a built-in aging sensor. An aging sensor integrated inside a flip-flop has three components: a stability checker (Fig.7), a delay element to create an interval during which stability checking is performed (Fig.8), and an output latch to store stability checking results. Details of each aging sensor component are discussed later in this section. The delay element and the output latch may be shared among multiple flip-flops for power and area savings. Depending on how scan flip-flops are designed, it may be possible to reuse the scan portion of a design for the output latch (e.g., utilizing 3-latch or 4-latch scan flip-flop designs[8]

Figure 7 shows the design of a stability checker and Fig.9 shows the corresponding waveforms. In the beginning of a clock cycle when Clock = 1 (i.e., $Clock_b = 0$), PMOS transistors T1 and T5 in Fig. 7 are on (NMOS transistors T3 and T7 are off), and the stability checker output Out = 0. This is called the *precharge phase* of the stability checker. The delay element (*Delay*) in Fig.7 (and shown in detail in Fig.8) introduces a delay of 'Tclk/2 – Tg' (assuming 50% duty cycle of *Clock*). Here, Tg is the guardband interval (Fig.5). This guarantees that transistors T3 and T4 (and transistors T7 and T8) are both on during the guardband interval Tg (called the *evaluate phase*). During the guardband interval, PMOS transistors T1 and T5 are turned off. Stability Checker output *Out* becomes 1 if and only if the combinational logic output *OUT* transitions from 1 to 0 or 0 to 1 once or multiple times during the guardband interval, i.e., the guardband is violated.

The output latch in Fig.6 is responsible for holding the state of the sensor output whenever the stability checker catches any guardband violation (i.e., stability checker output is 1). Example waveforms are shown in Fig.9 For the presented technique to work for NBTI-induced PMOS aging, it is critical that the performance of the aging sensor itself does not degrade significantly due to PMOS transistor aging. Degradation of PMOS transistors T1 and T5 is not a major concern because the precharge phase, when T1 and T5 affect the performance of the stability checker (i.e., when Out is precharged to 0), is generally sufficiently long.

Design of an aging resistant delay element is shown in Fig.8 Since NBTI-induced PMOS aging is a slow process, aging sensors can be turned off most of the time to ensure that they do not age significantly. This requires an additional slow global input signal, Monitor in Fig.8 This signal may be derived from the scan enable signal. When *Monitor* = 1, aging monitoring is turned on and the delay element outputs a delayed version of $Clock_b$. When Monitor = 0, aging monitoring is turned off and the delay element produces 1. Turning aging monitoring off also reduces power consumption of the delay element. However, we must ensure that the sourcegate junctions of all PMOS transistors used in generating the guardband interval must not be forward biased when aging monitoring is turned off. The aging resistant delay element design in Fig.8 accomplishes this in the following way discussed next. When Monitor = 1, aging monitoring is turned on and the series of NAND gates (G2,G3,G4) introduce the delay required to produce a delayed version of $Clock_b$. When Monitor = 0, each NAND gate (G2, G3, G4) produces a 1 at its output irrespective of the other input signal. As a result, the corresponding PMOS transistor in the following NAND gate that this output is connected to is off and doesn't age. Note that, the PMOS transistor in a NAND gate connected to the Monitor signal continues to age. However, this PMOS transistor will not affect the delay of the circuit path which produces *delayed Clock_b* since it is in parallel to the other PMOS transistor which is off when Monitor = 0.













Fig 7 Aging resistant Stability Checker design.



To prevent aging of the first PMOS transistor connected to the clock input of the delay element, we use a NOR gate (G1) instead of NAND. The PMOS transistor inside G1 connected to the *Clock* input is off (and does not age) when *Monitor* = 0. This NOR gate inverts *Clock* to generate *Clock_b* when *Monitor* = 1, and produces 0 when *Monitor* = 0. The NOR gate output cannot be directly connected to the input of NAND gate G2 because the corresponding PMOS transistor on the circuit path producing *delayed Clock_b* will age when *Monitor* = 0. Instead, the output of G1 is connected to an inverter formed out of T11 and T13. When *Monitor* = 0, T10 and T12, in series with T11, are turned off ensuring that T11 does not age. When *Monitor* = 0, T13 is off and T14 is on producing 1 at the input of G2. This ensures that the PMOS transistor of G2 connected to the circuit path producing *delayed Clock_b* does not age when *Monitor* = 0.

V. Simulation Result And Discussion

Tanner 14.1 tool is used to draw schematic and to simulate the proposed design. Schematic of the proposed ABB circuit and Sensor Design for Transistor Aging Failure Prediction is drawn and the simulation results of the circuits are shown.

The Circuit design, generate the body bias voltage required to compensate the effect of change in threshold voltage due to NBTI or process variations.





Fig 11.Squaring Circuit



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D-ABB Circuit: Finally all the block of the D-ABB circuit when combined produces body bias voltage



Fig 13.D-ABB Circuit

Waveform and Transient Analysis of D-ABB.

Waveform:



Sensor Design for Transistor Aging Failure Prediction circuit: Schematic and Waveform of Aging resistant delay element design:





VI. Conclusion

In this paper we have implemented adaptive body bias technique to mitigate the effect of NBTI and process variation. The simulation result shows that proposed method compensate the change in threshold voltage due to process variation/NBTI. The proposed technique alleviates effect of process and NBTI at run time with small area overhead compared to the existing techniques. Sensor Design for Transistor Aging Failure Prediction circuit is useful to prevent the circuit from aging. Future Work will also include to use D –ABB and Sensor Design for Transistor Aging Failure Prediction circuit to prevent the circuit from aging.

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