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A Novel Switched Capacitor Technique for NBTI Tolerant Low Power 6T-SRAM Cell Design

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Abstract : *The work in this paper is focused on designing a NBTI tolerant 6T SRAM cell while maintaining low power operation. We explore the usefulness of switched capacitor circuit to provide NBTI tolerance while reducing overall power consumption. A thorough analysis of the 6T SRAM cell has been done to show the reduction in power consumption of the cell without degrading the read and write stability. The results obtained in proposed technique are compared and contrasted with reported data for the validation of our approach. The proposed technique reduces read power by 32%, write power by 15% and leakage power by 14%. The applied technique effectively reduces overall current by considerable amount and also significant reduction in Vth degradation due to NBTI is observed hence it is suitable for NBTI tolerant low power 6T SRAM cell design.*

Keywords: *NBTI, Low Power, 6T SRAM cell, Switched capacitor, SNM.*

I. Introduction

As the circuit complexity of day to day applications is increasing at a rapid speed, memory is emerging as the most important factor in deciding the performance of any system. Larger the memory available better will be the performance. The modern video processors have to do a lot of complex computations which can be done at faster rate if more memory is available. The processing speed of a processor is often limited by the amount of cache being used, thus more and more memory need to be added on a single chip to improve system performance, but at the same time it has been found that most of the power is being dissipated by the memory alone. Most of the times the power consumed by the memory becomes more than the logic circuit present on the chip. Thus memories have become the epicenter of power consumption in modern systems [1].

On the other side the trend of reducing the transistor feature size continues, process variation in devices has made it very difficult to reduce the cell area at 50% rate. Among the entire different device variations Negative Bias Temperature Instability (NBTI) is found to affect the device reliability more severely and thus in recent years have become major reliability issue for the semiconductor industry. NBTI impact is getting worse in each technology generation with greater performance and reliability loss. Register's and caches which are SRAM cells, are also much severely affected due to the NBTI aging. If an SRAM cell stores same value for a large period of time it goes through high amount of stress, thus reducing its reliability characteristics which will in return result in a loss of the stored data. Therefore, register files and caches have become more prone to failures due to NBTI. Remaining part of the paper is arranged as follows, section-2 gives a brief about basic 6T SRAM cell operation, section-3 describes the proposed technique in detail, the obtained results are discussed in section-4, and section-5 concludes the paper.

II. Sram Review

SRAM has been the core area of study since decades and many techniques have been continuously developed to meet the power requirements. In reported paper [2] authors have discussed sleep stack technique wherein multiple cell voltages have been used to reduce the leakage power. Careful selection of cell voltages reduces the leakage current up to a certain extent, also in [15] dynamic voltage scaling been discussed which says that during a fixed period of time the activity in a cache is only centered on a small subset of the lines. This behavior has been exploited to cut the leakage power of large caches by putting the cold cache lines into a state preserving low-power drowsy mode but Moving lines into and out of drowsy state incurs a slight performance loss [13].

Today, SRAM cell needs to be designed not only with minimum area or high density but with as less power consumption as possible. Thus main focus in this research work is to reduce the overall power consumption of the SRAM cell. The proposed technique uses the switched capacitors to accumulate the charge flowing in the circuit during read and write cycles and when sufficient amount of charge is accumulated the SRAM is feed through the Switched capacitors instead of VDD, thus reusing the accumulated charge.

2.1 SRAM 6T cell Basic operations

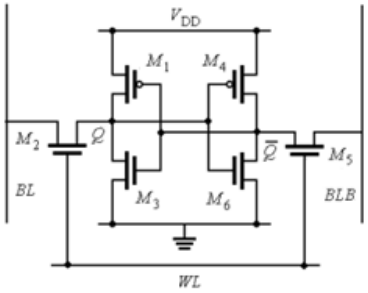


Figure 1: 6T SRAM Cell

Standby operation: When WL=0, M2 and M5 disconnect the cell from Bitlines. The two cross-coupled inverters formed by M1-M3 and M4-M6 will continue to reinforce each other as long as they are disconnected from bitlines.

Read operation: **R**ead-1 cycle starts with pre-charging BL and BL to 1. Within the memory cell M1 and M6 are ON. Asserting the word line, turns ON M2 and M5 and the values of Q and QB are transferred to Bit-Lines (BL and BLB). No current flows through M2, thus M1 and M2 pull BL up to VDD that is BL=1.BLB discharges through M5 and M6.

Write operation: The value to be written is applied to the Bit lines. Thus to write data 0, we assert BL=0, BLB = 1 and to write data 1, the BL = 1, BLB = 0, asserted when WL = 1.

2.2 Switched Capacitor: A switched capacitor is electronic circuit which works by moving charges into and out of capacitors when switches are opened and closed. Usually, non-overlapping signals are used to control the switches, so that not all switches are closed simultaneously [9]. The switched capacitor diagram is as shown in Figure 2.

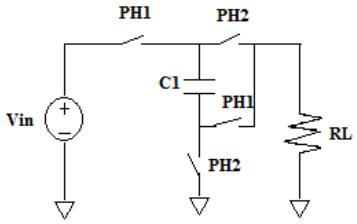


Figure 2: Switched Capacitor

During phase-1(PH-1), capacitor C1 is connected between the input node Vin and the output resistor RL. The charge flows from Vin goes though C1 and finally reaches the load resistor RL thus the capacitor gets charged up during phase-1. In phase-2(PH-2) C1 is connected between RL and GND, and hence now the charge stored previously on capacitor C1 drives the load resistor RL.

III. Proposed Technique

3.1 Proposed SRAM with Switched Capacitor

In the proposed technique the switched capacitor is connected in between the SRAM cell and the ground terminal. So that the charge flowing during read and write cycles would otherwise flow directly to the ground will now flow through the switched capacitor. As a result the capacitor will get charged and when a sufficient charge is accumulated this switched capacitor will replace the supply voltage VDD and will drive the SRAM cell. SRAM with switched capacitor is shown in Figure 3. Thus as shown in Figure 3, during phase-1 switches PH-1 will be turned on and the cell is operating at VDD=1V, and also the switched capacitor will get charged during this phase.

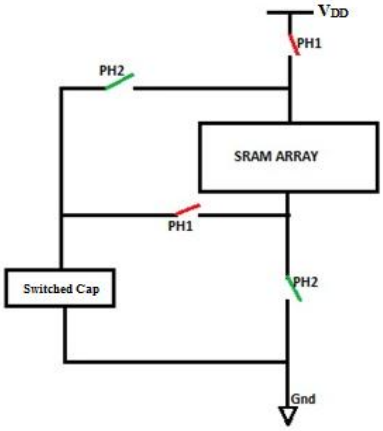


Figure 3: SRAM with switched capacitor

Phase-2 starts as soon as sufficient charge is accumulated and a sufficient voltage is obtained across the switched capacitor. Thus turning ON switches PH-2, now the switched capacitor circuit will drive the SRAM cell during idle state. Now in the idle state the SRAM is operating on voltage that is generated from the charge that would have been wasted in case switched capacitors were not used.

3.2 Switched capacitor design:

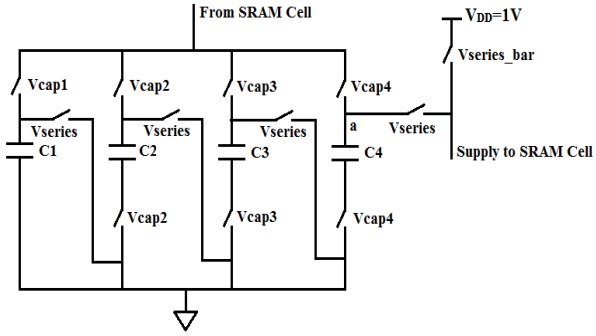


Figure 4: Switched Capacitor Arrangement

Initially Vseries is OFF, at the same time Vseries_bar is in ON condition, thus SRAM cell gets power from VDD. Now at this point Vcap1 is turned on therefore the read or write current depending on SRAM operation flows through SRAM Cell passes through capacitor C1 resulting in rise in capacitor voltage up to 0.2V. As soon as the capacitor voltage reaches 0.2V Vcap1 is turned OFF and Vcap2 is turns ON thus now charging capacitor C2. This will continue till all four capacitors get charged. As soon as voltage across the fourth capacitor C4 reaches 0.2V, Vseries is turned ON resulting in connection of all the capacitors in series thus adding the potential across each one of them. If the switches are assumed to be ideal the total potential at point 'a' will be 0.8V. But due to the drop across the transistors the voltage obtained at this point is 0.6V. Now the switched capacitor is ready to drive the SRAM Cell, so Vseries is turned ON, the capacitors get connected in series and now whenever the Cell goes in idle state the switched capacitor will drive the cell instead of VDD and the potential at terminals Q if it stores '1' will be 0.6V instead of 1V. Thus reducing the standby power by 14.6%.

IV. Results And Discussion

The simulations were done at 65nm technology with VDD=1V and Vth=0.36V. As can be seen in Figure 5(a)-(d) the capacitors c1-c4 gets charged to a voltage of 0.2V. Figure 6(b) shows the series signal which connects the capacitors in series and also disconnects the cell from the VDD and drives the cell during idle state. Figure 6(c) clearly shows when Vseries is ON the cell goes into idle state and V(Q) falls to 0.6V which is supplied from the switched capacitor, thus reducing leakage current.

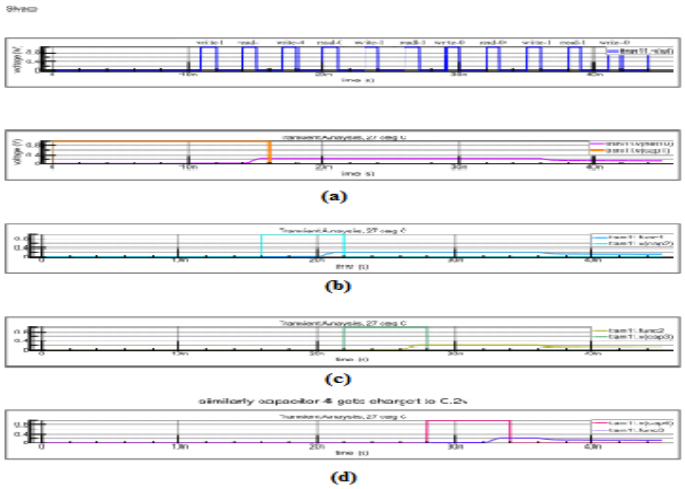


Figure 5 : Charging of capacitors during read and write operations

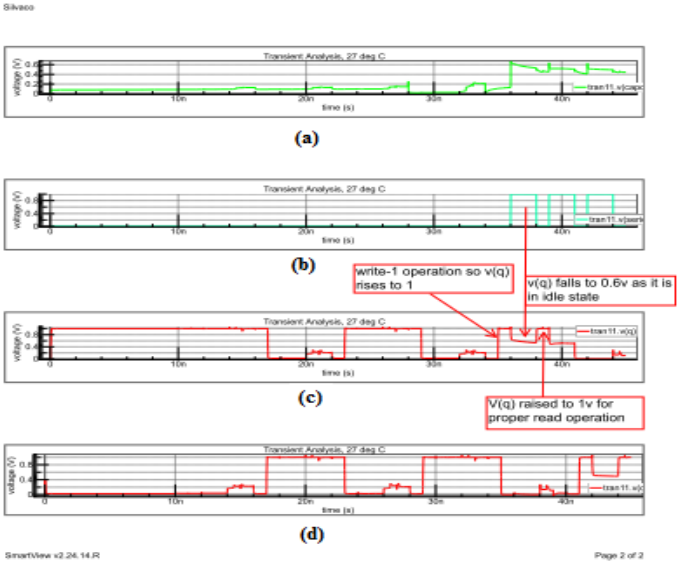
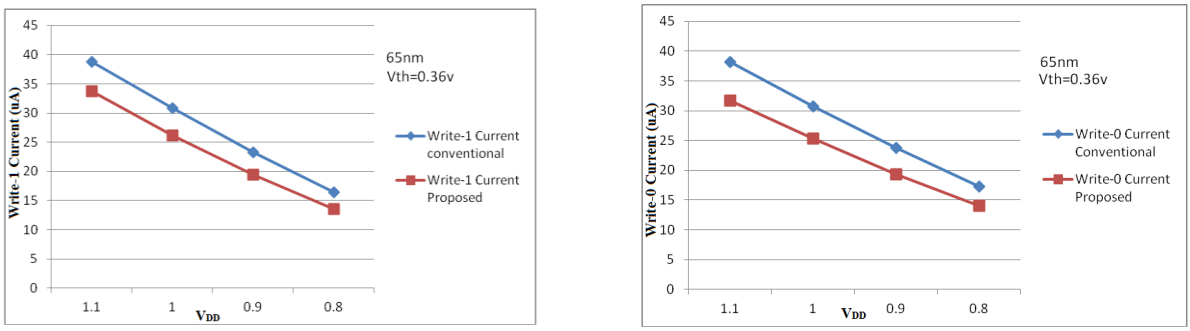


Figure 6 : Switched capacitor drives the cell in idle state

4.1. Read, Write and Leakage current:

Figure 7 (a) and (b) shows the comparison of write-1 and write-0 currents in conventional SRAM cell and Cell with switched capacitor circuit respectively,as the supply voltage reduces the drain to source voltage reduces which results in reduction of the write current as can be observed in these Figure 7.



(a) (b)

Figure 7 : Comparing (a) write-1 current (b) write-0 current in conventional SRAM Cell and Cell with switched capacitor

Figure 8(a) and (b) shows the variation of read current and leakage current as supply voltage is reduced from 1.1V to 0.8V in both the conventional SRAM cell and cell with switched capacitor, as expected the read current and leakage current falls as the supply voltage is reduced,also the plot of the read current in proposed technique is always lower than that of a conventional SRAM cell.

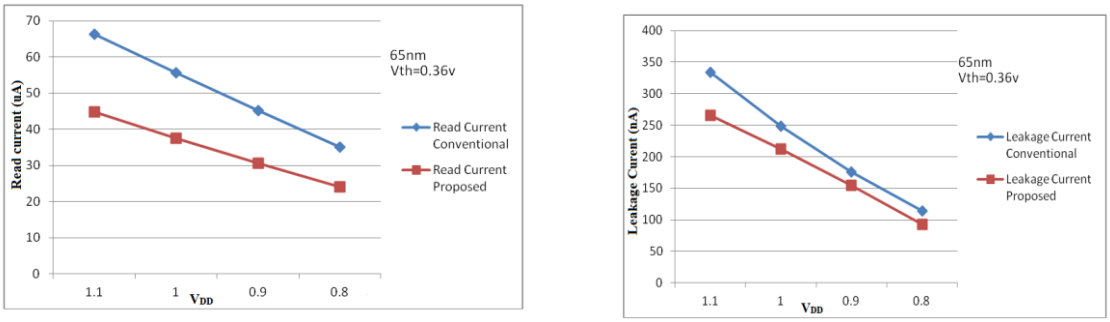


Figure 8 : Comparing (a) Read current (b) Leakage current in conventional SRAM Cell and Cell with switched capacitor

4.2. Stability :

Noise Margin (NM) is the maximum spurious signal that can be accepted by the device when used in a system while still maintaining the correct operation [7].the proposed technique tends to rise the source potential of the NMOS transistor of the cell and as stated in [1] source biasing tends to reduce the read noise margin thus it becomes necessary to test the cell for the stability. As shown in Figure 9(a) and (b) the static noise margin is 0.24v for the conventional SRAM cell and same for cell with switched capacitor circuit, thus proving that there is no effect on the SNM of the cell due to applied technique, also shown in Figure 10(a) and (b) is the read noise margin which is 0.1v for both the conventional SRAM cell and cell with switched capacitor.

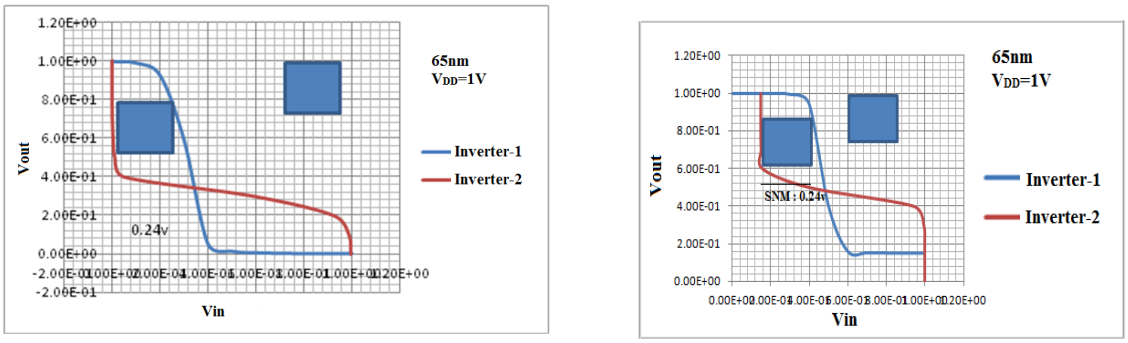
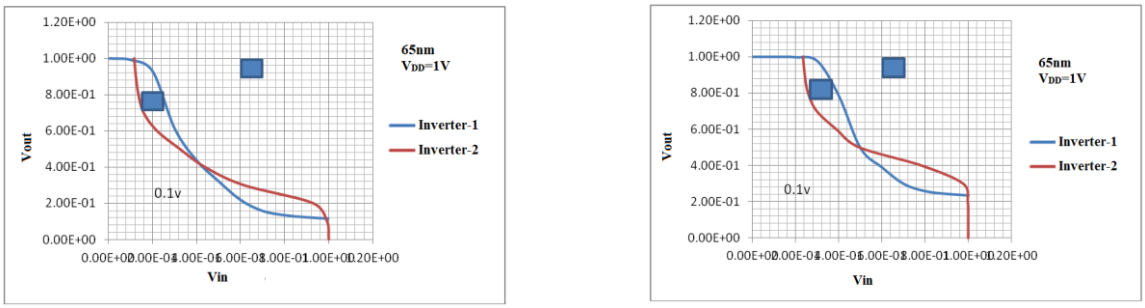


Figure 9: SNM of (a)Conventional 6T SRAM cell (b) 6T SRAM cell with switched capacitor



(a) (b)

Figure 10: Read Noise margin for (a) Conventional 6T SRAM cell (b) for 6T SRAM Cell with Switched Capacitor.

Table 1 shows the read write and leakage currents at VDD=1v,which shows a reduction of 15.24% in write-1 current 17.7% in write-1 current,32.48% in read current and 14.6% in leakage current.

Table 1: Comparing various current's in Conventional SRAM Cell and SRAM cell with proposed technique.

65nm,V_{DD}=1V, Vth=0.36V	Write-1(uA)	Write-0(uA)	Read(uA)	Leakage(nA)
Conventional SRAM	30.83	30.7	55.57	249.01
Proposed Technique	26.13	25.26	37.52	212.57
% Improvements	15.24%	17.7%	32.48%	14.6%

4.3. NBTI Analysis

It can be observed in Figure 11 in conventional SRAM cell the stress on transistor 4 during write-1 and read-1 cycle is 0V for 6ns similarly in write-0 and read-0 cycles the stress is 1V for 9ns and in idle phase the stress is 1V for 3ns,it means out of total 15ns of operation transistor-4 will face a stress voltage of 0V for 40% of time and a stress voltage of 1V for remaining 60%,now if we observe same conditions in proposed technique we can see that for first 6ns the stress on transistor is 0V but in the next 3ns as the switched capacitor gets charged the potential at Q terminal rises to 0.2V instead of 0V thus reducing the stress voltage on transistor-4 to 0.8V,now when the cell goes in the idle state unlike conventional cell the proposed cell is driven by the switched capacitor replacing the supply voltage of 1V by the switched capacitor voltage of 0.65V,thus again reducing the stress voltage to 0.65V instead of 1V thus now of the total 15ns of time the time for which the stress voltage is 1V is reduced to 20%(3ns/15ns) of total time and stress voltage is 0.8V for 20%(3ns/15ns) similarly 0.67V for 20%(3ns/15ns) and 0V for 40%. Thus the stress is reduced from 1V for 60% of total time to 1V for 20% time 0.8V and 0.65V for 20% each, thus reducing the Vth degradation.

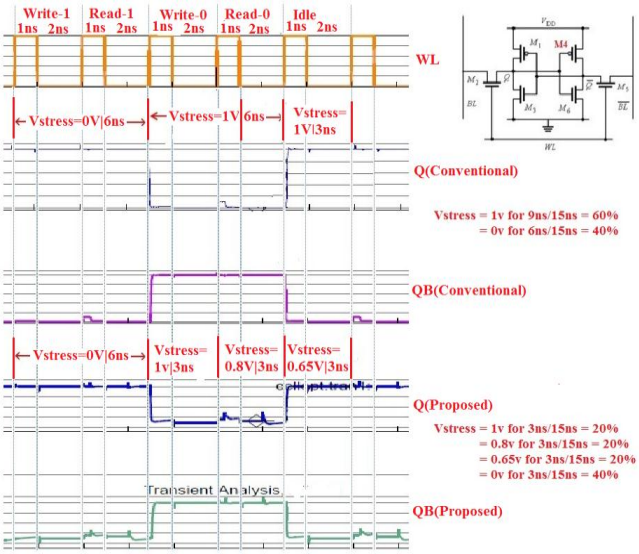


Figure 11 : Stress time for conventional and proposed SRAM cell.

Figure 12(a) shows the degradation in threshold voltage Vth with increasing temperature. As the temperature increases the bonds break more easily and the NBTI effect worsens seen in Figure 12(a).The effect of stress voltage over the Threshold voltage degradation is shown in Figure 12(v) which shows increasing rate of degradation due to increased level of stress.

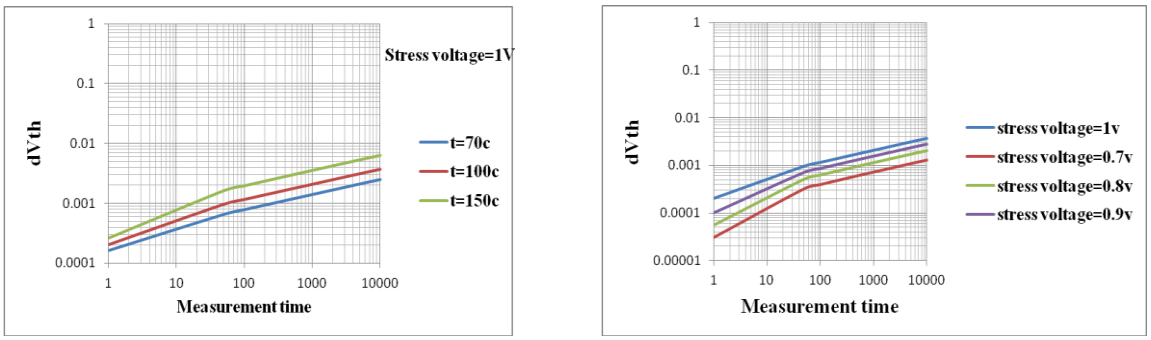


Figure 12 : dvth vs time at (a) Different temperatures (b) Different stress voltages

Figure 13(a) shows the degradation in threshold voltage in the proposed technique, as discussed above the stress voltage over the two PMOS devices is continuously 1V for 60% of total time in conventional cell whereas in proposed technique the stress reduces to 0.8V for 20% of the time and again when the cell goes to idle phase the stress is reduced to 0.65V,these phases can be clearly observed in Figure 13(a) where the curve is continuously increasing when the stress is 1V starts decreasing when the stress is 0.8V and again decreases further when the stress is 0.67V.

It is quite clear from Figure 13(b) the difference in the rate of degradation of the two PMOS devices in conventional cell and the proposed cell, the upper curve shows the rate of degradation in conventional SRAM cell, as the stress is continuously 1V the curve is also increasing continuously, whereas in the proposed technique the stress reduces from 1V to 0.8V to 0.67V as explained above thus resulting in less rate of degradation.

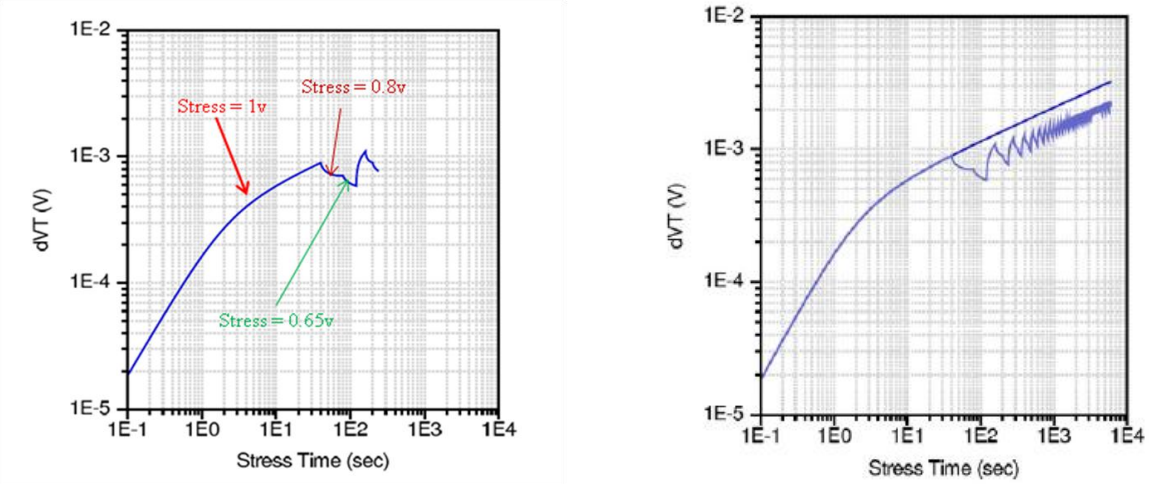


Figure 13 : (a) dvth vs time in proposed technique (b) Vth variation in conventional SRAM cell and Proposed SRAM cell

Table 2 shows the comparison of degradation in threshold voltage after 6000sec, in conventional SRAM cell where the degradation is 3.23mV that in proposed technique it is reduced to 2.10mV, thus proving the effectiveness of the proposed technique in mitigating NBTI effects.

Table 2: Comparison of rate of degradation in conventional SRAM cell and proposed SRAM cell

	240s	6000s
dV_{th} in conventional SRAM cell	1.4mV	3.23mV
dV_{th} in proposed cell	0.76mV	2.10mV

V. Conclusion

A novel switched capacitor based SRAM Cell is proposed in this research work. A thorough power analysis of the cell indicates a significant reduction in overall power consumption of the cell. It can be seen from the obtained results that the proposed technique reduces the Read power by 32% write power by 15% and leakage by 14% without affecting the stability of the cell even during standby mode. Also from the stability analysis it can be observed that even though the source potential is raised there is negligible variation in stability. The basic idea to provide NBTI tolerance is that if the stress is reduced the rate of Vth degradation also reduces thus as the switched capacitor is connected between the cell and the ground terminal, as the capacitors gets charged the source potential raises thus reducing the stress on both the PMOS devices, also when the cell goes to standby mode the switched capacitor circuit charged to a potential of 0.65V will drive the cell, further reducing the stress. The effect can be seen in the results obtained. The degradation in threshold voltage observed in conventional cell after 6000sec is found to be 3.23mV whereas in the proposed technique the same reduces to 2.10mV. Thus the switched capacitor technique is found to be very effective in mitigating NBTI effects while maintaining low power operation in 6T-SRAM cell. Hence, the proposed SRAM cell is suitable for low power applications in hand held devices.

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