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Power Efficient adder Cell For Low Power Bio MedicalDevices

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Abstract: *In this paper a new design of full adder cell based on Sense Energy Recovery concept using novel exclusive NOR gates is presented. Low-power consumption and delay are targeted in implementation of our design. The circuit designed is optimized for low power at 0.18-µm and 0.09 µm CMOS process technologies in full custom environment. The new circuit has been compared to the existing work based on power consumption, speed and power delay product (PDP). Cadence simulations show that the proposed adder can work more reliably at different range of supply voltage over a frequency of ranges. The Simulations carried out showed that the proposed adder design has 37.3% power savings capability over conventional 28-T CMOS adder at 200 MHz for a supply voltage of 1.1V with negligible area overhead. The proposed design has been used as the basic building block for column compression Dadda multipliers (CCDM) and found to be working successfully with high energy efficiency.*

Keywords: *Column compression, full adder, low power, multipliers, SERF, TG Adder, VLSI circuit.*

I. INTRODUCTION

1.1 Low Power Addition

The addition of two binary numbers is fundamental in various circuits especially circuits used for performing arithmetic operations like multiplication and division, compressors, comparators and parity checkers. There is no ideal adder cell that can be used by all types of applications. Therefore, many different circuits for binary addition have been proposed over the last decades [1, 2, 3, 4], covering a wide range of performance characteristics to satisfy the constraints enforced by different applications. Design of digital integrated circuits for many applications relies on three major criteria: low power consumption, small chip area, and high speed. Demand and popularity of portable electronics is driving the designers to strive for smaller area, higher speed of operation, longer battery life and more reliability [3]. Power is one of the premium resources a designer tries to save when designing a system. The battery technology doesn't advance at the same rate as the IC technology. The goal to extend the battery life span of portable electronics is to reduce the energy consumed per arithmetic operation. Enhancing the performance of the adder units can significantly improve the system performance. Therefore careful design and analysis is required for these units to obtain optimum performance. [7] .Lowering the supply voltage and reducing the number of transistors of bit adder design is a proper method for lower power consumption. Using lower number of transistors to implement a logic function is beneficial in reducing the device and interconnect parasitic and reducing the chip area, resulting in lower time delay and potentially lower power consumption. However, many low-number-transistor adders do not operate correctly at low supply voltage in 0.18µm and subsequent CMOS technologies due to threshold voltage (Vt) loss problem. The goal of this work is to design a full adder that works successfully at ultra-low supply voltage, avoids any degradation on the output voltage, and has less delay in critical path with lower number of transistors. These low power arithmetic modules are embedded into digital signal processors for wearable and implantable bio medical devices. The rest of this paper is organized as follows: in Section 2 we present and analyze the proposed 1-bit full-adder cell. Simulation setup and results are described in Section 3. Section 4 concludes the paper.

II. THE PROPOSED ADDER CELL

The total power dissipated in a generic digital CMOS gate is given by Eq. (1).

$$P_{total} = P_{dynamic} + P_{short-circuit} + P_{static} \quad (1)$$

$$= V_{dd}.\ F_{clk}\Sigma_i V_{iswing}.C_{i\ load}.\alpha_i + V_{DD}.\Sigma_i I_{sc} + V_{dd}.I_{leakage}$$

Where F_{clk} denotes the system clock frequency, V_i swing is the voltage swing at node i equal to V_{DD}, Ci load is the load capacitance at node i, α_i is the activity factor at node i, and I_{sc} and leakage are the short circuit and leakage currents, respectively. Switching power is power consumed in charging and discharging of the circuit node capacitances during transistor switching, short circuit power dissipation occurs because of the short circuit current flowing from power supply to ground during transistor switching and static

power is due to leakage and static currents flowing while the circuit is in the stable state. The first two components of the equation are referred to as dynamic power which constitutes the majority of the power dissipated in CMOS VLSI circuits. [9].

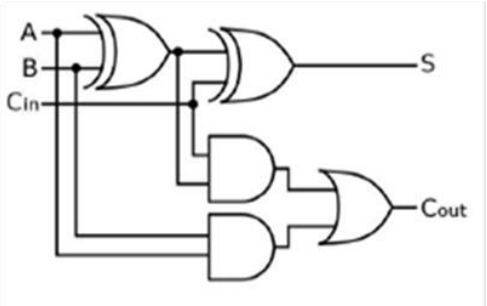

Figure 1: Symbol of conventional CMOS Full Adder [4]

The complementary CMOS full adder circuit was designed using 28 transistors. This adder was based on regular CMOS structure (pull-up and pull-down network). [8].One of the most significant advantages of this full adder was its high noise margins and thus reliable operation at low voltages. The layout construction of CMOS gates was also simplified due to the complementary transistor pairs. But the use of substantial number of transistors results in more power consumption, larger area and high input loads. Also the serially connected transistors in the output stage gave rise to relatively weak output driving capability that made the circuit unreliable if we are required to use them in cascade. The TG based full adders, Mux based adders existing in literature were also considered for comparison of performance evaluation. [9 ,12].

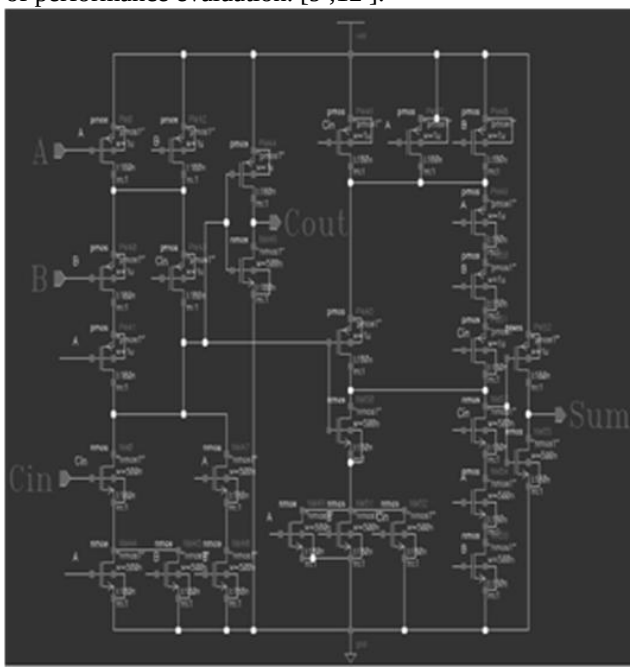

Figure 2: Schematic of 28 T full adder

The second class of adders considered for analysis was energy recovery adders. The Static Energy Recovery Full Adder [10,11] SERF adder circuit consists of two XNORs realized by 4 transistors. Energy recovering logic reuses the charge and therefore consumes lower power than non-energy recovering logic. The charge applied to the load capacitance during the logic high level is drained to ground during the logic low level in non-energy recovering logic . An energy recovering logic reuses this charge, which charges the load capacitance during the logic high to drive the gates rather than draining the charge to ground To illustrate static energy recovery concept let us consider an example where initially A=B=0 and then A changes to 1. Let us consider that there is a capacitor at the output node of the first XNOR module. When A and B both equals to zero the capacitor is charged by VDD. In the next stage when B reaches a high voltage level keeping A fixed at a low voltage level, the capacitor discharges through A and certain amount of charge is retained in A. Hence when A reaches a high logic level it need not be charged fully. Also it cannot be cascaded at low power supply due to multiple threshold problems. The SERF Full adder is as shown in the below fig 3 [10], which does not operate reliably and is confronted

with serious problems especially at lower supplies.

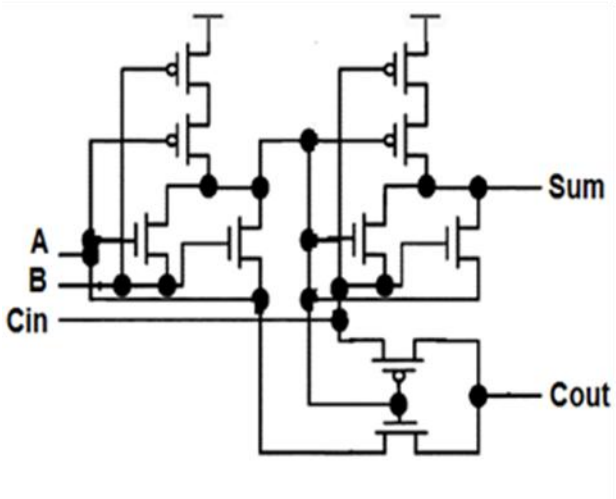

Figure 3: Schematic of SERF FA [10]

There are two possible solutions to improve the operation of the SERF circuit. The first one is connecting the output of XNOR gate (first stage) to V_{DD} instead of V_{DD}-V_{th} (when the output of XNOR gate is high) and modifying Cout to be connected to V_{DD} instead of V_{DD}-V_{th} or V_{DD}-2V_{th}. The modified version of SERF [10, 11] circuit as shown in the fig 3, it makes use of Pass transistors at the Summation stage and output reaches only to Vt, since the pass-transistor logic has an inherent threshold voltage drop problem. The output is a weak logic "1" when "1" is passed through an nMOS and is a weak logic "0" when "0" is passed through a pMOS. At the carry out stage, it loses its signal strength as shown from analysis.

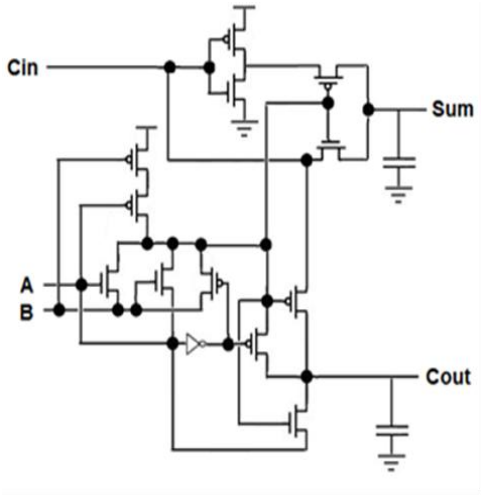

Figure 4: Modified SERF Full Adder [11]

The proposed Low power Full adder is based on the static energy recovery concept [10] [11] and uses the novel XNOR circuit and the Transmission Gate based MUX along with level restoring clock gating technique for its operation. The use of properly sized transistor and transmission gate stages instead of the pass transistor will give better performance and avoids the threshold voltage drop problem along with reliable operation. It is also important to know that the power reduction is not just a problem of number of transistors. The Sum is generated from the output of the second stage XNOR circuit, i.e. Sum = (A XNOR B) XNOR C_{in}. The C_{out} is calculated by multiplexing A &C_{in} controlled by (A $\oplus$ B).Its low transistor count results in switched capacitance reduction and the capability of working at ultra-low supply voltage. Operating properly at lower supply voltage range without threshold voltage loss, with TG and PT based XNOR gates along with AND gating technique makes it a good choice for low power environment. [12, 13] .

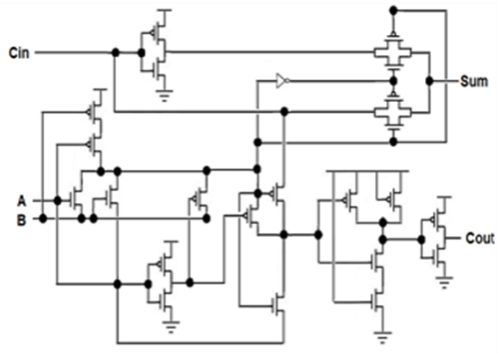

Figure 5: Proposed Full Adder

The new design is robust against supply voltage variation without any modification in transistor's threshold voltage at high supply voltage. It benefits from good drivability so it can be cascaded easily when used with 32 0r 64 bit multipliers. This good driving strength in cascading makes the proposed adder a better alternative for the full adders in tree based multipliers using column compression of partial products in any signal processors.

III. Simulation

The standards of today's technology require three main parameters to measure performance: Power, Delay, and Size. The power delay product (PDP) is also a quantitative measure of the efficiency and a compromise between power dissipation and speed. The Circuit Simulation of this paper were carried out using numerous random input vectors with SPECTRE simulator in CADENCE VIRTUOSO Analog Design Environment under CADENCE CMOS 90nm Technology. The Simulation Setup is shown in the Fig 6. The Simulations were conducted at different frequencies, i.e 5MHz, 50MHz, 100MHz, and 200MHz for different supply voltages ranging from 0.7V to 1.5V. The Power, Delay and Power-delay product of the various full adder designs are listed in the Table 1 for comparison. Table 2 gives the analysis carried out at various frequencies.

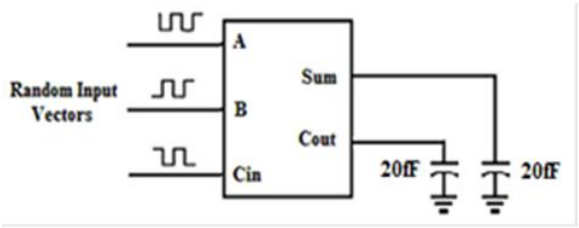

Figure 6: Simulation test bench

Fig. 6 shows the simulation test-bench. It has been made of three cascaded adder cells. The inputs are fed from the buffers (two cascaded inverters) to give more realistic input signals and the outputs are loaded with buffers to give proper loading condition. In order to establish an impartial simulation environment, we preferred to give the input patterns as shown in Fig. 7, which covers every possible input combination of A, B, and C_{in} pulses of amplitude vs time . Power consumption and working speed (frequency and delay) are standard measures for the performance of CMOS circuits

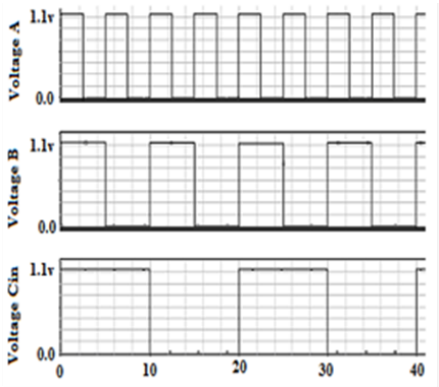

Figure.7. Simulation input patterns

.The delay is calculated from 50% of voltage level of input to 50% of voltage level of resulting output for both rise and fall output transitions. For the calculation of the power delay product, worst-case delay is chosen to be the larger delay amongst the two outputs. By optimizing the transistor sizes of full adders considered, it is possible to reduce the delay of adders without significantly increasing the power consumption, and transistor sizes can be chosen to achieve minimum PDP. The proposed full adder design of Fig. 5 has been compared with static CMOS, TG adder [9], mux based [12] adder cells existing in literature. The Tables 1-3 show the results of simulation carried out for total power consumption and delay at 100 MHz for various supply voltages for all full adder designs for 90nm and 180nm libraries provided by Cadence.

Table 1. Comparison of power consumption (µw)vs. supply voltage 100MHz)

C-CMOS	6.0119	6.0012	6.0116	6.0003	6.0041

V_{DD} (V)	0.7V	0.9V	1.1V	1.3V	1.5V
C-CMOS	2.5356	07.6888	27.3510	73.1727	152.772
O-TGA	4.2262	12.2117	31.0817	63.7167	110.935
MBA-12T	24.246	33.2585	41.7267	25.1693	23.4301
ULPFA	8.5851	19.2515	37.1811	62.7335	98.2891
Mfd SERF	21.1882	27.7734	66.2027	123.307	199.404
Proposed FA	**1.3119**	**3.4824**	**8.4722**	**17.9344**	**33.2452**

Table2. Delay (ns)vs. supply voltages

O-TGA	5.9512	5.9637	5.9651	5.9625	5.9612
MBA-12T	5.9925	6.0052	6.0135	6.0137	6.0125
ULPFA	5.8551	5.8452	5.8511	5.8667	5.8652
Mfd SERF	5.9751	6.0152	6.0104	6.0051	6.0013
Proposed FA	**6.0493**	**6.0451**	**6.0470**	**6.0162**	**6.0482**

Table 3. PDP (fJ) vs. supply voltage

C-CMOS	15.2437	46.1420	164.4232	439.0584	917.2581
O-TGA	25.1509	72.8269	185.4054	379.9108	661.3069
MBA-12T	145.297	199.723	250.9235	151.3606	140.8734
ULPFA	50.2666	112.528	217.5503	368.0386	576.4852
Mfd SERF	126.601	167.062	397.9047	740.4708	1196.683
Proposed FA	**7.9360**	**21.0514**	**51.2313**	**107.896**	**201.0724**

Table 4 shows the comparative analysis of the full adders for a range of frequencies at a supply voltage of VDD = 1.1v. From the analysis it is understood that the proposed adder shows an improvement of 37.3 % in terms of power saving compared with static CMOS full adder at 1.1v in 90 nm 200 MHz and 31.16 % improvement in terms of PDP at 100 MHz. Hence it can be inferred that this cell is a better alternative in low power domain.\

Table4. Comparison of power, delay, PDP vs. frequency (Vdd=1.1v)

FA Design	Power Consumption (µW)			
	5MHz	50MHz	100MHz	200MHz
C-CMOS	13.8921	20.1652	27.3511	41.3592
O-TGA	02.1537	15.9225	31.0817	61.3675
MBA-12T	0.05544	0.02568	0.04172	0.03006
ULPFA	02.6121	18.6812	37.1811	73.8528
Mfd SERF	67.1064	67.1059	66.2027	63.8629
Proposed FA	01.1823	04.4342	08.4722	15.4437
FA Design	Delay (nS)			
	5MHz	50MHz	100MHz	200MHz
C-CMOS	100.9999	11.0010	6.0112	3.5031
O-TGA	100.9551	10.9653	5.9652	3.4675
MBA-12T	101.0225	10.9902	6.0135	3.5095
ULPFA	100.8515	10.8551	5.8511	3.3526
Mfd SERF	101.0152	10.9998	6.0125	3.0501
Proposed FA	**101.0212**	**11.0425**	**6.0470**	**3.5467**
FA Design	Power Delay Product (fJ)			
	5MHz	50MHz	100MHz	200MHz
C-CMOS	1403.100	221.8373	164.4129	144.8854
O-TGA	217.4269	174.5949	185.4085	212.7918
MBA-12T	05.60061	0.282211	0.25088	0.105492
ULPFA	263.4342	202.7862	217.5503	247.5988
Mfd SERF	6778.766	738.1514	398.0437	194.7882
Proposed FA	**119.4373**	**048.9646**	**51.2313**	**054.7741**

Fig 8 shows the full custom handcrafted layout implementation of the proposed full adder using Cadence in 180 nm technology. The LVS was done and RC extraction was successfully implemented and GDS II file was extracted.

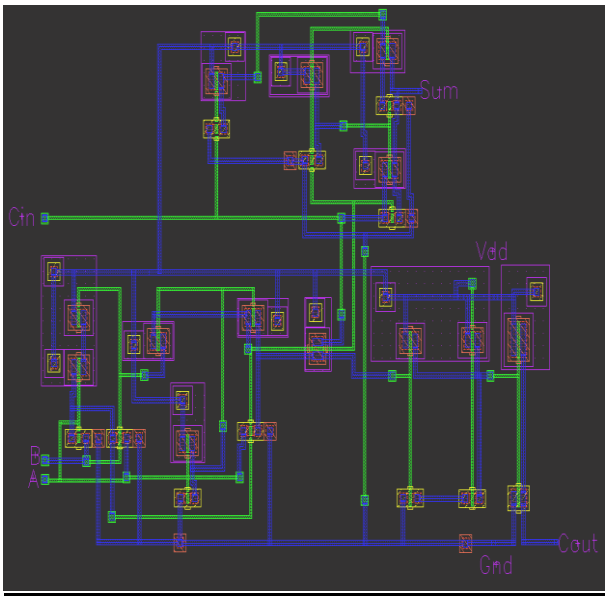

Figure. 8: The compact layout of the presented adder cell.

IV. Conclusion

A power efficient and ultra-low power 1-bit adder cell, using the low-number of-transistors was described, designed and simulated. It works based on XNOR function. Lowering transistor counts with pass transistor logic and clock gating make this design suitable to operate at low supply voltage. In

addition, some techniques to eliminate the direct path power consumption cause this new adder to benefit from the lower power dissipation and a better PDP than previous similar designs without any transistor threshold voltage modification. The circuit has high driving capability so it can be cascaded easily in large tree structured arithmetic circuits and compressor trees for multipliers. In this paper, we proposed a 24-transistor full-adder that is able to operate at 1.1 V power supply. The performance of various full-adders was compared and the simulation results proved that the proposed full-adder dissipates the lowest power and has lowest PDP (Power Delay Product). The simulation results demonstrate that the proposed full adder can be a better alternative for the low power applications and they can be used as a building block in compressor, multiplier and multiple and accumulate units that are used in DSP chips. [14]

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