# Design and Analysis of Low Power Comparator Using Switching Transistors

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Abstract: Comparator is one of the fundamental building blocks in most analog to digital converters. Many high speed analog to digital converters such as flash analog to digital converter require high speed and low power comparators. A new double tail comparator is designed, where the circuit of a conventional double tail comparator is modified for low power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors the positive feedback during the regeneration is strengthened which results in remarkably reduced delay time. Post layout simulation results in a 0.18 $\mu$ m technology confirm the analysis results. It is shown that in the switching transistors using dynamic comparator, both the power consumption and delay time are significantly reduced. Power consumption of conventional double tail comparator is 12 $\mu$ W in 0.8 $\nu$  and power is reduced to 9.5 $\mu$ W in double tail comparator using switching transistors with the same supply voltage.

*Keywords:* Double tail comparator, dynamic clocked comparator, high speed analog to digital converters, low power analog design, switching transistor.

# I. INTRODUCTION

Dynamic latched comparators are very attractive for many applications such as high speed analog to digital converters (ADCs), memory sense amplifiers (SAs) and data receivers, due to fast speed, low power consumption, high input impedance and full swing output. They use positive feedback mechanism with one pair of back to back cross coupled inverters (latch) in order to convert a small input voltage difference to a full scale digital level in a short time [12].

A clocked comparator generally consists of two stages. In that first stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. In a CMOS based latch, the regenerative stage and its following stages consume low static power since the power ground path is switched off either by a NMOS or PMOS transistor.

High speed comparators in ultra-deep submicrometer (UDSM) CMOS technologies suffer from low supply voltages especially, when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. The general trend in CMOS technology is to make the devices smaller and smaller to increase the density and speed of digital circuits. Reduced power supply voltage is normally not an advantage for analog design and a low supply voltage may require some special circuit techniques.

The input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output-latch stage. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise [6]. The pre-amplifier based comparators suffer not only from large static power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain to source resistance due to the continuous technology scaling.

CMOS evolution has come to a point where for analog circuits new phenomena need to be taken into account. A major issue is the decreasing supply voltage. Although the supply voltage has dropped from 5 V in the early nineties down to 1.2 V today, most analog circuits can still be designed. However, a further drop in supply voltages is expected to cause serious roadblocks for analog circuits, because the signal headroom becomes too small to design circuits with sufficient signal integrity at reasonable power consumption levels. Although the analog transistor properties do not really get worse when comparing them at identical bias conditions, lower supply voltages require biasing at lower operating voltages which results in worse transistor properties, and hence yield circuits with lower performance. The second issue is gate leakage. Gate leakage will increase drastically when migrating to newer technologies. When the gate oxide thickness is reduced with the equivalent of one atomic layer, the gate current increases by approximately one order of magnitude. Despite technological remedies, gate leakage will become part of analog design-especially for long transistors; e.g., in 65 nm technology the current gain of a MOSFET will be as small as unity for a channel length of 30m.

In this paper a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double tail comparator.

The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative comparators and the pros and cons of structure is discussed. The double tail comparator is presented in Section III. Section IV discusses the double tail comparator using switching transistors. Simulation results are addressed in Section V, followed by conclusions in Section VI.



Fig. 1. Schematic diagram of single tail comparator.

# II. SINGLE TAIL COMPARATOR

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset [2], [11], and random decision errors [14], and kick-back noise [6]. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analysed, based on which the proposed comparator will be presented.

The schematic diagram of the conventional dynamic comparator widely used in analog to digital converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig.1. Comparator having two operation modes, the reset phase and the evaluation phase. The modes of operation depend on the clock input given. Clk = 0 known as reset phase and clk = Vdd known as evaluation phase. When clk = 0, nMOS transistor is in off and pMOS transistor is in on. When clk = Vdd, nMOS is in on and pMOS transistor is in off.

When clk = 0, the circuit is in reset phase, while Mtail is off. The reset transistors  $M_7$  and  $M_8$  became on. These reset transistors pull both output nodes Outn and Outp to Vdd. In the evaluation phase, clk = Vdd, reset transistors  $M_7$  and  $M_8$  became off and Mtail is on. Outn and Outp, which had been pre-charged to Vdd, start to discharge. Discharging rates are different depending on the corresponding input voltage INN and INP. Assuming the case where VINP > VINN, Outp discharges faster than Outn, hence Output voltages, which had been pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltages.

Assuming the case where  $V_{INP} > V_{INN}$ , Outp discharges faster than Outn, hence when Outp (discharged by transistor  $M_2$  drain current), falls down to Vdd–|Vthp|before Outn (discharged by transistor M1 drain current), the corresponding pMOS transistor will turn on initiating the latch regeneration. Thus, Outn pulls to Vdd and Outp discharges to ground. If  $V_{INP} < V_{INN}$ , Outn discharges faster than Outp and operations performed vice versa. Fig.2. represents the output waveform of single tail comparator.

The delay of this comparator is comprised of two time delays,  $t_0$  and  $t_{latch}$ . The delay  $t_0$  represents the capacitive discharge of the load capacitance until the first p-channel transistor (M5/M6) turns on. In case, the voltage at node INP is bigger than INN (i.e.,  $V_{INP} > V_{INN}$ ), the drain current of transistor M2 causes faster discharge of Outp node compared to the Outn node, which is driven by M1 with smaller current.



Fig.2. Output waveform of single tail comparator.caused by back-to-back inverters (M3, M5 and M4, M6).

Single tail structure has the advantages of high input impedance, rail to rail output swing, no static power consumption, and good robustness against noise and mismatch [7]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently reason is that, at the beginning of the decision, only transistors  $M_3$  and  $M_4$  of the latch contribute to the positive feedback until the voltage level small enough to turn on transistor  $M_5$  or  $M_6$ , to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate source voltage for transistors  $M_3$  and  $M_4$ , where the gate source voltage M5 and M6 is also small. Thus the delay time of the latch becomes large due to lower transconductances.

The disadvantage of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval, a large tail current would be desirable to enable fast regeneration in the latch. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favourable for regeneration.

#### III. DOUBLE TAIL DYNAMIC COMPARATOR

Fig. 3 demonstrates the schematic diagram of the double tail comparator. Double tail architecture has two tail transistors. Double tail comparator is used for low power applications. In this technique, increase the voltage difference between the output nodes in order to increase the latch regeneration speed. For this purpose, two control transistors have been added to the first stage in parallel to  $M_3$  and  $M_4$  transistors but in a cross-coupled manner. Double tail comparator has two operation modes, the reset phase and the decision making phase. The modes of operation depend on the clock input given. Clk = 0 known as reset phase and clk = Vdd known as evaluation phase. When clk = 0, nMOS transistor is in off and pMOS transistor is in on. When clk = Vdd, nMOS is in on and pMOS transistor is in off.



Fig. 3. Schematic diagram of the double tail dynamic comparator.

The operation of the proposed comparator is as follows. When clk = 0, the reset phase, both the tail transistors Mtail1 and Mtail2 are in off to avoiding static power. Transistor  $M_3$  and  $M_4$  are in on.  $M_3$  and  $M_4$  pulls both fn and fp nodes to Vdd, hence transistor MC1 and MC2 are cut off. The circuit has two intermediate stage transistors MR1 and MR2. These transistors reset both latch outputs to ground.

During decision-making phase, clk = Vdd, both the tail transistors are on,  $M_3$  and  $M_4$  transistors are off. At the beginning of this phase, the control transistors MC1 and Mc2 are still off (since fn and fp are about Vdd). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose  $V_{INP} > V_{INN}$ , thus fn drops faster than fp, (since  $M_2$  provides more current than  $M_1$ ). As long as fn continues falling, the corresponding pMOS control transistor (MC1 in this case) starts to turn on, pulling fp node back to the Vdd, so another control transistor remains off, allowing fn to be discharged completely. Fig.4 represents the output waveform of double tail comparator.

When one of the control transistors turns on, a current from Vdd is drawn to the ground via input and tail transistor (ie, MC1, M1, and Mtail1) result in static power consumption. To overcome this issue, two nMOS switches are used below the input transistors such asMsw1 and Msw2. At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre-charged to Vdd (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn or fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the Vdd and fn should be discharged completely, hence the switch in the charging path of fp will be opened, but the other switch connected to fn will be closed to allow



Fig. 4. Output waveform of the double tail dynamic comparator with INN=0.7V and INP=0.5V.

the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

### IV. DOUBLE TAIL COMPARATOR USING SWITCHING TRANSISTORS

Fig.5 shows the schematic diagram of the double tail comparator using switching transistors. Due to the better performance of double tail architecture in low voltage applications the comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase  $\Delta V fn/fp$  in order to increase the latch regeneration speed. Two more transistor connected below the Msw1 and Msw2, which is used for switching.

## A. Operation of the Comparator using Switching Transistor

The operation of the proposed comparator is as follows in fig.5. During reset phase, clk = 0, tail transistors are off to avoiding static power,  $M_3$  and  $M_4$  pulls both fn and fp nodes to Vdd, hence transistor MC1 and MC2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision making phase clk = Vdd, both the tail transistors are on, transistors  $M_3$  and  $M_4$  are turn off. At the beginning of this phase, the control transistors are still off, since fn and fp are about Vdd. Thus, fn and fp start to drop with different rates according to the input voltages. Suppose  $V_{INP} > V_{INN}$ , thus fn drops faster than fp, since  $M_2$ provides more current than M<sub>1</sub>. As long as fn continues falling, the corresponding pMOS control transistor ,MC1 in this case, starts to turn on, pulling fp node back to the Vdd, so another control transistor (MC2) remains off, allowing fn to be discharged completely. In other words, unlike conventional double tail dynamic comparator, in which  $\Delta V fn/fp$  is just a function of input transistor transconductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node in discharges faster, a pMOS transistor turns on, pulling the other node fp back to the Vdd. Therefore by the time passing, the difference between fn and fp ( $\Delta V fn/fp$ ) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors turns on, a current from Vdd is drawn to the ground via input and tail transistor, resulting in static power consumption. To overcome this issue, four nMOS switches are used below the input transistors such as Msw1, Msw2, Msw3 and Msw4.



Fig. 5. Schematic diagram of the power gated double tail comparator.



Fig. 6. Output waveform of the power gated double tail comparator with INN=0.7V and INP=0.5V.

At the beginning of the decision making phase, due to the fact that both fn and fp nodes have been pre charged to Vdd (during the reset phase), both switches are closed and fn and fp start to drop with different discharging rates. As soon as the comparator detects that one of the fn/fp nodes is discharging faster, control transistors will act in a way to increase their voltage difference. Suppose that fp is pulling up to the Vdd and fn should be discharged completely, hence the switch in the charging path of fp will be opened (in order to prevent any current drawn from VDD) but the other switch connected to fn will be closed to allow the complete discharge of fn node. In other words, the operation of the control transistors with the switches emulates the operation of the latch.

# **B.** Delay Analysis

The dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference  $(\Delta V_0)$  at the beginning of the regeneration  $(t = t_0)$ ; and second, it enhances the effective transconductace of the latch.

1)Effect of Enhancing  $\Delta V0$ :  $t_0$  is a time after which latch regeneration starts. In other words,  $t_0$  is considered to be the time it takes until the first nMOS transistor of the back to back inverters turns on, so that it will pull down one of the outputs and regeneration will commence. The latch output voltage difference at time  $t_0$ , ( $\Delta V_0$ ) has a considerable impact on the latch regeneration time, such that bigger  $\Delta V_0$  results in less regeneration time.

2) Effect of Enhancing Latch Effective Transconductance: In conventional double-tail comparator, both fn and fp nodes will be finally discharged completely. The fact that one of the first stage output nodes (fn/fp) will charge up back to the Vdd at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective transconductance of the latch is increased. In other words, positive feedback is strengthened, which strengthen the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of Vth/Vdd, the transconductance of the transistors decreases, thus the existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator.

3) Reducing the Energy per Comparison: In conventional double-tail topology, both fn and fp nodes discharge to the ground during the decision making phase and each time during the reset phase they should be pulled up back to the Vdd. However, in our proposed comparator, only one of the mentioned nodes (fn/fp) has to be

charged during the reset phase. This is due to the fact that during the previous decision making phase, based on the status of control transistors, one of the nodes had not been discharged and thus less power is required.

COMPARATOR	POWER	DELAY
Single Tail Comparator	7μW	66ns
Double tail Comparator	12µW	7.4ns
Double tail comparator using switching transistors	9.5µW	0.94ns

Table 1. Comparison of Power and Delay of Various Comparators.

# **V. SIMULATION RESULTS**

In order to compare the proposed comparator with the conventional and single tail dynamic comparators, all circuits have been simulated in a 0.18-µm CMOS technology with Vdd = 0.8V. Single tail comparator consumes 7µW power and the delay is 66ns. For the modified double tail comparator the power is 15µW and delay is reduced to 7.5ns. In double tail comparator using switching transistor, power and delay are significantly reduced. The consumed power is  $9.5\mu$ W and delay is 0.94ns.

#### VI. CONCLUSION

In this paper, presented a comprehensive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-µm CMOS technology confirmed that the delay and energy per conversion of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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