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Memory less Rotation Based BIST with Low Area Overhead

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Abstract: *BIST is an efficient method for testing the circuits, area overhead is the main problem associated with BIST. Here we presents a deterministic BIST technique with low area overhead and that can provide complete fault coverage without using any storage devices. The test structure containing a circular shift register with some feedback from the CUT as its input, which provide all the required test patterns. It can provide 100% fault coverage for all testable stuck-at faults.*
Keywords: *BIST, Circular Shift Register, Circuit Under Test, Self Feedback Logic*

I. Introduction

Built-In Self-Test (BIST) is a self testing mechanism. That can be used to check the functionality of the device. It has been shown to be an effective design for testability (DFT) technique in which some on-chip test structure is used to test the digital circuit itself [5,10,12]. Pseudo-random testing based on linear feedback shift registers (LFSRs) is widely used because of its simplicity and effectiveness. However this mechanism fails when a complex circuit often contains some hard-to-detect faults. At this case pseudo random test scheme usually requires long test time to reach satisfactory fault coverage. To overcome this problem, so many techniques have been proposed. The weighted random test (which means that the primary inputs are given individual probabilities (weights) of being 1) method [5] is presented to enhance the detectability of hard-to-detect faults. This technique may require long test time when a circuit containing many hard-to-detect faults. The mixed-mode BIST technique[4-5] use the advantages of both pseudo random and deterministic patterns to achieve complete fault coverage in a small time. In *Mixed-mode testing* where the circuit is tested in two phases. A complicated control may be required to control the two test phases. In [2,4,6,8] another BIST methods they use simple control logic to generate only *deterministic patterns* without pseudo-random patterns. Twisted-ring counters (TRC) along with some reseeding logic are employed to generate all the required patterns. The required seed patterns are stored in an on-chip ROM. A large number of patterns are generated from a single seed pattern. So the number of seed required is reduced and the controlling complexity is also reduced. But this technique may require long test time to achieve complete fault coverage if the length of the TRC is large. A [7] partially rotational scan (PRS) register is used in a hybrid BIST. In this method a scan chain is divided into multiple segments, each of which can independently perform rotation operations. The required test patterns for complete fault coverage are generated based on some seed rotations. Since only shifting and rotation operations are needed, and the test control is also simple. It requires a long test time if the number of shifting and rotation operations is large. In circular self-test scheme [9, 11] each primary IO is replaced by a special BIST cell and the internal scan cells of the BIST cells are connected together to form a long circular self-test path. Only small area overhead is needed in this technique because both signature analysis and pattern generation can be done by the self-test path itself. However the fault coverage may be degraded if some states cannot be reached by the self-test path. Rotation based memory less BIST [1] consist of a self feedback loop along with the circular shift register, that provide all the required test patterns. Self feedback logic loop is a circuit that consists of large number of gates, hence area overhead is high.

All of the above methods except memory less BIST required either on-chip ROM or some external testers to provide the required seed patterns or some input patterns. This leads to an increase in area and the power consumption. In this work we propose a deterministic BIST scheme that requires no storage device with low area overhead and reduced power consumption. A Circular Shift Register (CSR) with some of the internal nets of the CUT as its input provides all the required test patterns. Here we tries to identify a set of internal nets from the CUT to provide the required logic values to the CSR, we develop an efficient method to generate effective test patterns (seeds) based on the current circuit responses. Experimental results show that our method can achieve complete stuck-at fault coverage using fewer test cycles than those in [2] and [5]. Comparison with the other techniques shows that we can use lower area overhead and comparable test time to reach complete fault coverage.

II. The Proposed BIST Architecture

The proposed BIST architecture consists of a circular shift register (CSR), internal feedback from CUT to the CSR, a response monitor and an on-chip BIST control unit as shown in fig 1. The CSR along with the internal nets of CUT are used to generate all the required test patterns, and the response monitor is employed to capture the test responses and compared with the stored response. The whole test procedure is controlled by the control unit. During test application, the pattern stored in the CSR is circularly shifted (rotated) by one bit per test cycle. If the length of the CSR is *n* then it can generate up to *n*-1 additional test patterns. However it should be noted that in our method full rotation is not always required for each pattern. Due to this novel feature, fewer test cycles are required than previous works [2-5]. The required initial patterns for the CSR can be generated by resetting the CUT. By resetting CUT we get some internal net responses that can apply to the CSR input. So the area overhead is minimum as compared with other techniques. The response monitor consists of a comparator. It captures the response of CUT and compared with the pre-stored results. If both are equal there is no error occurred otherwise a stuck-at fault occur. A control unit is used to control the whole procedure.

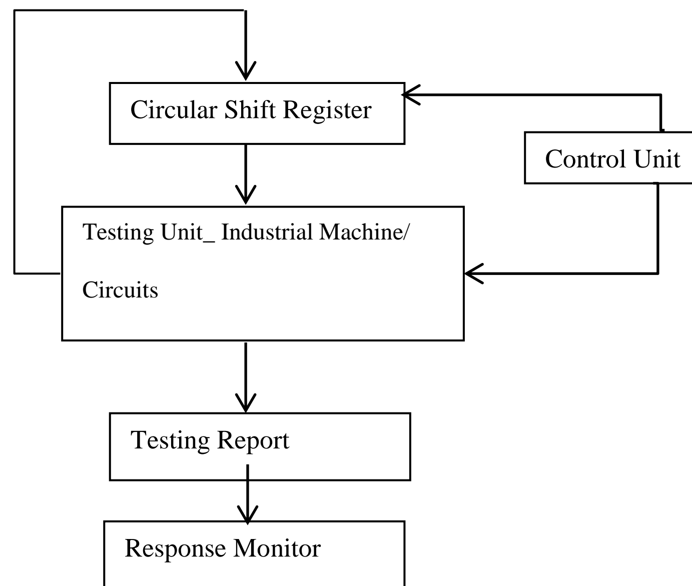


Fig 1: proposed BIST architecture

III. Test Generation And Pattern Determination

This section presents our method for test generation and pattern determination. The flow chart for test generation and pattern determination is shown in Fig 2. We consider pre-defined fault coverage for stopping the process. Initially a feedback pattern with full rotation is generated by resetting the CUT so as to detect maximum number of faults. Feedback pattern generates n-1 different patterns through CSR. A predefined fault coverage value will be used as a criterion to determine when to stop the process.

At first we use an all-zero pattern as the initial pattern to the CUT. The response of the internal nets of the CUT is added to the feedback pattern set and drop all faults detected by this pattern from the testable fault list *F*. Based on this pattern, we can build a special data structure called a *feedback binary tree* (FBT) is used to record the status of current available feedback candidates that can provide the required logic-0 and logic-1 values for the next feedback pattern. We will show an example in Figure 3 to illustrate how a FBT is constructed. Assume the CUT has 5 input pins {*I1*, *I2*, *I3*, *I4,I5*} and 5 internal nets {n1, n2, n3, n4,n5}. Internal nets are directly connected to the CSR input. After applying the all-zero pattern, the FBT is built in which the root is linked to the all-zero pattern and the two leaf nodes {Class0, Class1} are included the logic-0 and logic-1 values, respectively. Here the responses of the nets of n3, n4 and n5 are logic-0, so the Class0 node is linked to the set {*n3*, *n4, n5*}. Similarly the Class1 node is linked to the set {*n1*, *n2*}. Next we generate a partially specified test set (*S*) for all the remaining faults in *F*. This set is generated by using the feedback patterns to be generated in the following process. The number of patterns generated by the CSR is high. So we execute a *circular merge* process on *T1* to generate a set of compressed patterns (*CS*) to reducing the number of test patterns. An example to generate one compressed pattern is shown in Figure 4, where *P2* and *P3* can be generated by circularly shifting *P1* for one and seven cycles, respectively. Thus the three patterns can be merged into one.

In our procedure each pattern in *CS* is associated with a *weight* which indicates the similarity between the patterns. We say that a pattern is *compatible* to the FBT if the required logic values of the pattern can be

provided by the internal nets that are linked to the FBT. Among those patterns in *CS* that are compatible to FBT, we select the one that has the maximum number of rotation as the next feedback pattern. For the example in Fig 3, consider the pattern *TP1*=11000. This pattern is compatible to FBT because the values of *i1, i2* and *i3* of *TP1 (*Test pattern 1*)* can be provided by any net in {*n1, n2, n3*} and those of *i4* and *i5* can be provided by any net in {*n4,n5*}.

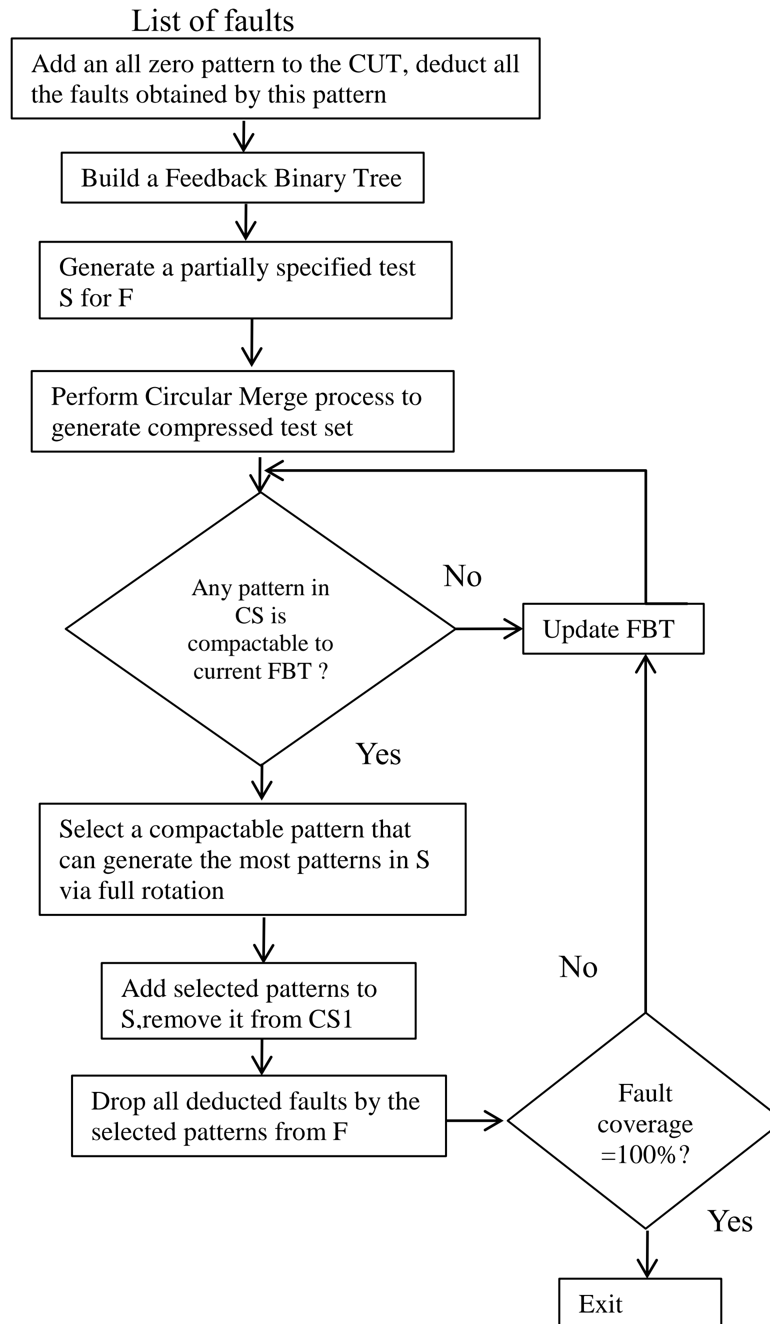
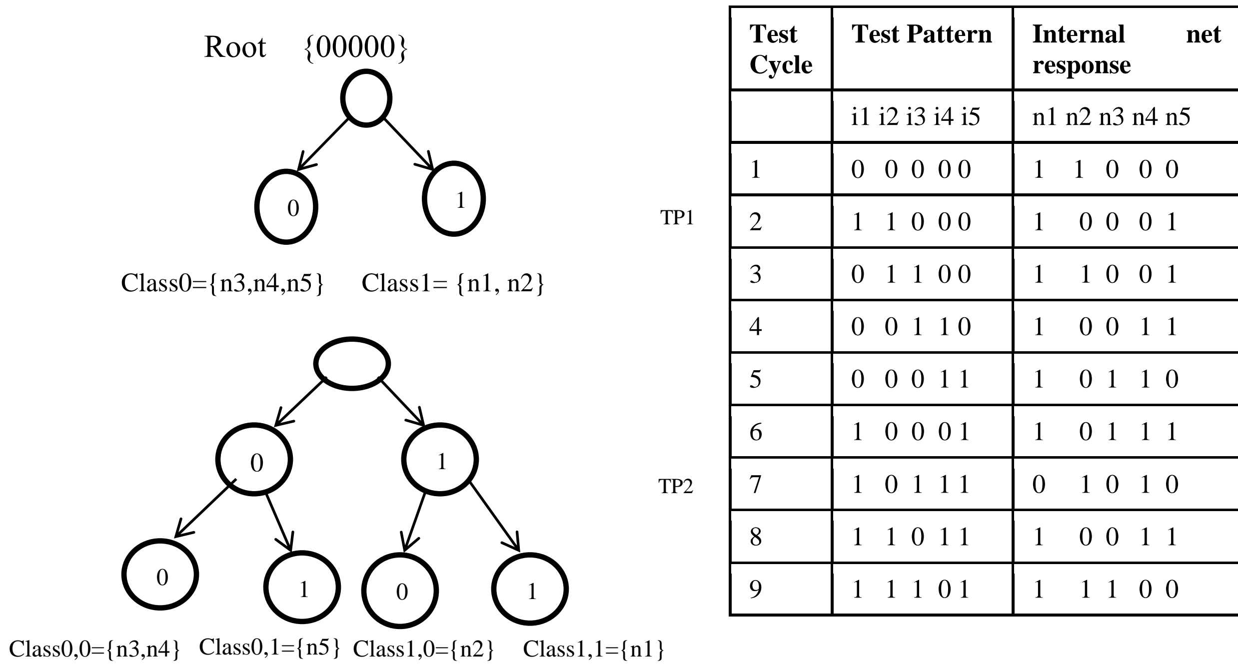


Fig 2. Test Pattern generation

This pattern is then used as the first feedback pattern and will be applied at second cycle.

Once a proper pattern in *CS* is selected, the pattern is added to *S* and removed it from *CS*. Next all the faults that are detected by the selected pattern and its associated rotation patterns are removed from the fault list. If now all testable faults are detected, then our procedure ends. Otherwise the FBT will be updated based on the current circuit responses. Refer Figure 3, after fully rotating *the first test pattern* we will enter Test Cycle 6 and the responses at this cycle will be used to update the current FBT. Here initially the logic value of *n1* is 1, *n1* is linked to a new leaf node Class1, 1, n2 is linked to Class1, 0, which provide a logic-0 value for the next feedback pattern.



Test Cycle	Test Pattern	Internal net response
	i1 i2 i3 i4 i5	n1 n2 n3 n4 n5
1	0 0 0 0 0	1 1 0 0 0
2	1 1 0 0 0	1 0 0 0 1
3	0 1 1 0 0	1 1 0 0 1
4	0 0 1 1 0	1 0 0 1 1
5	0 0 0 1 1	1 0 1 1 0
6	1 0 0 0 1	1 0 1 1 1
7	1 0 1 1 1	0 1 0 1 0
8	1 1 0 1 1	1 0 0 1 1
9	1 1 1 0 1	1 1 1 0 0

Fig 3. Example of feedback pattern generation and FBT

Similarly *n3, n4* are linked to new leaf nodes Class0, 0 and n5 is linked to Class0, 1. After the updating of FBT, the next test pattern is 10111 at the 7th cycle and if the current fault coverage is equal to the predefined value (PDFC) then we will stop the procedure otherwise again update the FBT until reaches the complete fault coverage.

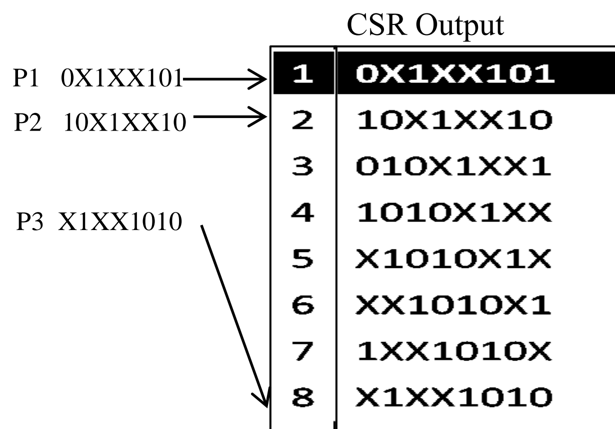


Fig 4. Circular Merge Process

IV. Experimental Results

1) Circular shift register

Fig. 5 shows the output response of a 5-bit CSR. By applying a single 5-bit input pattern to the primary inputs, we obtain 3 combinations. Here y0, y1, y2, y3, y4 are the outputs of CSR. Here the output is 1-bit circularly rotated in each clock cycle.

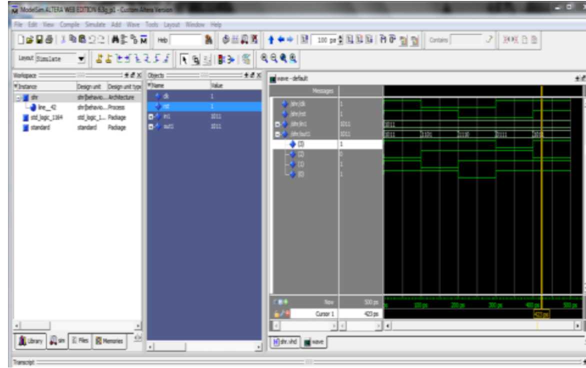


Fig 5: CSR Result analysis

2) *Circuit under test*

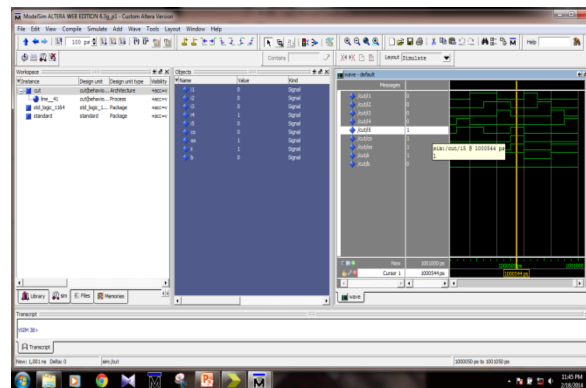


Fig. 6: CUT Result analysis

The fig.6 shows the response of a Circuit Under Test. Here the obtained response and pre-stored response are same that means no error occurred.

3) Internal net response of CUT

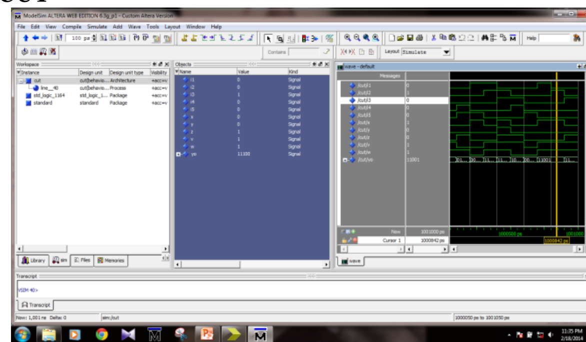


Fig. 7: Internal net response of CUT

Fig.7 shows the output waveform of the internal nets of CUT. In this a, b, c, d, e are the inputs and yo is the output.

V. Conclusion And Future work

In this paper we have developed an efficient deterministic BIST technique to achieve complete fault coverage. In this method there is no storage devices are required for storing the test patterns. We employ a circular shift register with some of the internal net response of the CUT has its input these provide all the required test patterns. By completely eliminating the memory storage device the area overhead and the power consumption is reduced. Comparison with other methods shows that 62% power reduction is occurred in this method. An efficient method to concurrently determine the test patterns to be generated from the feedback connections which results in much shorter test time compared to previous work. We can apply this method to industrial machines with reduced area overhead.

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