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Analysis of active resistors realized using CMOS technology

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Abstract: *The resistors implemented by IC technologies were found to be lacking in several areas of performance. The typical sheet resistance was sufficiently small that large values of resistors required large areas. The higher values of resistance attained with pinched resistors suffered nonlinearity. In addition, the tolerance of the resistors , their temperature coefficient, and their voltage coefficient were all poorer than those of capacitors. Modifications to the standard IC technology can result in better resistor implementation. However, the objective of this paper is to analyze and investigate ways of emulating a resistor without having the inherent disadvantages using standard IC technologies.*

Keywords: *Active resistors, Aspect ratio, Bulk effect, Saturation region, Voltage divider.*

I. INTRODUCTION

In many CMOS technologies, it is difficult to fabricate resistors with tightly-controlled values or a reasonable physical size. Consequently, it is desirable to replace such resistance with a MOS transistor. A MOSFET can operate as a small-signal resistor if its gate and drain are shorted. The active resistor can be used in place of polysilicon or diffused resistor to produce a DC voltage drop and /or provide small signal resistance that is linear over a small range. There are many cases where the area required to obtain a small signal resistance is more important than the linearity. A small MOS or BJT device can simulate a resistor in much less die-area than is required with an equivalent polysilicon or diffused resistor[1].

In this paper, section II provides a brief background about how active resistors are implemented. Section III discusses various resistor configurations including a simple voltage divider realization using active resistor combinations followed by active ac resistors in which how a large linearity range achieved is shown and bulk effect is reduced while a controllable high resistance is designed.

II. BACKGROUND

Active resistors can be implemented by simply connecting the gate of an n- or p- enhancement MOS device to the drain[1]. For the n-channel device, the source should be placed at the most negative power supply, V_{ss}, if possible, to eliminate the bulk effect. The source of the p-channel device should be taken to the most positive voltage for the same reason. Since V_{GS} is now equal to V_{DS}, the trans-conductance curve (I_d vs V_{gs}) of the MOS transistor shown in fig.1. This curve is valid for both n-channel and p-channel enhancement transistors for the polarities shown. The resistance is not linear as expected. In many circumstances, the signal swing is very small, and in these cases the active resistor works very well.

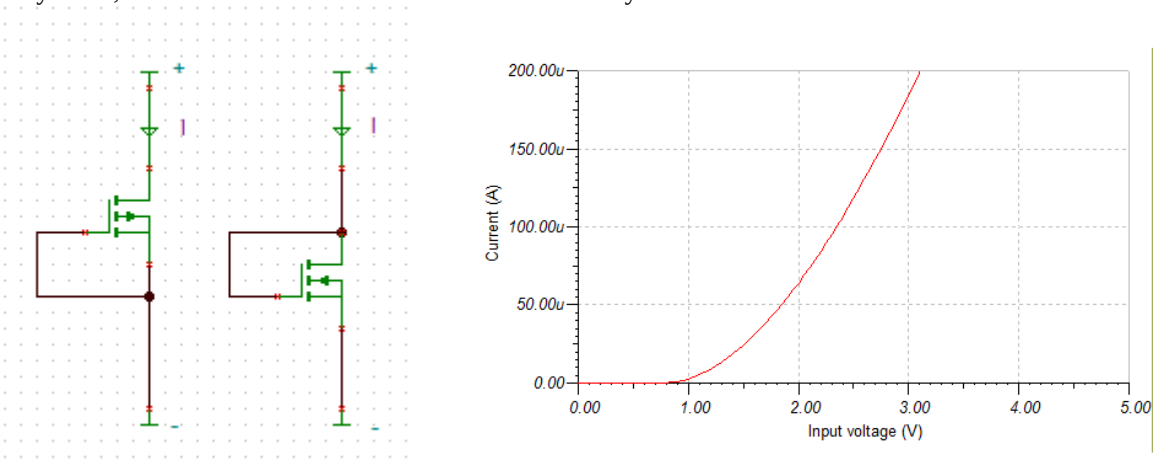

Figure 1 (a) n-channel enhancement active resistor (b) p-channel enhancement active resistor (c)Voltage-current characteristics of the MOS active resistor.

Since the connection of the gate to the drain guarantees operation in the saturation region for V > Vt, the I-V characteristics can be written as.

$I = I_D = \frac{K'W}{2L}[(V_{GS} - V_T)^2]$ (1)

$V = V_{GS} = V_{DS} = V_T + (\frac{2I_D L}{K'W})^{1/2}$ (2)

$K' = \mu_o C_{ox}$ (3)

Connecting the gate to the drain means that the V_{DS} controls I_D, and therefore the channel trans-conductance becomes a channel conductance. The small signal conductance can be found by differentiating equation (1) with respect to V, resulting in equation (4).

$g = \frac{\partial I}{\partial V} = (\frac{2IK'W}{L})^{1/2} = \frac{K'W}{L}(V\text{-}V_T)$ (4)

The bipolar junction transistor can be used to form an active resistor in the same manner as for the MOS transistor.

III. RESISTOR CONFIGURATIONS

3.1. Voltage Divider using active resistors

Active resistors can be used to produce a dc voltage or to provide a small signal resistance. The use of active resistors to develop large DC voltages requires large currents or W/L ratios that are much less than unity. This can be done by cascading devices shown in Fig.2(a).The voltages V_1, V_2 are given by equation(2), where I is from a known current source. If the voltages are specified, then the W/L ratio of each device can be determined from equation (2) if the bulk-source voltage is taken into consideration. If the W/L ratios are known, then the voltages can be calculated. Using more than one device to drop the voltage will result in W/L ratios closer to unity and smaller dc currents[2].

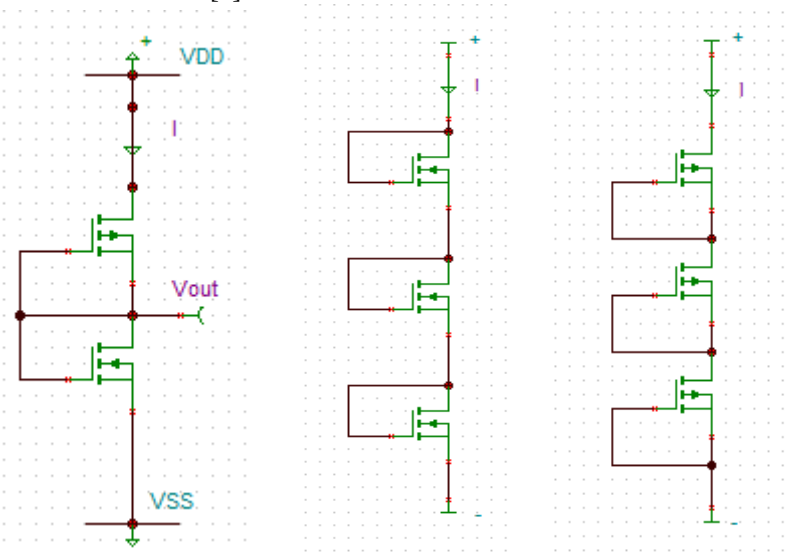

Figure 2. (a)Use of active resistors to achieve voltage division, (b) use of cascaded N-channel MOS devices for large voltage drops, (c) use of cascaded P-channel MOS devices for large voltage drops.

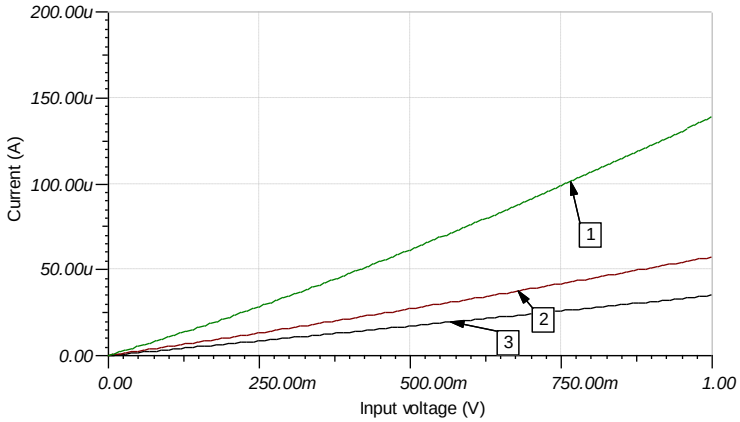

Figure 3. I-V characteristics for circuits in Fig 2 (b) by varying the number of MOSFETS.

In the above graph, the numbers pointing to each curve represent the number of MOSFETS used as active resistors. Here we observe that as the number of MOSFETS increase, it results in smaller dc currents hence resulting in large resistance.

By varying aspect ratio of MOSFETs (W/L) , the voltage divider configuration can be used in various applications such as in Schmitt trigger, feedback circuits, biasing circuits etc.

3.2. MOS ac resistor

An another application of a resistor is to provide an ac voltage (or current) for a given ac current (or voltage)[3]. For zero dc current, the active resistor of Fig. 1 is not satisfactory because the values of resistance approaches infinity. The circuit in Fig. 2 makes a much better alternative for an ac resistor with the MOS switch being nearly linear and having no dc offset. Linear ac resistances for small values of ΔV can be achieved by controlling the value of voltage difference between the gate and source. But the bulk influences the linearity by causing V_T to change. The drain-source voltage influences the linearity by leaving the ohmic region and entering the saturation region. Hence to eliminate these effects the following combination of MOSFETs can be used.
The effects of V_{DS} is eliminated upon the ac resistor realization in Fig.3. The principle used is to use 2 identical devices biased so that the effects of V_{DS} cancels.

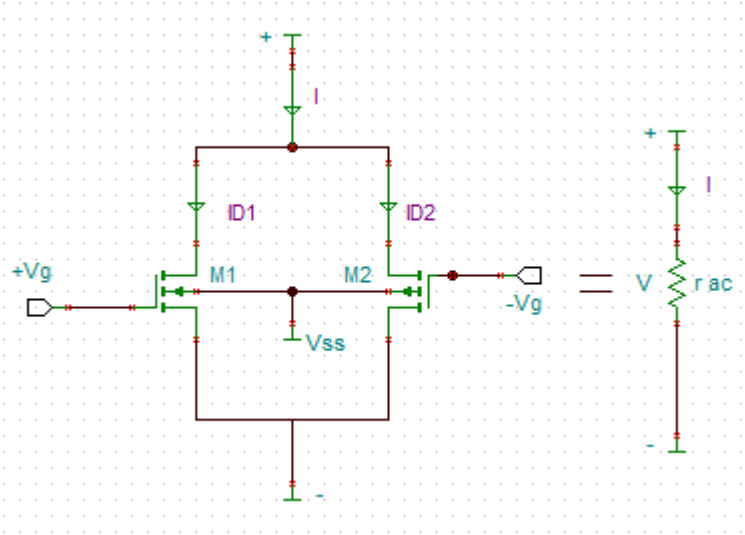

Figure 4. Configuration to eliminate the effects of V_{DS} in the ac resistor implementation of MOSFET

$$I_{D1} = K'_N\left(\frac{W_1}{L_1}\right)\left[(V_{GS1} - V_{T1})V_{DS1} - \frac{V_{DS1}^2}{2}\right]$$
$$= K'_N\left(\frac{W_1}{L_1}\right)\left[(V_{DS1} + V_C a - V_{T1})V_{DS1} - \frac{V_{DS1}^2}{2}\right]$$
$$= K'_N\left(\frac{W_1}{L_1}\right)\left[\frac{V_{DS1}^2}{2} + (V_C - V_{T1})V_{DS1}\right] \quad (5)$$
$$I_{D2} = K'_N\left(\frac{W_2}{L_2}\right)\left[(V_{GS2} - V_{T2})V_{DS2} - \frac{V_{DS2}^2}{2}\right]$$
$$= K'_N\left(\frac{W_2}{L_2}\right)\left[(V_C - V_{T2})V_{DS2} - \frac{V_{DS2}^2}{2}\right] \quad (6)$$

Assuming matched transistors the current I can be expressed as:

$$I = I_{D1} + I_{D2} = \frac{2K'_N W}{L}(V_C - V_T)V_{DS} \quad (7)$$

Thus the values of r_{ac} (ac resistance) can be found by differentiating equation (7) with respect to I:

$$r_{ac} = \frac{\partial V_{DS}}{\partial I} = \frac{1}{2K'_N(W/L)(V_C - V_T)} \quad (8)$$

In the above equations, the transistor is assumed to remain in ohmic region or $V_{DS} < (V_G - V_T)$. Thus a large value of V_G will lead to larger value of V. Although the linearity range has been increased , the dependence of V_{BS} through V_T is still present and must be eliminated to achieve a wide linearity range. In many applications,

resistors are used differentially in pairs. In such cases, an increase in linearity and to eventually even cancel bulk effects is possible. In such differential use , the ac resistance is represented by:

$$r_{ac} = \frac{\partial V_{DS}}{\partial I} = \frac{1}{K'_N(W/L)(V_C - V_T)}$$

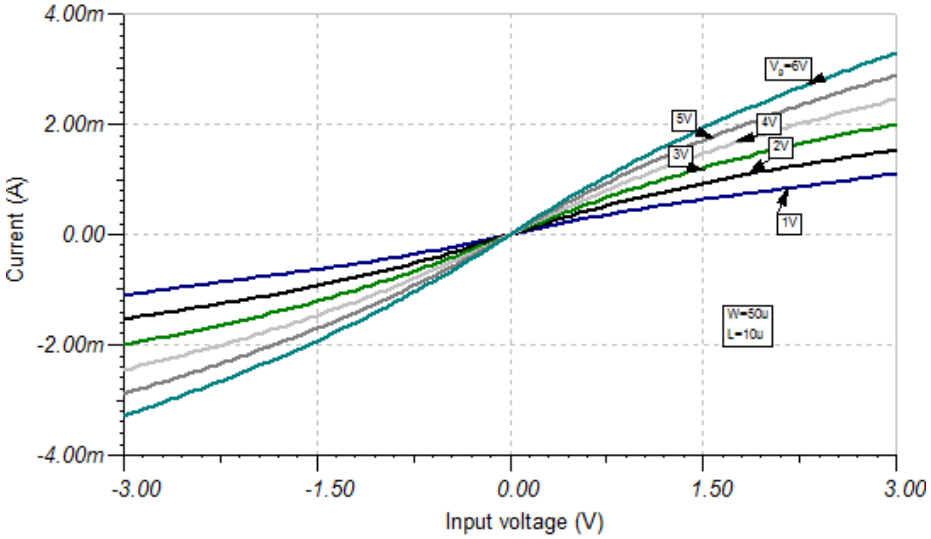

Figure 5. I-V characteristics parallel MOS resistor (ac resistor)

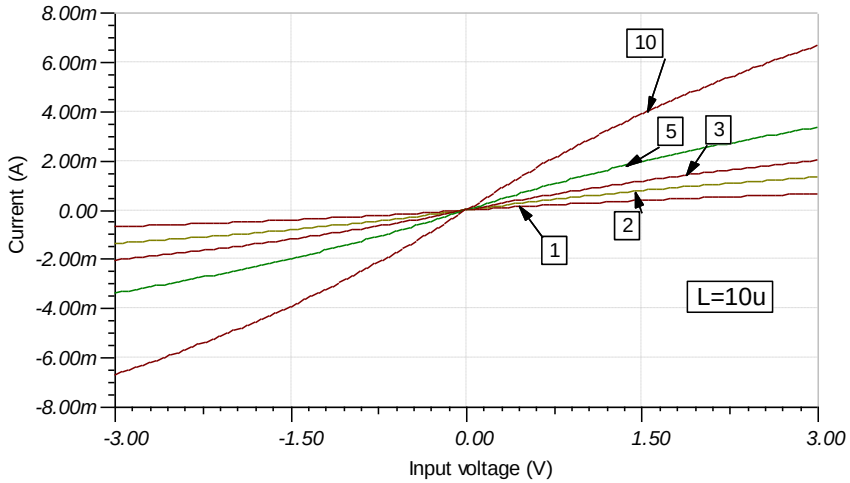

Figure 6. V-I Characteristics for different aspect ratios for circuit in Fig 4

The above graph is obtained by simulating the circuit in Fig 4 with constant channel length , varying width. The numbers pointing to each curve is aspect ratio of MOSFETs. Here, we observe for lower aspect ratios, slope of the curve is low and hence g_m is low, resulting in high resistance. Thus active resistance offered by the combination is inversely proportional to aspect ratio of the MOSFETs.

IV. CONCLUSION

The active resistors realized using enhancement type N-channel and P-channel MOSFETs are desirable over normally implemented external resistors and monolithic resistors[4] because a very high value of resistance can be achieved as observed in simulation results and with low die-area. Using more than one device results in lower dc currents. In terms of linearity , active resistors show a large range and are better.

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