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Analysis of CMOS Multiplexer Circuits of Different Area and Logic Style

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Abstract: *This paper is an approach to comprehend the VLSI design of multiplexers. A number of conventional designs of multiplexers along with several XOR based transmission gate and pass transistors based models are analyzed as a building block of diverse complex circuit system. Different sizes were approached starting from 4T to 22T. A comparative learning was made on total of eighteen (18) different 2:1 multiplexers to analyze the performance, area, power consumption and noise. PSPICE, DSCH, MICROWIND have been used for simulation. Finally different designs of multiplexers are specified for individual purpose to have better performance in diverse requirement.*

Keywords : *Digital Circuits, CMOS, Multiplexer, XOR, Output Voltage level.*

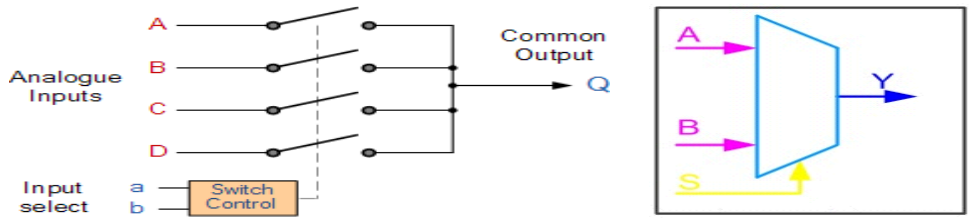
I. Introduction

Very-large-scale integration (VLSI) [1][2][3] is the design of extremely small, complex circuitry using modified semiconductor material. It may contain millions of transistors, each a few mm in size which is called Integrated circuit (IC).Multiplexers are unique VLSI device are so designed that have versatile use in different sectors of communication and digital system. By enhancing the performance of the different conditioning factors of the multiplexors we can change the system performance significantly. In our paper we have followed different techniques of VLSI [1][2][3] design to find various circuit designs of 2:1 multiplexer circuit and also observed the behaviour of those designs under various conditions to find the best models for different requirements. This approach was a way to introduce ourselves to the comparative study of VLSI design.

II. Multiplexer

In this paper analysis of various multiplexer designs is divided into four subsections. One is the voltage level comparison where output voltage for different combination of inputs is observed. This is done by using the Orcad Pspice 9.2 software.A multiplexer (MUX) is a digital switch which connects data from one of n sources to the output. A number of select inputs determine which data source is connected to the output. A multiplexer of 2n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. [9]

A 2 to 1 line multiplexer is shown in Fig 1(b) below, each 2 input lines A to B is applied to one input of an AND gate. Selection lines S are decoded to select a particular AND gate. The symbol for the 2:1 mux is given in the table below. Following is a simple example-source selection control on a home stereo unit. [4]



(a) (b)

Figure 1: (a) 4 to 1 channel multiplexer (b) Symbol for the 2:1 multiplexer

The Boolean expression for a 2:1 multiplexer is as: Y=AS+BS'
Here A and B are Inputs and S is the selector parameter and Y is the output.
For XOR Based 2 input multiplexer the Boolean expression is given by: Y= AB'+BA'
Here A and B are inputs and Y is the output.

III. Design Issue

In this paper all the circuits are simulated by PSPICE & DSCH2 software. Here we use two special types of MOS,N-Mos(mbreakN4D) & P-Mos (mbreakP4D) whose ratio is 2:1. The physical W/L size of P-Mos & N-Mos is 4.8µ/0.8µ respectively. The input signals are depicted in Fig 2. XOR or Transmission gate input signals for A & B covers four types of combinations i.e. 00, 01, 10& 11. In case of selection pin S, then three input combinations are 000,001,010,011,100,101,110,111.

1.1. VPULSE input signals for two input design & their wave-shapes

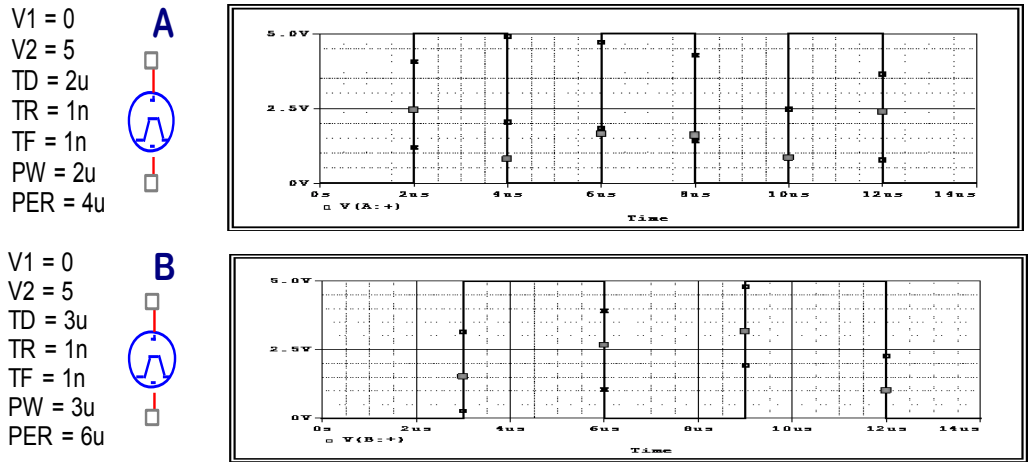


Figure 2: XOR and Transmission gate input signal A & B respectively

1.2. VPULSE input signals for three input design& their wave-shapes

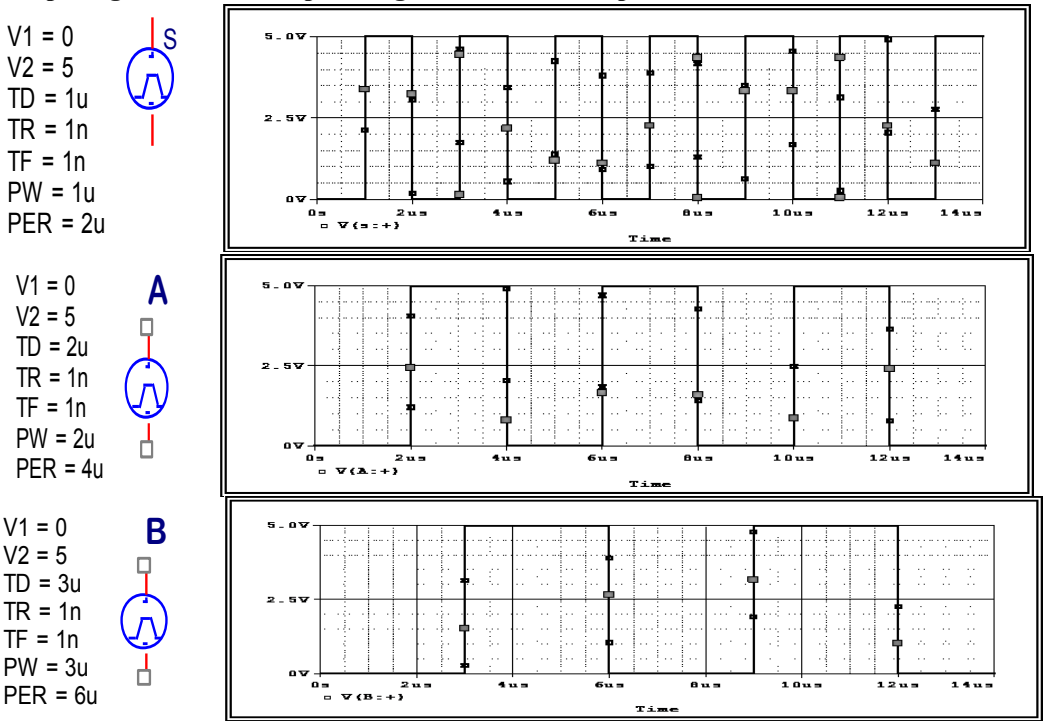


Figure 3: Multiplexer input signals S, A & B respectively.

For simulation, in simulation setting we used time domain (Transient) as analysis type, run to time 20µs, start saving data after zero second, maximum step size 0.1µs. normally N-MOS (mbreakN4D) & P-MOS (mbreakP4D) have threshold value |VT| of -4.0. But to achieve better result we use threshold value of -0.9 instead of -4.0, it means we decrease the value .The lower the |VT|, the smaller the gap between the defect case and the normal case. LEVEL 1 MOSFET has been used for simulation. Model parameters of all simulations are same and they are given below. [13]

Table 1: The Parameter of Transistor Use in Simulation.

Model MbreaknD NMOS LEVEL=1			
+VTO=-0.9 +WD=25E-09 +LAMDA=0 +PBSW=0.8 +CGDO=0 +UCRIT=10E+03+WETA=0 +XPART=0	L=100E-06 KP=20E-06 IS=10E-15 CJ=0 CGBO=0 DIOMOD=1 U0=0	W=100E-06 GAMMA=0 JS=0 CJSW=0 TOX=0 VFB=0 TEMP=0	LD=60E-09 PHI=0.6 PB=0.8 CGSO=0 XJ=0 LETA=0 VDD=0

Model MbreakpDPMOS LEVEL=1			
+VTO=-0.9 +WD=25E-09 +LAMDA=0 +PBSW=0.8 +CGDO=0 +UCRIT=10E+03 +WETA=0 +XPART=0	L=100E-06 KP=20E-06 IS=10E-15 CJ=0 CGBO=0 DIOMOD=1 U0=0	W=100E-06 GAMMA=0 JS=0 CJSW=0 TOX=0 VFB=0 TEMP=0	LD=60E-09 PHI=0.6 PB=0.8 CGSO=0 XJ=0 LETA=0 VDD=0

II. Logic style

1.3. Conventional CMOS Style Multiplexer

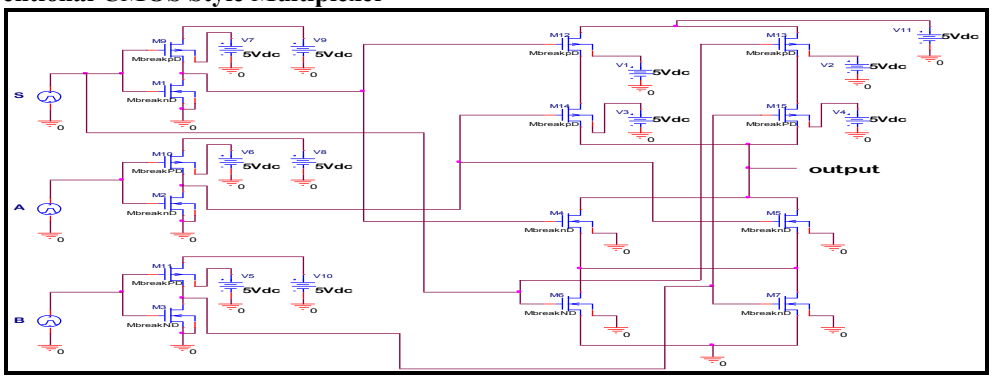


Figure 4: Conventional CMOS Style Multiplexer Circuit.

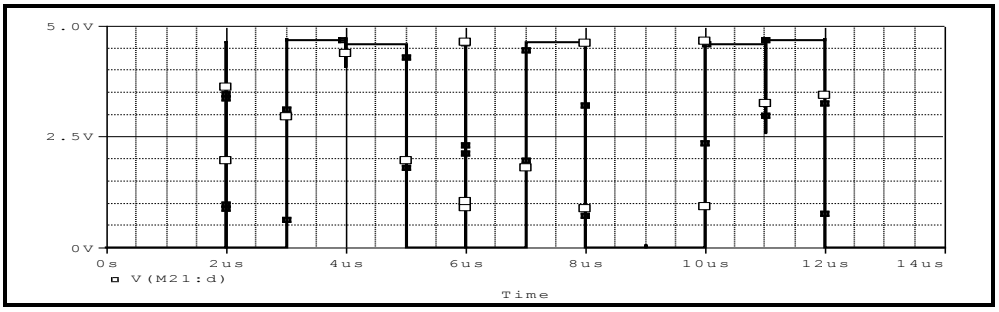


Figure 5: Simulation Result of Conventional CMOS Style Multiplexer

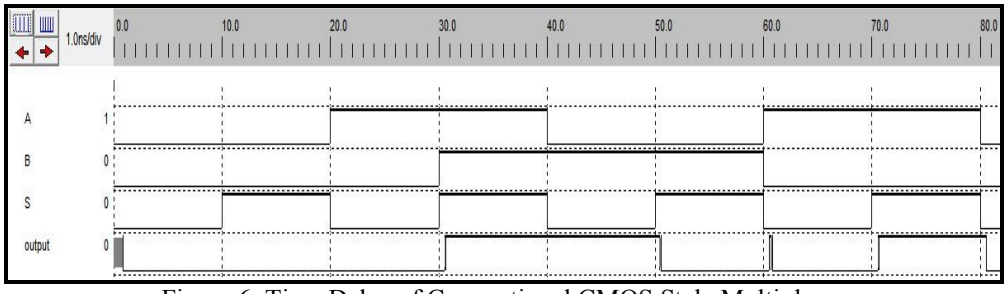


Figure 6: Time Delay of Conventional CMOS Style Multiplexer

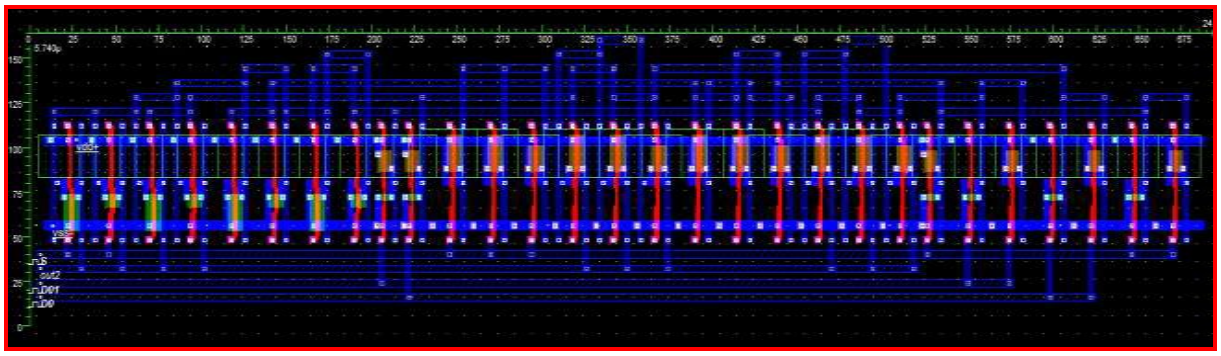


Figure 7: Layout Diagram Conventional CMOS Style Multiplexer

Table 2: Output Voltage Level of Conventional CMOS Style Multiplexer.

S	A	B	Logic Output	Simulated Output (Volt)
0	0	0	0	0.0
0	0	1	1	4.6
0	1	0	0	0.0
0	1	1	1	4.6
1	0	0	0	0.0
1	0	1	0	0.0
1	1	0	1	4.7
1	1	1	1	4.7

Table 3: Total Power Dissipation of Conventional CMOS Style Multiplexer for Different Supply.

Supply Voltage (Volt)	Power Dissipation (Watt)
0.8	1.52 E-5
1.0	2.95E-5
2.0	0.25E-4
3.0	2.96E-4
4.0	3.44E-4
5.0	8.29E-4

The time delay of the conventional CMOS style multiplexer is 0.85ns. [6] The area of the multiplexer depends on the number of transistor in the integrated circuit. Here the total number of transistor of conventional CMOS style multiplexer is 14T. The output voltage level of this model is varying from 4.6 to 4.7, where it should be 'LH' and 0.0 for 'LL' output. From the above data, we can say that, the overall performance of conventional CMOS style multiplexer is moderately good in terms of its output voltage level deviation and also the speed, power dissipation fluctuation remains within the considerable range [5].

In this way we also design and simulate the Pass Transistor type Multiplexer (Module 1)[11][12], Multiplexer using NAND gate, Multiplexer using NOT, AND and NOR gates and find out their simulation result [8], time delay, layout diagram[7].

1.4. Pass Transistor Type Multiplexer(Module-1)

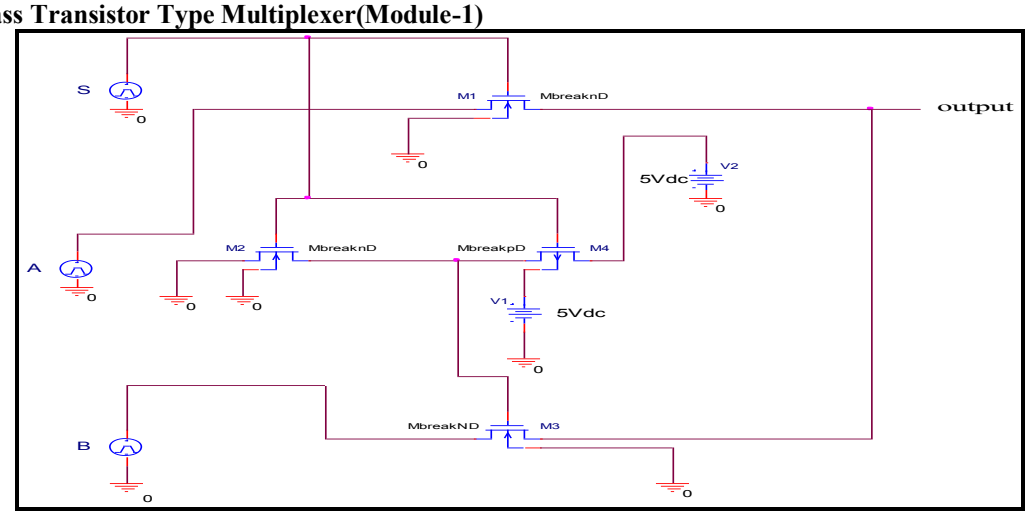


Figure 8: Pass Transistor Type Multiplexer (Module-1)

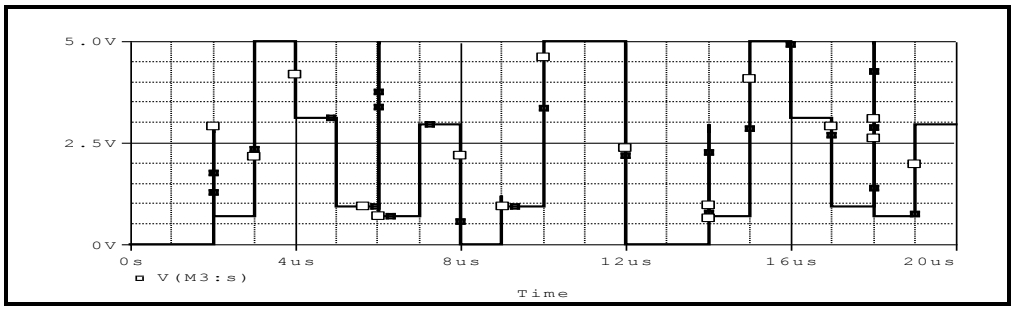


Figure 9: Simulation Result of Pass Transistor Type Multiplexer (Module-1)

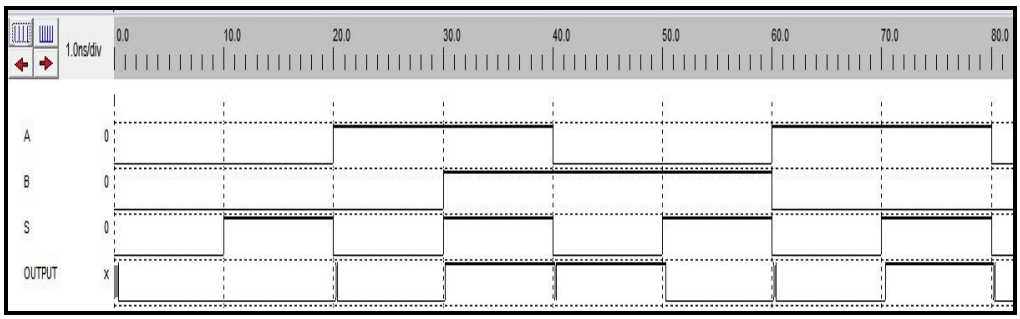


Figure 10: Time Delay of Pass Transistor Type Multiplexer (Module-1)

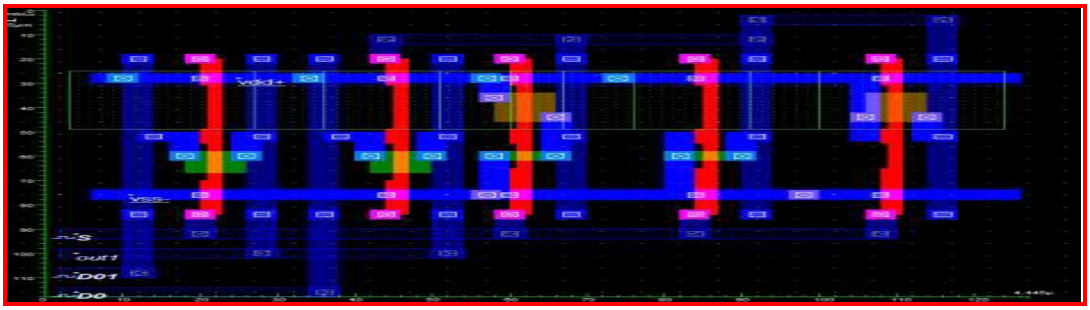


Figure 11: Layout Diagram of Pass Transistor Type Multiplexer (Module-1)

1.5. Multiplexer using Universal NAND Gate

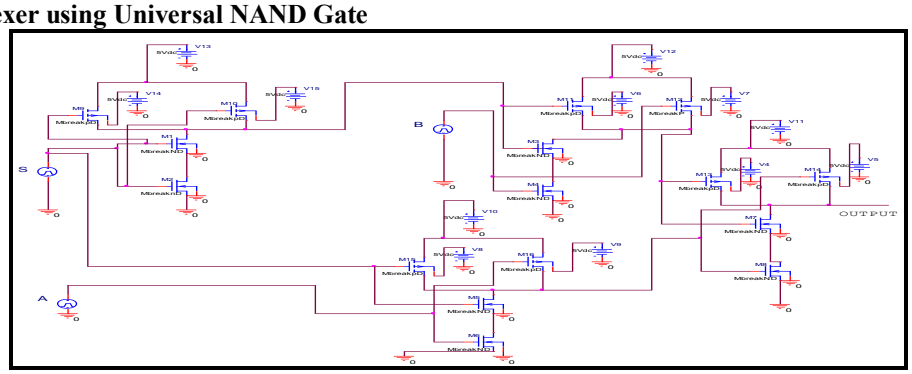


Figure 12: Multiplexer using Universal NAND Gate.

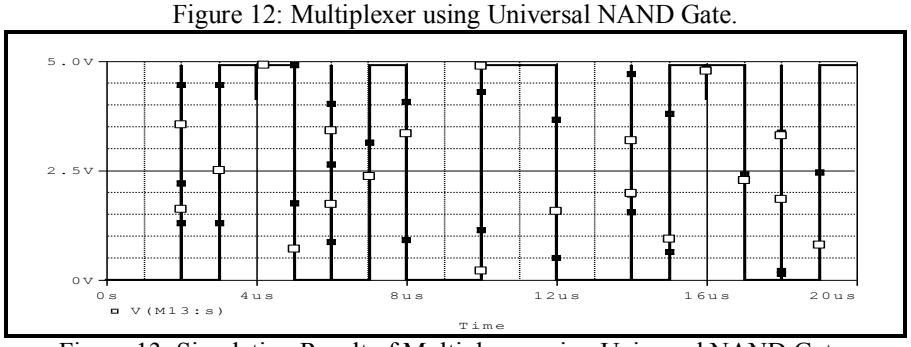


Figure 13: Simulation Result of Multiplexer using Universal NAND Gate.

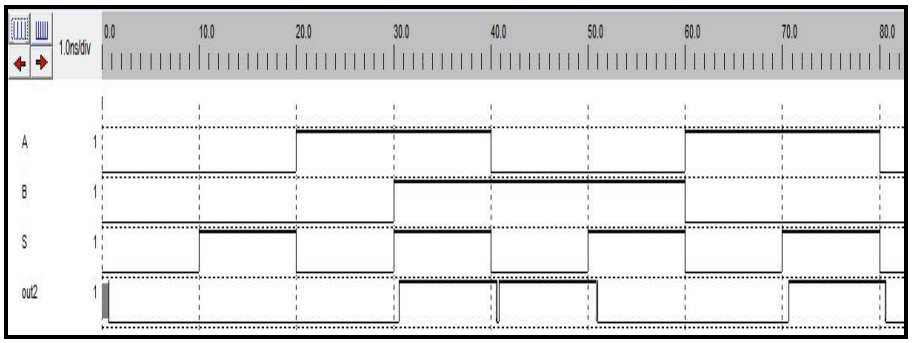


Figure 14: Time Delay of Conventional Multiplexer using Universal NAND Gate.

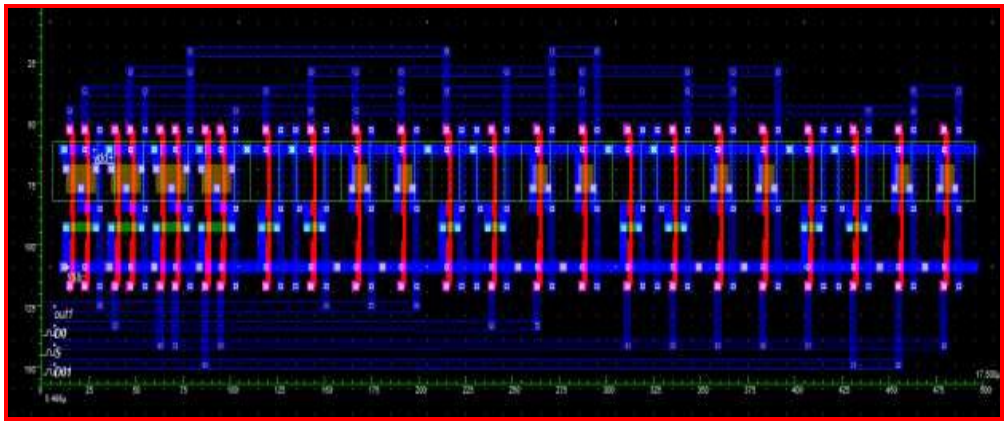


Figure 15: Layout Diagram of Conventional Multiplexer using Universal NAND Gate.

1.6. Multiplexer Using NOT,AND & NOR Gates

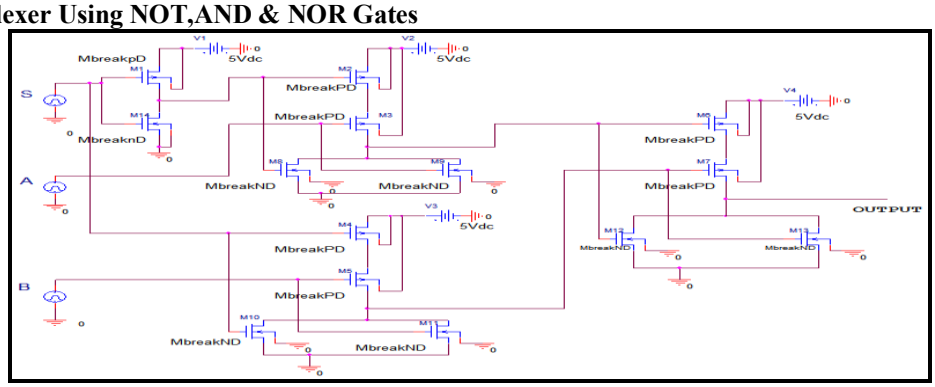


Figure 16: Multiplexer Using NOT,AND & NOR Gates

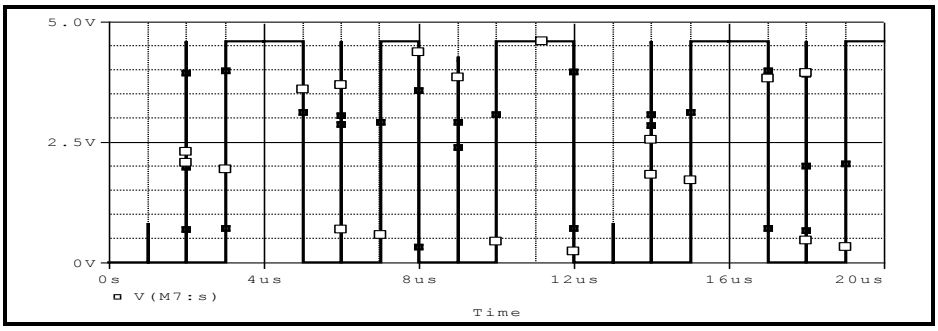


Figure 17: Simulation Result of Multiplexer Using NOT,AND & NOR Gates

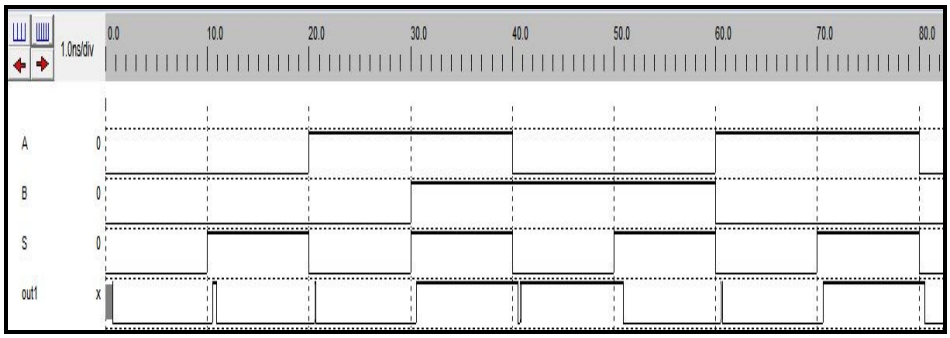


Figure 18: Time Delay of Conventional Multiplexer Using NOT, AND & NOR Gates

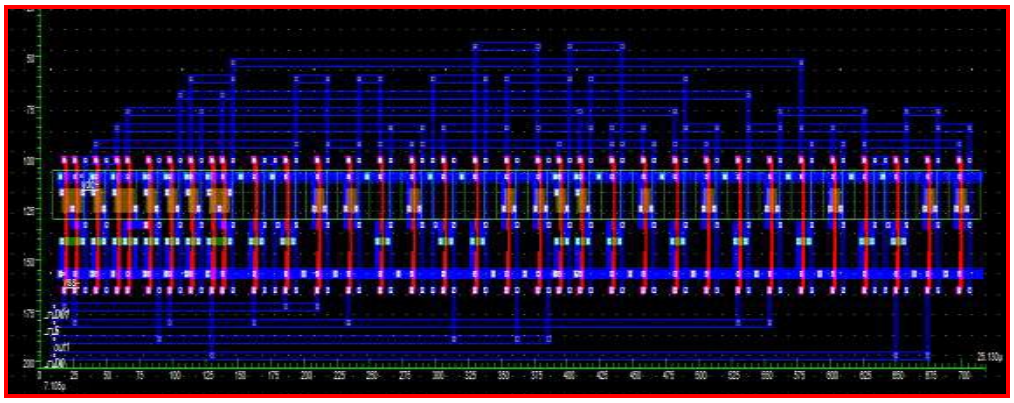


Figure 19: Layout Diagram of Conventional Multiplexer Using NOT, AND & NOR Gates

1.7. XOR implementation with Transmission Gate

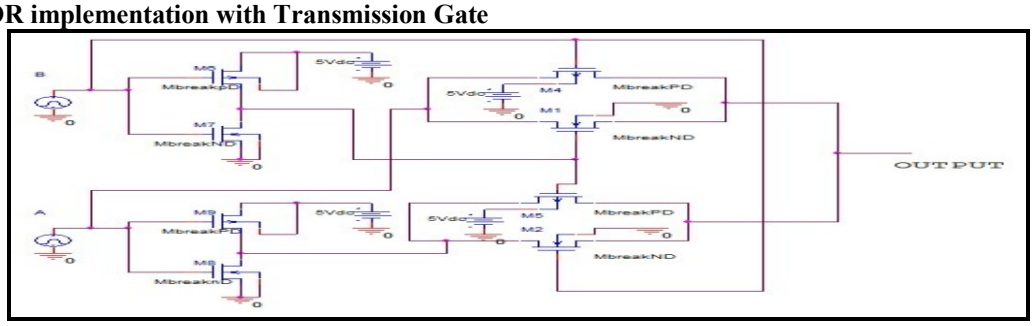


Figure 20: XOR implementation with Transmission Gate.

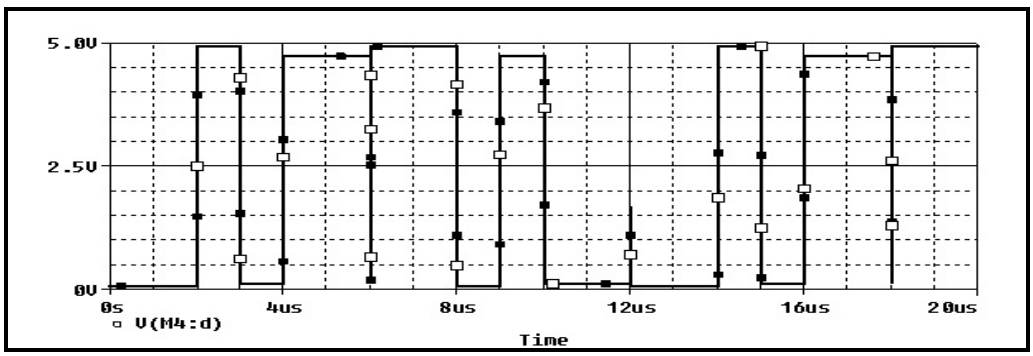


Figure 21: Simulation Result of XOR implementation with Transmission Gate.

1.8. Improved XOR Structure

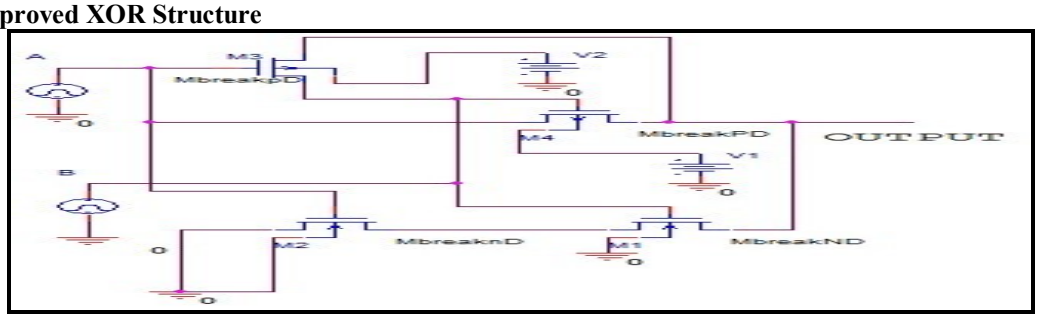


Figure 22: Improved XOR Structure.

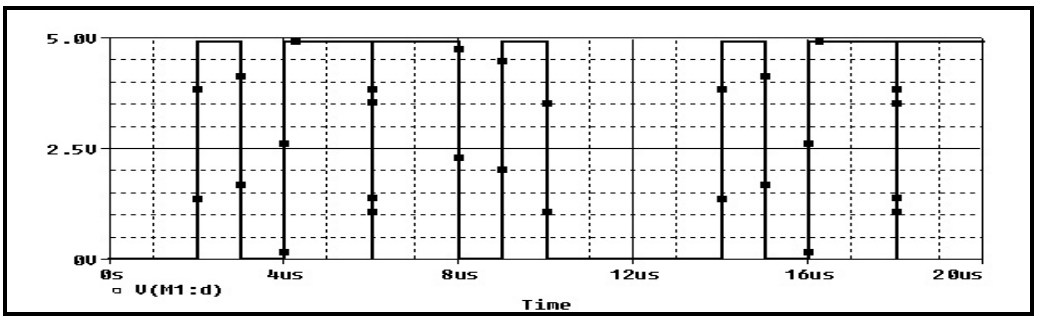


Figure 23: Simulation Result of Improved XOR Structure.

In this way we accomplished XOR implementation with Transmission Gate, XOR implementation by Transmission Gate with Driving Output, Inverter Based XOR Structure, Modified XOR Structure with Driving Output, High Performance XOR Implementation and find out their simulation output. [14]

III. Analysis On Simulation Result

It is possible to reduce the delay of all designs without significantly increasing the power consumption by calibrating the transistor sizes of the multiplexers considered. At the initial stage of simulation all multiplexer were designed with minimum transistor sizes. In this stage comparison of various multiplexers is discussed. The discussion is divided into four subsections refer to the output voltage level, delay or speed, power and area respectively.

1.9. Comparison of output voltage level for three input design

In this section we discussed output for different values of input from the figure we can find the best multiplexer designed with respect to the output voltage. The comparison is based on VDD 5V.

For input combination 000 there should be output 0 theoretically, From Fig 24 (a) we can declared that CMOS/ AND,NOT/ NAND,NOT,NOR/ NAND/ NOT,AND,NOR have good outputs and PT-1/TG-1/NOR have comparatively deprived output.

For input combination 001 there should be output 1 theoretically, From Fig 24 (b) we can declared that NAND,NOT,NOR/ NAND have good outputs and PT-1/TG-1 have comparatively deprived output and others are not bad.

For input combination 010 there should be output 0 theoretically, From Fig 24 (c) we can declared that Pt-1 gives the worst output,TG-1 and NOR shows negligible deviation and rest of the outputs are excellent.

For input combination 011 there should be output 1 theoretically, From Fig 24 (d) we can declared that TG-1 and PT-1 have good outputs and NAND,NOT,NOR and NAND also have good outputs and rest of the designs are not bad.

For input combination 100 there should be output 0 theoretically, from Fig 25 (a) we can observe that and PT-1, TG-1 and NOR have some deviation with good outputs and rest of the designs are very good.

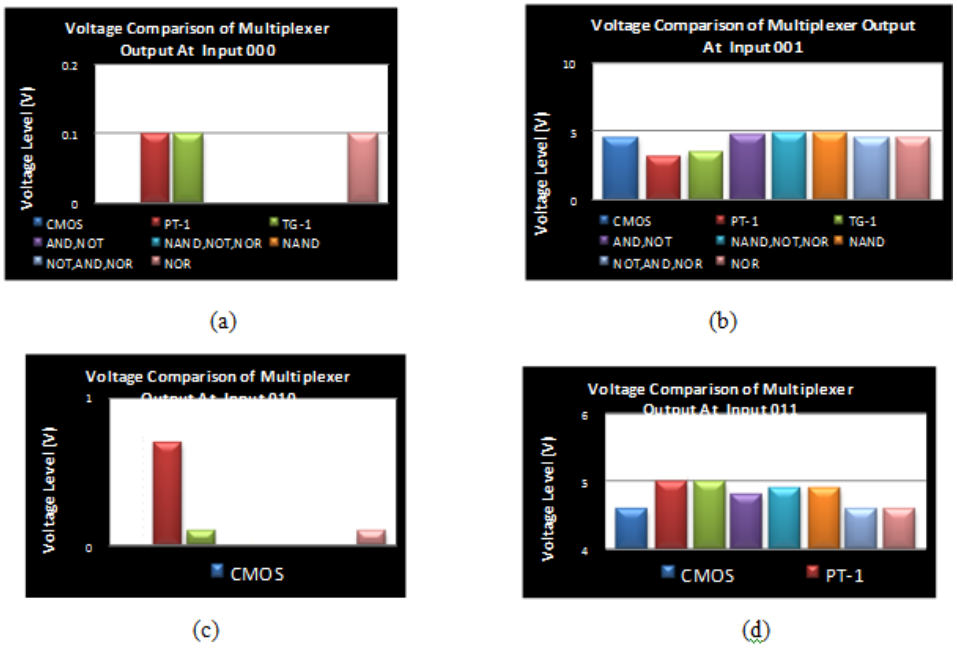


Figure 24: Voltage Comparison of Three Inputs Multiplexer Output At Input (a) 000 (b) 001 (c) 010 (d) 011

For input combination 101 there should be output 0 theoretically, from Fig 25 (b), we can state that Pt-1 gives the worst output, TG-1 and NOR shows negligible deviation and rest of the outputs are excellent.

For input combination 110 there should be output 1 theoretically, From Fig 25 (c) we can observe that TG-1/AND,NOT/NAND,NOT,NOR/NAND have the best outputs and CMOS/NOT,AND,NOR/NOR have comparatively good outputs and PT-1 has the worst output comparing to the others.

For input combination 111 there should be output 1 theoretically, From Fig 25 (d) we can observe that PT-1/ TG-1 have the perfect output while NAND,NOT,NOR/ NAND are the penultimate and AND,NOT have slightly less output result compared to NAND,NOT,NOR/ NAND. While CMOS shows the output with little bit deviation compared to AND, NOT. At last the output of the NOT, AND, NOR/NOR are the worst compared to the other parameters of this design.

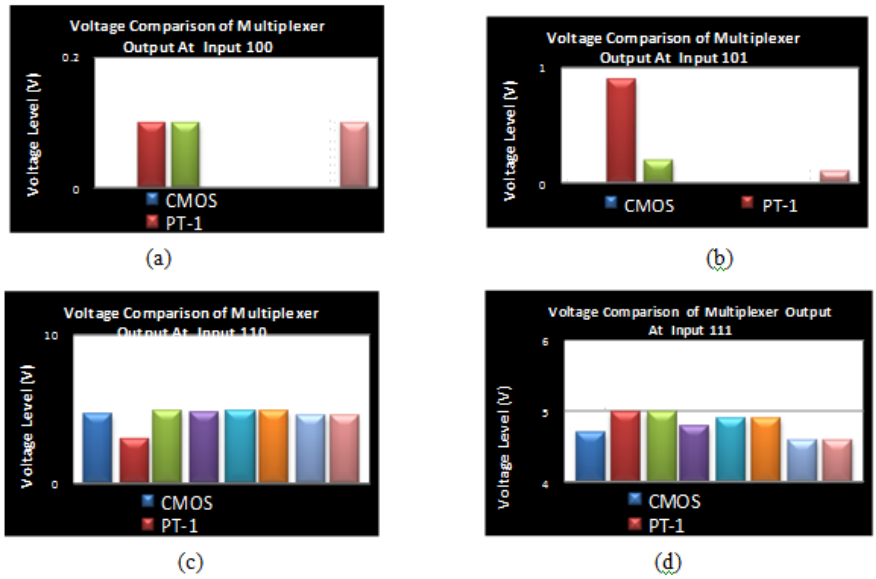


Figure 25: Voltage Comparison of Three Inputs Multiplexer Output At Input (a) 100 (b) 101 (c) 110 (d) 111

1.10. Power Dissipation Comparison

The average power dissipation is evaluated under different supply voltages and summaries in Fig 26. Among the conventional three input multiplexers CMOS logic style designs have the highest power dissipation. Because of the dual rail structure and high number of internal nodes this design style consumes high power. Therefore these multiplexers should not be used if primary target is low power dissipation[10]. Some designs

consists of logic gates such as NOR, AND, NOT, NAND. These gates are also designed in CMOS logic style which dissipates higher power. The designs with two transmission gates consumed higher power in spite of having less number of transistor and nodes. XOR based two input designs IMPV-1 have the lowest power consumption due to less number of transistors (only 4), less nodes and no transmission gates.

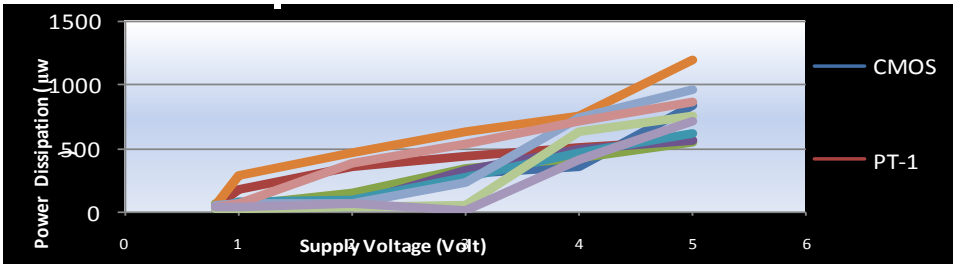


Figure 26: Power Variation Graph of all Multiplexers for Different Supply Voltage

1.11. Delay Comparison

The value of delay obtained for considered values of VDD 5V for all the multiplexers are calculated and compared. It is apparent that among the existing conventional three input multiplexers the transmission gate based designs have the lowest time delay. Pass transistor based designs also suffered less time delay compared to others. This is due to less number of inversion levels and compact design. The AND/NOT gate based design showed the highest delay. So this is not a good design if speed is the primary concern. In the two inputs XOR based designs the designs without driving capability have the smallest delay. For example XOR-TG-1 and XOR-TG-2 are almost same design but XOR-TG-2 has driving capability. Due to this difference XOR-TG-2 shows almost double the time delay of XOR-TG1.

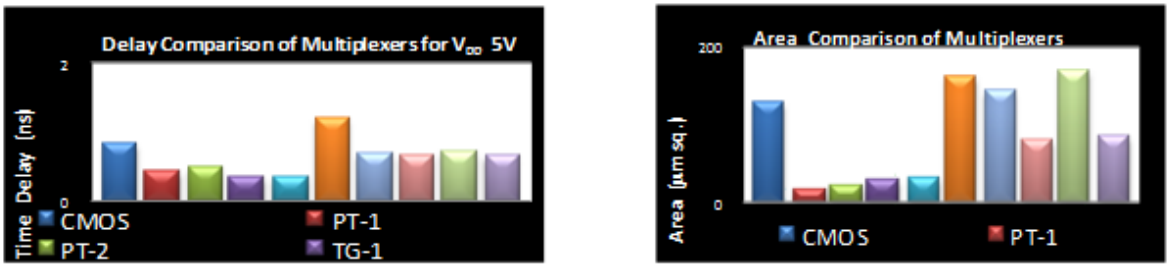


Figure 27: (a) Delay Comparison of Multiplexers for V_{DD} 5V (b) Area Comparison of Multiplexers

IV. Conclusions

In this paper, different multiplexers have been implemented, simulated, analyzed and compared. We observed that among the three input designs transmission gate and pass transistor based deigns are faster and smaller compared to conventional CMOS style designs. In spite of having this advantage mentioned designs are not the best if we consider output voltage levels. Using driving capability technique this problem can be minimized. The conventional CMOS style based designs have great output voltage level and less noise margin. Some deigns like universal NAND, AND/NOT, NAND/NOR/NOT give precise output voltage. Though they suffer higher delay and consume large area these designs can be considered for accurate and reliable output.

The two input XOR based designs are very compact and fast. [15] Transmission gate based designs consumes high power. But the main drawback is that there is no selection pin, so these designs are not appropriate for multiplexing where both the inputs may have identical value at any instant. In the end we may conclude that no single design is found to be the best in every criterion. Different multiplexers were found to render the best performance for diverse requirements. So we should choose the most suitable model considering the best performance in their required condition for a certain level.

Acknowledgements

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