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Reduction of unwanted switching through skewing the circuit

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Abstract: *This Paper proposed a method of Skewed circuit to avoid the unwanted switching of the controlling operation during the continuation of same level of the signal. In Application where the control model has to check the command signals at beginning of each clock cycle to control the further operation , this types of switching can provide the better potency. In this paper we apply this method on the widely used CMOS technology .All the proposed work is designed & analysed over the DSCH2.7f & Microwind 2.6k.In this paper we compare a full adder using the conventional CMOS and proposed Skewed CMOS on 0.12µm.*
Keywords: *CMOS, Skew, Microwind, DSCH*

I. Introduction

In today's era most of the Integrated circuit is based on CMOS technology due to the area, speed and power constraints and performance. This performance may be improved to better potency and control by skewing the integrated circuit [1]. In skewing process, we changes the sizes of different MOS of different types [2].The circuit topology of the skewed logic is same as the unskewed logic [3].When we keep parameter ($\beta = \mu$CoxW/L) equal for both PMOS and NMOS i.e. $\beta p = \beta n$ in an inverter, the inverter threshold voltage V_{inv} is $V_{dd}/2$, where μ, Cox, W, L are mobility, oxide capacitance per unit area, width and length of channel respectively. Which provide the better noise margins and allows a capacitive load to charge and discharge in equal time? This provides the beta ratio $\beta p / \beta n = 1$ which has normal skew or say unskewed. But we know that the mobility of NMOS is approx. double of PMOS. Hence to keep beta ratio equal to one we have to keep the width of PMOS double to the NMOS for the unskewed. We adjust the width of MOS the beta ratio affected and known as skewed inverter. If $\beta p / \beta n \rangle 1$ then this account as high skewed or HI-skew and if $\beta p / \beta n \langle 1$ then it is known as low skewed or LO-skew. An HI-skew has stronger PMOS while LO-skew has weaker PMOS. This beta ratio simply affects the switching voltage as shown in transfer characteristic in fig (1).As we move right the beta ratio increase and the switching voltage also increases. Particularly when one input transition is more important than other, we can use HI-skew gate to favour the rising output transition or LO-skew gates to favour the falling output transition. This favouring can be done by changing the size of non-critical MOS. Skewed logic is comparable in performance to the dynamic circuit but have better noise margin. Basically skewed circuit have a trade-off between gate delay and noise margin[3].Section II will describe the skewed & unskewed logic practical description by taking an example of NAND-NOR logic circuit. Section III & IV will discuss an avoidance of switching by the use of skewed CMOS applied on adder.

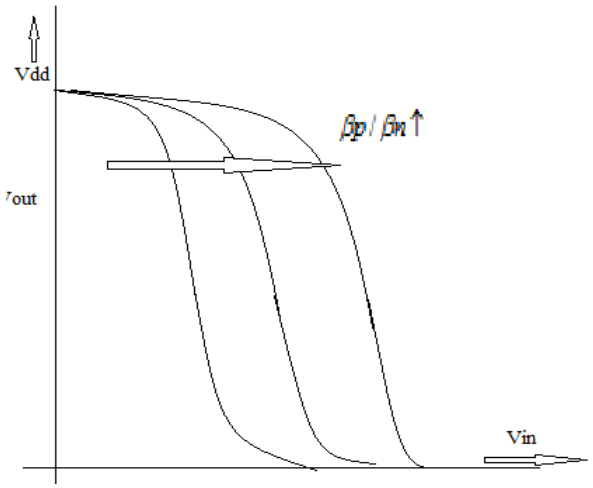

Fig.1Transfer Characteristic for different beta ratio

II. Unskewed & Skewed Circuit

An NAND-NOR logic is designed over DSCH tool and analysed over the Microwind, The PMOS transistor in the unskewed gate are enormous in order to provide equal rise delay. They contribute input capacitance for both transitions, while only helping the rising delay. Fig (2) shows the schematic of the logic in unskewed condition and fig (3) shows the output waveforms for different input combination for that. The Boolean expression of the output is given by

$$Out1 = \overline{\overline{IN1*IN2}+IN3} \quad = IN1*IN2*\overline{IN3}$$

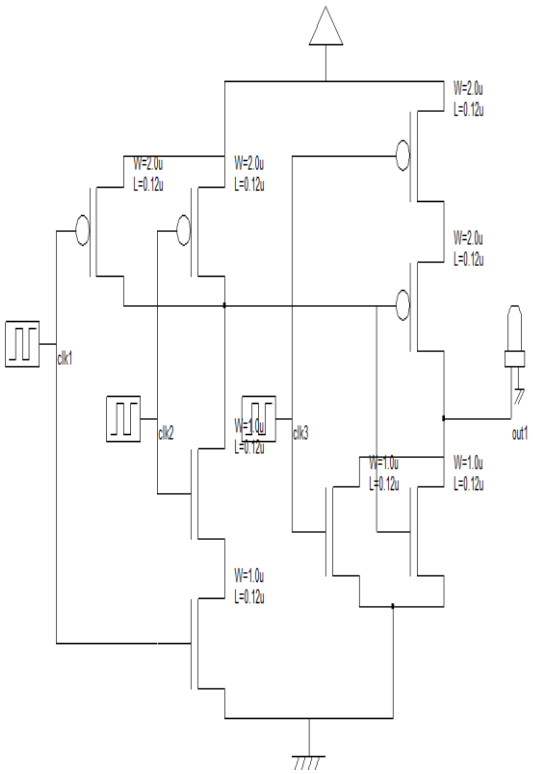

Fig.2 Schematic of unskewed NAND-NOR

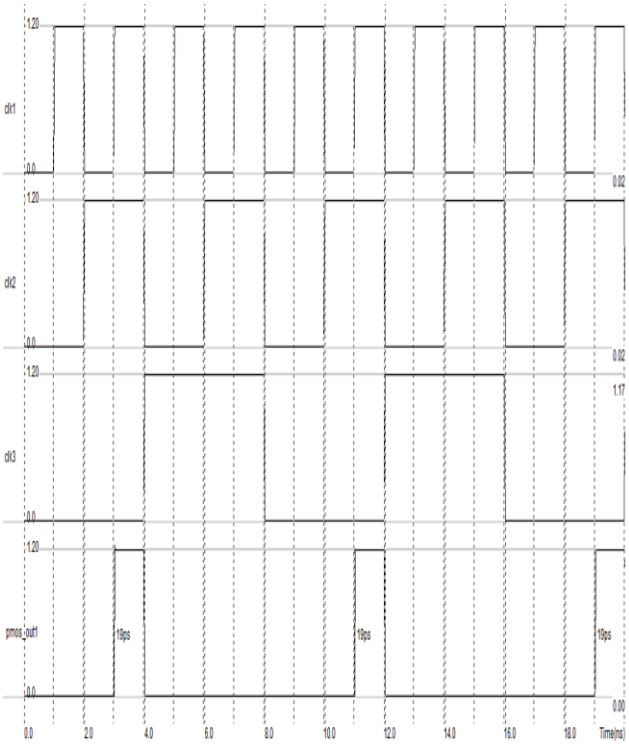

Fig.3 Waveform of unskewed NAND-NOR

This circuit contains an NAND with input IN1 and IN2 and followed by a NOR having input IN3 and output of NAND.The width and length of PMOS in pull-up circuit of unskewed logic are 2µm and 0.12µm and for NMOS in pull-down are 1µm & 0.12µm.This NAND-NOR have the capacitance & resistance at output terminal 2.93fF,796ohm This provide the rise & fall delay of 0.004ns & 0.001ns respectively. Waveforms are shown in fig(3) for the different input apllied. First three waveform shown in fig(3) are three inputs and last one is the final output.Figure(3) shows a riseing delay of 19ns at every low to high transition in output waveform.

Now this logic is skewed. By accepting a slower rise delay, the PMOS transistor can be downsized to reduce input capacitance and average delay and also it reduces the power consumption [4].A high speed at high to low transition can be achieved by increasing the width of NMOS & decreasing the width of PMOS in NAND, while for low to high transition we just reverse this change in NOR logic i.e. Width of PMOS is increased & NMOS is decreased. A schematic of skewed NAND-NOR logic is shown in fig (4).The widths of PMOS & NMOS in NAND logic are 0.4µm, 1.2µm respectively, which provide considerably high width in NMOS for discharge. But in NOR logic, width ratio is kept reverse and these are 3µm & 0.4µm for PMOS & NMOS. This measurement provides a capacitance and resistance of magnitude 3.04fF & 837ohm at output terminal [5]. This skewing shifts the delay of 0.001ns from rising end to falling end. Now the new rise delay and fall delay are 0.003ns, 0.002ns. Waveforms for different input is shown in fig (5)

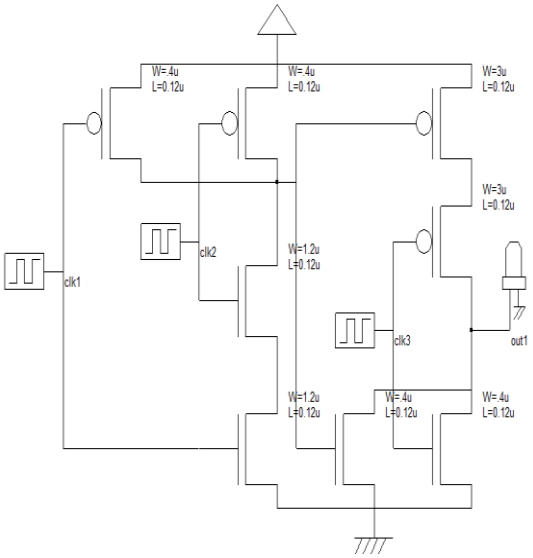

Fig.4 Schematic of skewed NAND-NOR

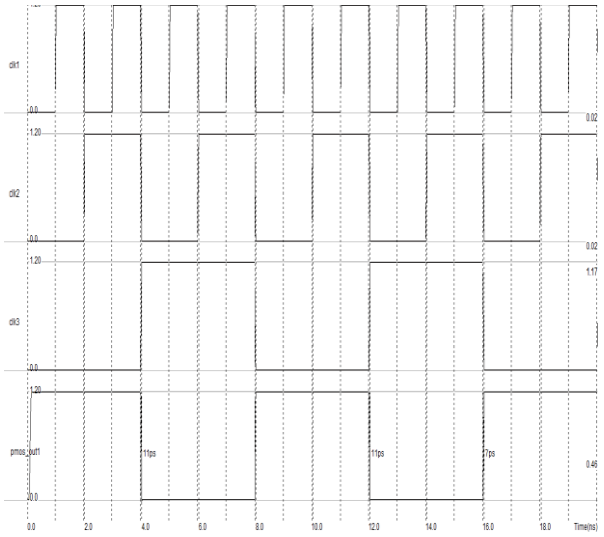

Fig.5 Waveform for skewed NAND-NOR

We can see in fig (5), the rise transition is now delayed by 7ns instead of 19ns as in previous case. This simply shows that the skewing can be used for faster transition of particular level change, can avoid unwanted switching.

III. Unskewed Adder Realisation

A full adder provide the sum of three input and carry, sum logic function is defined by equation (1), (2)

$$S = A \oplus B \oplus C \quad \text{-- (1)}$$

$$S = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC \quad \text{-- (2)}$$

The schematic of unskewed full adder on DSCH is shown in fig (6)

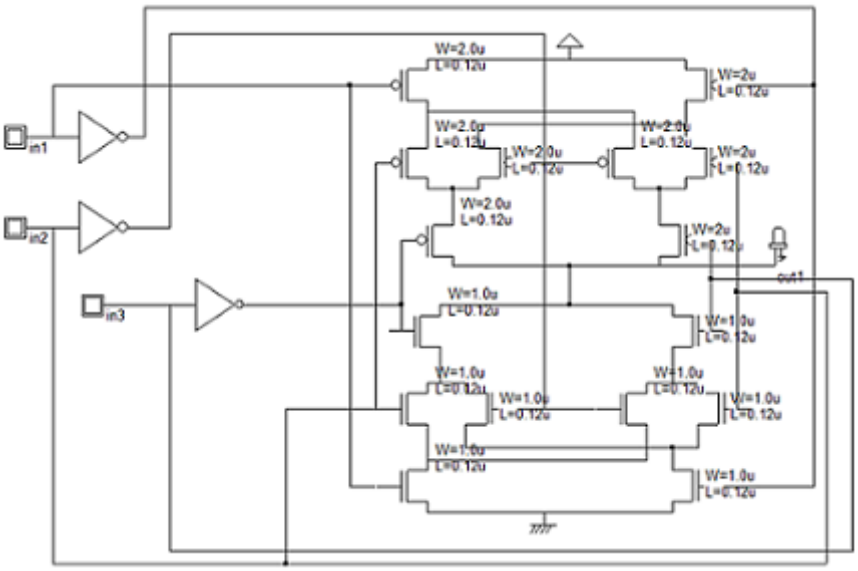

Fig.6 Schematic of Unskwed adder

The pull up circuit of the the adder circuit is designed using the PMOS of channel widths w= 2.0µm and length l=0.12µm , while in pull down circuit width is change to 1.0µm to keep the ratio of current ratios of PMOS to NMOS approx. equal to 1.We have eight different condition of the circuit for the eight input combination from the three input.let's say i.e input is 110 then sum output would be zero, the output terminal would find a connection to the GND. The combination of logic is shown in fig(7),

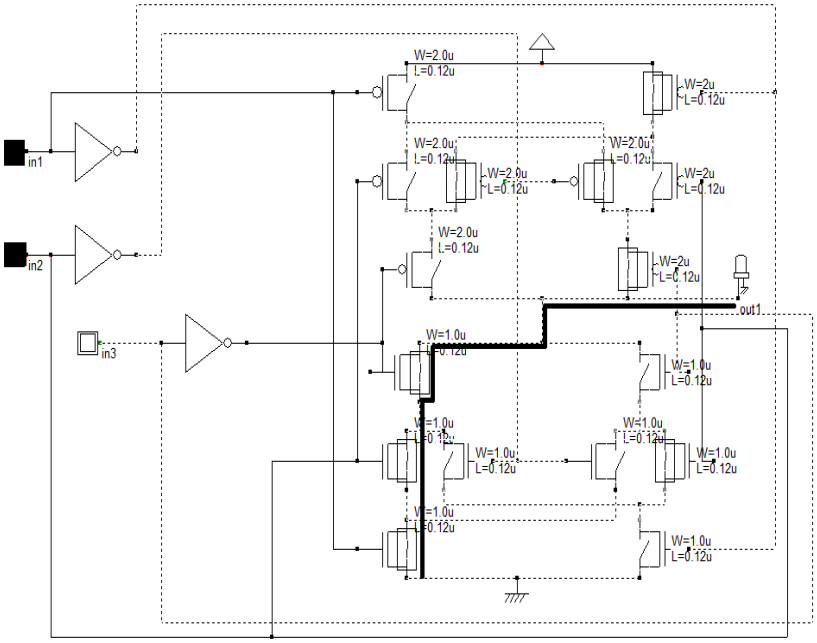

Fig.7 Operation of unskwed addder for i/p110

As shown no path is directly available from vdd to out1 and out1 is directly connected to gnd through three transistor of pull down circuit.Hence this output would be shown by off led at output terminal. The layout of adder designed over microwind is shown in fig (8),the designed logic has the rise delay and fall delay of 0.003ns. this layout has area 38.5X9.8 μm^2 [5]. The output waveform for different inputs is shown in fig(9).fig shows the voltage v/s time

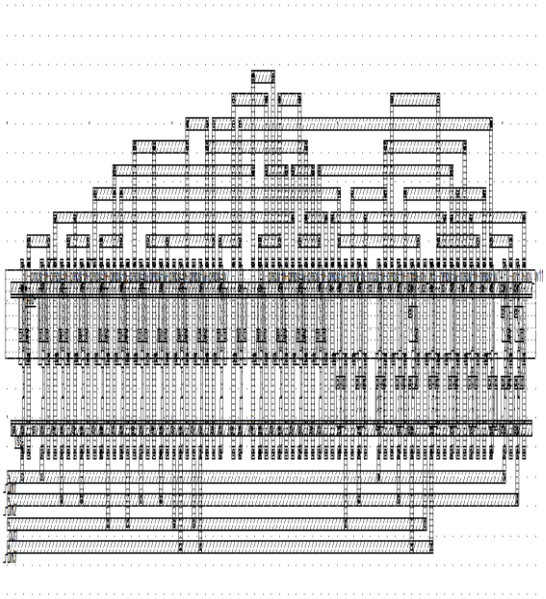

Fig.8 Layout of unskewed adder

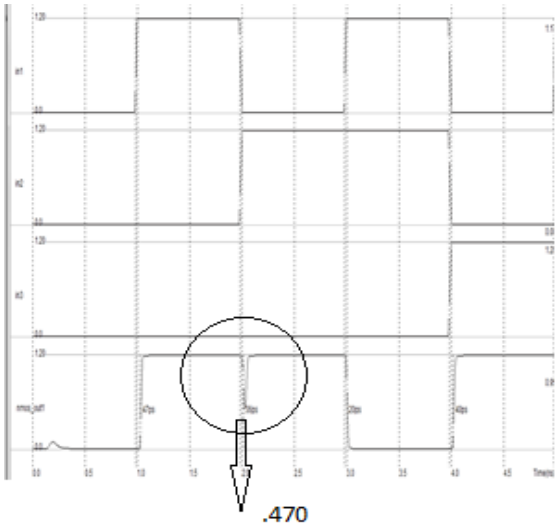

Fig.9 Waveform for unskewed adder

In fig(9), three waveforms from starting are the input waveform I/p 1, 2, 3 respectively and last waveform shows the sum of three inputs. An instant is marked to show, when the input combination changes from 100 to 010 then due to high rise time of 44ps and low fall time of 18ps ,there is a switching in the output between two successive clock[5]. Because the threshold for this conventional design is vdd/2 =1.20/2 i.e 0.60v, while the voltage b/w two clock is down to 0.470v that can switch the sum controlled device to low state and then it has to come to high state[5]. This unwanted switching may reduce the performance of overall system.

IV. Skewed Adder Realisation

As we have seen the unwanted switching in Conventional CMOS design but this switching may be avoided by the use of skewed design methodology hence to remove this effect this design is HI-Skewed by decrease the width of NMOS used in the pull-down circuit. A proposal of high skewed adder designed on DSCH tool is shown in fig (10)

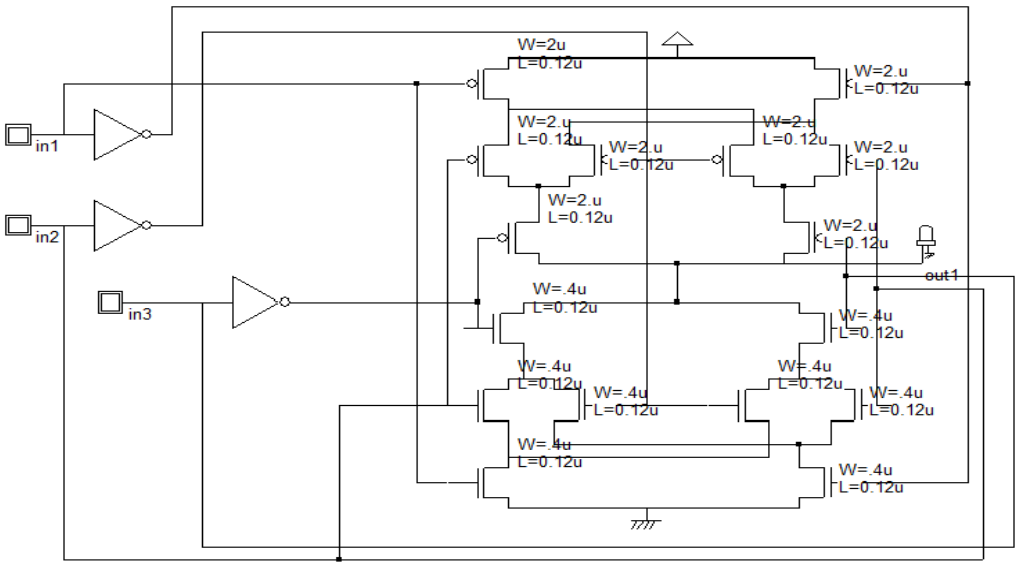

Fig.10 Schematic of skewed adder

Sum is generated at the output for different combination of inputs same as the previous case.A layout of HI-skewed adder and the output waveform voltage v/s time is shown in fig (11)& (12) respectively. This layout has area 38.5X9.8 μm^2 . For the designed CMOS Adder rise delay is 0.004ns and fall delay is 0.002ns. hence this skewing the fall delay transferred to rise delay.

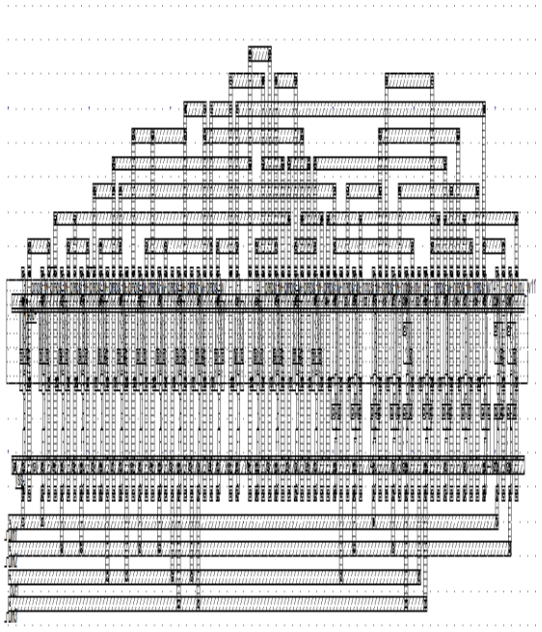

Fig.11 Layout of skewed adder

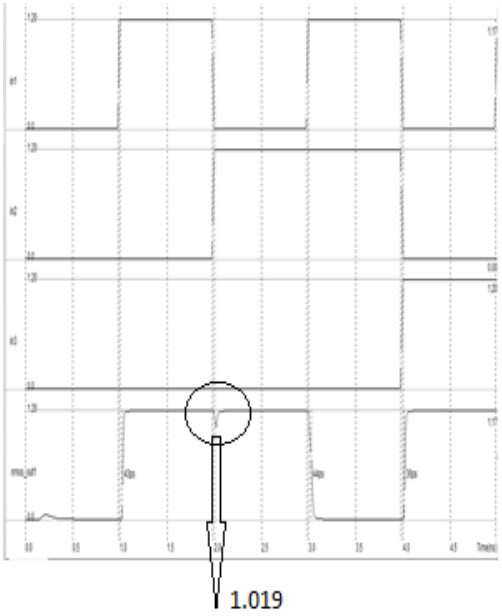

Fig.12 Waveform of skewed adder

As shown the rise time is reduce to 40ps from 44ps and fall time change from 18ps to 39ps which considerably changes the intermediate level b/w the two consecutive clock period. As indicated in fig.11, the intermediate level is approx. to 1.019v, which was 0.470v in the case of unskewed & lower than the threshold so it first switch to lower level & then raise to higher level which decrease the performance in terms of power consumption ,speed and productivity. But 1.019v is much greater than the threshold level hence there is no switch to lower level instead maintained at the same high level and count in higher productivity. The power dissipation in skewed circuit is 17.862µw which is low in comparison to 20.543µw in unskewed adder [5].

V. Conclusion

In this paper we describe full adder design using the skewed CMOS technology. This skewed CMOS technology helps to avoid the unwanted switching by transferring the delay from falling edge to rising edge with a demerit of capacitance and resistance increment. As the result shown above we can say that this skewed technology enhances the compatibility of one logical circuit to other logical circuits and can be used for low power and low voltage application.

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