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Digital Input, low latency, high performance low THD Closed-Loop Class-D Audio Amplifier with up to 192-kHz Audio processing

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Abstract*—A novel audio processing methodology with Dual interpolator option has been proposed using both FIR and IIR methodologies, high resolution noise shaping with high resolution sigma delta modulator with a new nontraditional design with high resolution 9 bit Sigma-Delta modulator has been designed alongside a 9 bit PWM generator. Special features like simplified automatic gain control and dual methods of Spread spectrum mode have been tested and simulated. All simulations are run using MathWorks' MATLAB and Simulink and the results have been verified.*

Index Terms*—FIR – Finite impulse response, IIR – Infinite impulse response, AGL – Automatic gain limit, SSM – Spread spectrum mode, RTL - Register transfer level, FPGA- Field programmable gate array, PCB – Printed circuit board, SNR-Signal to noise ratio, ENOB – Effective number of bits*

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I. INTRODUCTION

Audio processing or sound recording has been the revolution of the modern day sciences ever since the dawn of the acoustic era in 1877 which focused on mechanically recorded audio. The second wave of audio recording hit the world since the invention of electrical microphone sensors invented and perfected around the year 1925. This gave us the power to record, filter, amplify and re-balance audio to a remarkable degree. And thus the profession of audio engineer was dawned. Later towards the end of World war 2, the German invention of magnetic tapes revolutionized the audio industry once again and potable audio electric devices that were fed with magnetic tapes as input were envisioned. This lasted half a century and was still seen in commercial electronic stores till late 2000s. During the 1970s the modern digital era was born and in less than two decades made the all older methods obsolete. The era of disc records and magnetic tapes was buried under the rubble due to huge development in digital audio processing methodologies. Technologies like pulse code modulation introduced in early 70s along with discretized sampling of sound waves at high rates and reconstructed using a Digital to analog converter (DAC) has become the new standard of audio processing. With evolution of CDs and Identify applicable funding agency here. If none, delete this.

DVDs storage and replay ability of audio was improved a thousand fold. Ever since the release of Ry Cooder's Bop 'Til You Drop released in 1979 Digital audio became the new standard. This prospectus discussed the modern way of digital audio processing at par with the latest techniques and methodologies in use with suggested reliable improvements and cost reduced implementations of such improvements with entirely digital side of audio processing through and through the system. It explains the detailed process of over sampling, noise mitigation and power amplification along with digital modifications and control systems employed for better audio quality.

I. BLOCK DIAGRAM

Following is the audio processing block diagram of the proposed architecture. The overall block diagram is explained in Section VI below.

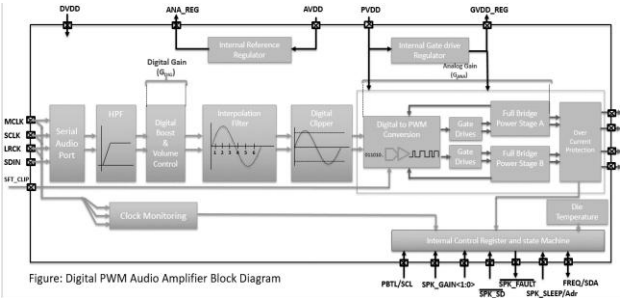

Fig. 1. System block diagram

II. BASIC OPERATION

The basic Operation of the proposed architecture is as follows. An I2S block receives signal from the source and converts it to readable data. It works like a SIPO system. Then, The DC removal filter removes any offset in the input signal. Interpolators increase the sampling frequency by oversampling and filtering the signal. Sigma delta modulator shapes noise such that the SNR is to the desired quality. Later the PWM generator compares audio to a high frequency triangular wave and generates PWM signal. Class D amplifier amplifies the power of the PWM signal and at the output, an LC filter reproduces audio at high power which is connected to the speaker.

III. DC REMOVAL FILTER

If the DC is passed as the input from the corresponding I2S block in certain such cases a decent DC removal filter needs to be employed to remove the DC offset in the audio signal. Placing a zero at DC frequency of 0 Hz is theoretically the right way to go for the task. However, due to this zero the lower frequencies of audio does get affected. Hence the FIR solution is a misfit for this application. So a pole close to z=1 is placed such that effect of zero is nullified for all other frequencies other than that of 0 Hz.

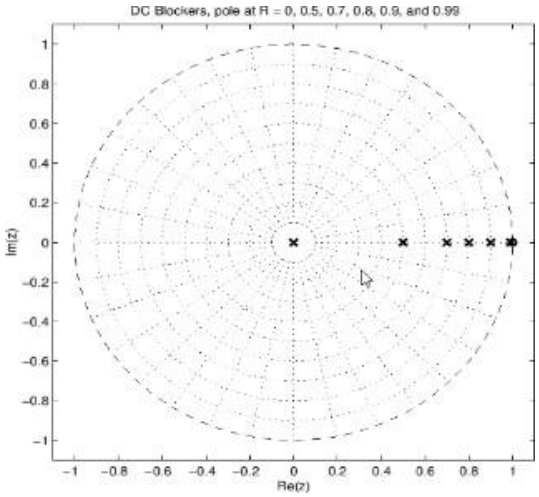

Fig. 2. Z plane plots for DC blocking filter

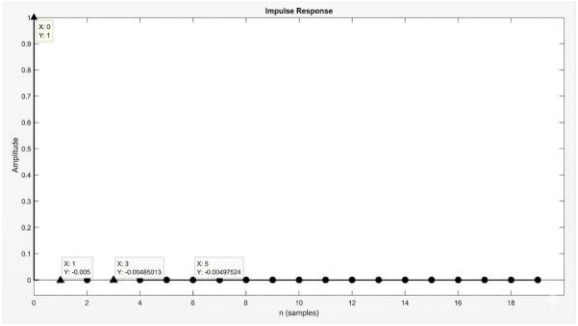

Fig. 3. Impulse response of the DC blocking filter

IV. PROPOSED AUDIO PROCESSOR

The proposed audio amplifier is made of a DSP block for signal processing and rest of the system is design to support the DSP operation. It mainly consists of Interpolators and a Sigma delta noise shaper followed by a PWM generator block. This forms the core of the audio processing system. The process of refining the audio input in done only by the Interpolators and Sigma delta modulator shown below.

The interpolator receives data from an I2S (Inter IC sound protocol block) and the general standard is the audio is sampled at either 44.1 kHz or 48 kHz and is 21 bit in resolution.

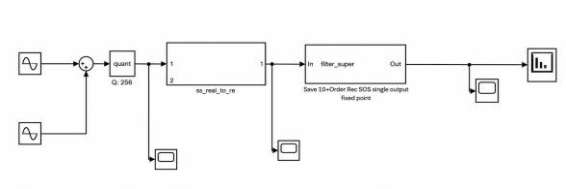

Fig. 4. DSP block diagram

The below image shows 2 separate DSP paths. One with IIR interpolator followed by Sigma delta modulator and other with FIR interpolator followed by the Sigma delta modulator. Each branch further is fed to their corresponding PWM generator blocks and PWM is generated in both AD mode and BD mode. Each of these individual blocks are discussed in detail in the corresponding sections below.

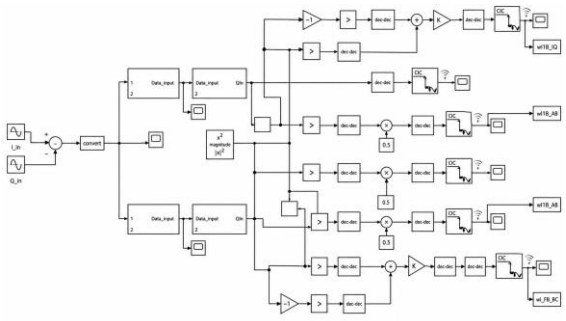

Fig. 5. DSP system block diagram with AD and BD mode

The below diagram shows the proposed overall audio sys-tem with supporting blocks like PLL, I2C (inter IC commu-nication), I2S, clock distribution tree, and control registers followed by the DSP system. And finally a closed loop class D digital audio amplifier is connected to produce sound at the output of the order of 100 W in power.

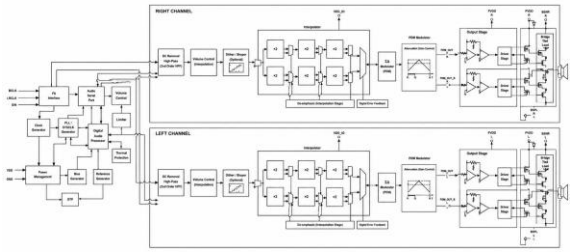

Fig. 6. Audio system block diagram

V. INTERPOLATOR

Nyquist principle says 2 * fin is sufficient to reproduce the true signal. But an oversampled signal gets better approximation to original signal. The quantized output gets closer and closer to true input as sampling rate increases. Because the discontinuities are smoothened out.

Oversampling and low pass filtering will result in better SNR. Such oversampling and low pass filtering are called interpolation filtering. As OSR rises by 2, SQNR increases by 2 which is 3 dB or ENOB increases by 0.5.

This oversampling can't be done infinitely and we therefore go for noise shaping modulator after we have reached the frequency limit.

Interpolator is the oversampling circuit used increase the sampling frequency of audio input and reduce noise power. Also, one must note that processing audio at very low fre-quency of sampling gives bad SNR at 48kHz. But over-sampling all the way to MHz range will cause interference with audio transmission of AM-FM transmissions. So a sweet spot for audio PWM exists between 200kHz and 500kHz range. In the domain of digital signal processing, the term interpolation refers to the process of converting a sampled digital signal (such as a sampled audio signal) to that of a higher sampling rate (Up sampling) using various digital fil-tering techniques (for example, convolution with a frequency-limited impulse signal). In this application there is a specific requirement that the harmonic content of the original signal be preserved without creating aliased harmonic content of the original signal above the original Nyquist limit of the signal (that is, above fs/2 of the original signal sample rate).

Interpolation always consists of two processes:

- Inserting L-1 zero-valued samples between each pair of input samples. This operation is called "zero stuffing".
- Low pass-filtering the result.

The result (assuming an ideal interpolation filter) is a signal at L times the original sampling rate which has the same spectrum over the input Nyquist (0 to Fs/2) range, and with zero spectral content above the original Fs/2 Below image shows an up sampling by a factor of 3.

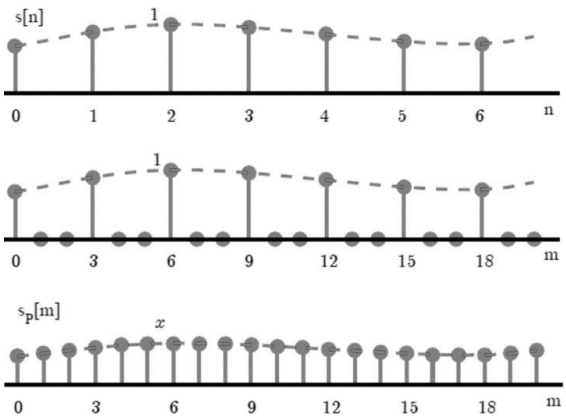

Fig. 7. Interpolation example

A. Types of interpolators

Interpolation is no doubt an intricate process but there is no one right way to do it. Below image shows the multiple interpolation methods supported but not limited to by MAT-LAB tool. Each of them come with their own advantages and disadvantages in terms of adders and multiplier count, group delay, order of interpolation etc.

Here 6 different interpolator circuits namely CIC interpola-tor, CIC compensation interpolator, X[n/3] interpolator, digital up converter along with IIR and FIR Half band interpolators are compared among each other to demonstrate the differences in filter response and group delay [unquantified for demonstra-tion].

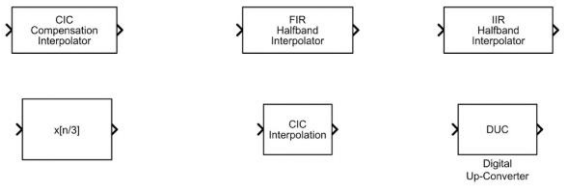

Fig. 8. Types of Interpolators

The below Image shows the individual low pass response of the selected 6 filters and corresponding differences in pass band gain, stop band attenuation, and transition band width are demonstrated below.

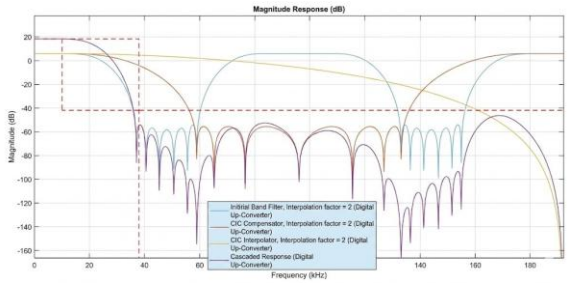

Fig. 9. Magnitude Response of Interpolators

The below graph shows the variation of Group delay with respect to different filters and also the no linear phase impressed as a non-constant group delay in IIR half band interpolator.

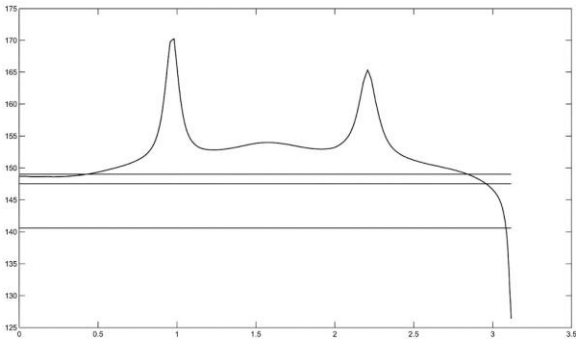

Fig. 10. Group delay of Interpolators

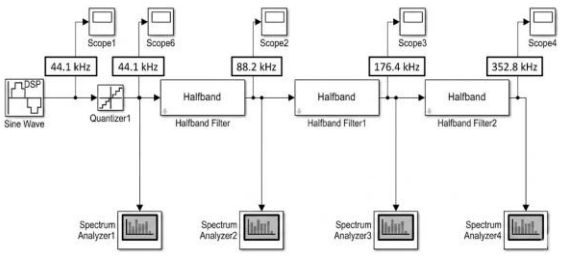

Fig. 11. Typical Interpolator Example

Above figure shows a typical interpolator using half band fitlers. Half band filters have become the modern standard for up-sampling by a factor of 2. They give precise OSR and Fsw of PWM generator is designed to be between 200kHz to 500kHz using this up-sampling technique.

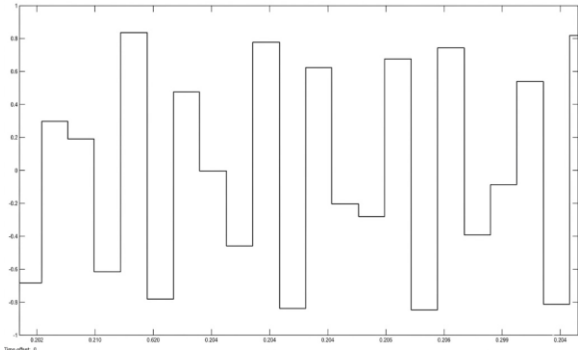

Fig. 12. Typical Interpolator Input example

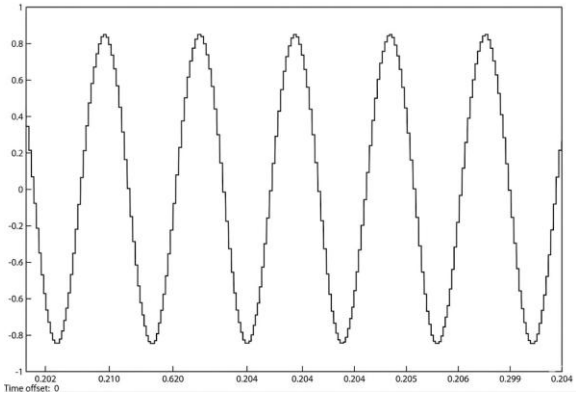

Fig. 13. Corresponding Interpolator Output

VI. FIR INTERPOLATOR

The FIR Half Band Interpolator block performs interpola-tion of the input signal by a factor of two. The block uses an FIR equi-ripple design or a Kaiser window design to construct the half band filters. The block uses an efficient polyphase implementation to filter the input signal. The main advantage of using the FIR half band interpolator is its liner phase and constant group delay. This ensures better fidelity compared to IIR interpolator. Below figure shows the FIR Interpolator and it's polyphase implementation for 3 stage 8x interpolation typically from 48 kHz to 384 kHz.

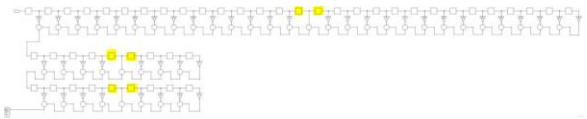

Fig. 14. FIR Interpolator

VII. IIR INTERPOLATOR

IIR Interpolator is a low fidelity high speed interpolator circuit. In comparison to FIR interpolator the audio quality reduces due to nonlinear phase and non-constant group delay. On the other hand, the observed group delay is way too low. Due to this advantage, it can be used for applications where latency is the higher priority over quality in like FPS gaming set ups etc.

In this application the poly phase implementation was chosen to reduce implementation cost and over all area. This implementation is discussed in detail in the references.

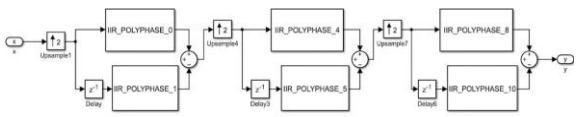

Fig. 15. IIR Interpolator block diagram

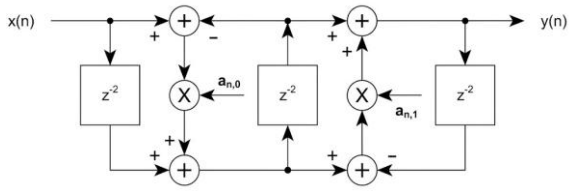

Fig. 16. Poly-phase implementation of IIR Halfband filter

VIII. FIXED POINT DESIGN

Fixed point design is an important step in digital system design process. Since it is impossible to make the filter coefficients infinitely accurate to the last decimal place one must decide the right tradeoff between implementation cost and filter accuracy.

There process of fixed point design involves rounding off the filter coefficients to fixed word length and to reassure the word length is decent enough 2 necessary tests need to be passed.

Firstly, the filter designed with new coefficient of fixed word length is compared with a filter of infinite precision and their frequency responses are compared. On comparison 3 things are measured. Pass band ripple, stop band attenuation and transi-tion frequency. As long as these are within a allowed limit, deviating from the ideal filter, the word length can be chosen for design. If the new filter fails to meet the set standards, word length is increased and so does the implementation cost.

Secondly, a crude way of testing the transient response of the ideal filter and fixed word length filter are compared and the difference between the output is expected to be zero if the word length chosen is decent enough. This is also a function of operating frequency of the filter. If the difference is non zero at any point, the word length is increased further and this iterative process continues.

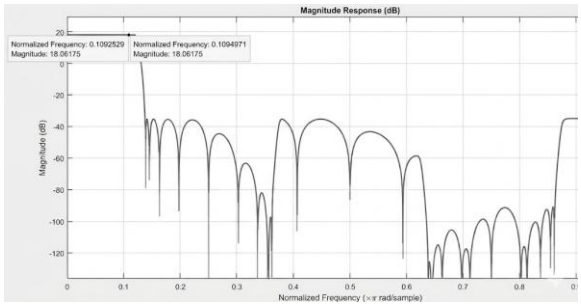

Fig. 17. Frequency response of fixed point design vs original design

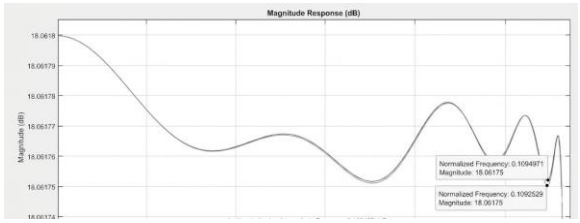

Fig. 18. PassBand response of Fixed point design vs Original Design

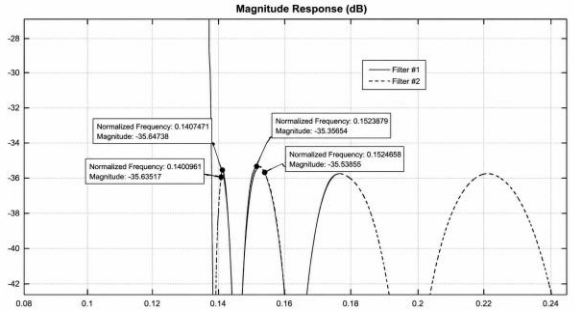

Fig. 19. StopBand Comparison of fixed point design vs Original design

IX. SIGMA DELTA MODULATOR

In the section above we have seen how oversampling is a good way to reduce noise power. But, with every doubling of oversampling frequency only improves the output by half a bit. Hence using a sigma delta noise shaper is much better approach to improving the signal to noise ratio.

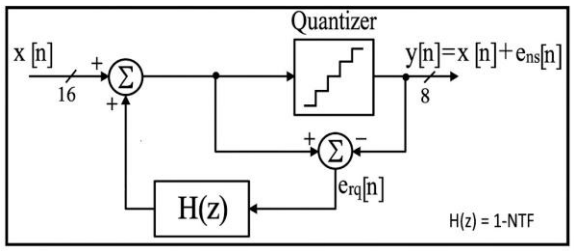

Fig. 20. sigma delta modulator loop

Matlab comes with a decent toolbox called the delta sigma tool box developed by Prof. Shanthi Pavan and Prof. Richard Schreier. It does all the work behind improving SNR, ENOB and limiting out of band gain, while keeping MSA decent. And a typical example is shown below.

A. Typical IIR CRFB implantation

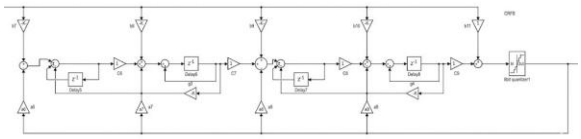

Fig. 21. Typical CRFB Architecture

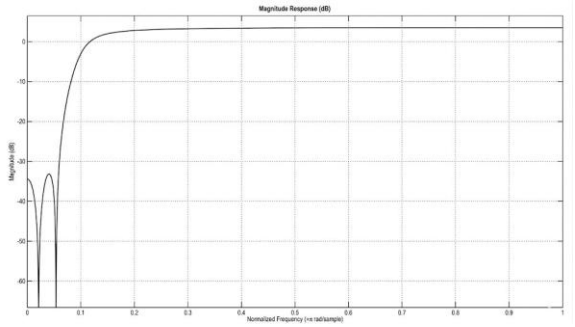

Fig. 22. high pass response of crfb modulator

B. Non traditional approach proposed

The non traditional approach proposed below, doesn't use the traditional method of sigma delta modulator design and instead works on the principle of designing a high pass filter specifically designed to make sure the NTF tranfer function is a good high pass filter in general and OOBG is decently suppressed using FIR high pass filter.

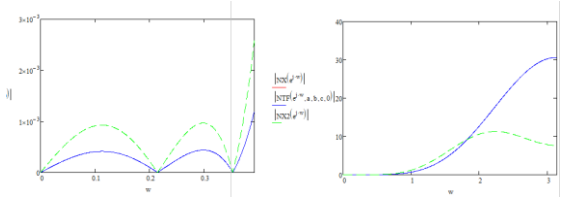

Fig. 23. Non Traditional SDM High pass Design

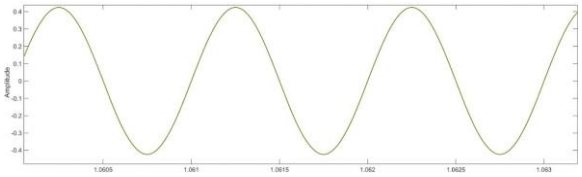

Fig. 24. SDM Input

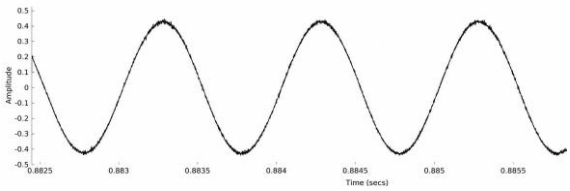

Fig. 25. SDM Output

C. MSA of Sigma delta modulator

Due to the noise shaping action the out of band gain keeps increasing as we make the high pass filter more and more precise. Also, the low bit quantizer which behaves as high bit quantizer loses it's property at maximum amplitude region. Because of this at some signal amplitude the sigma delta modulator loses it's property to shape the noise properly. This amplitude at which noise shaping is good enough to give us a decent SNR is called the Maximum signal amplitude (MSA) of the sigma delta modulator.

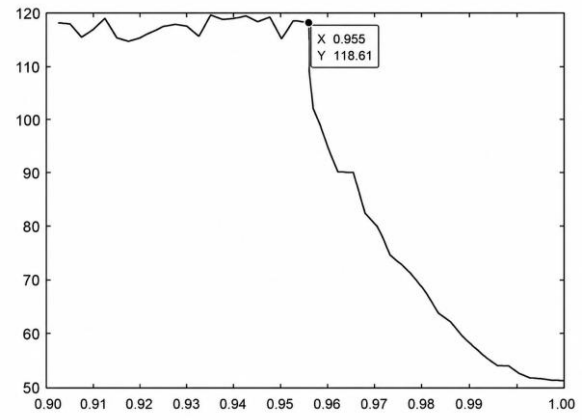

Fig. 26. MSA of the Proposed SDM loop

TABLE I
COMPARISON OF FIR AND IIR DESIGN COST AND RESULTS.

SL	Parameter	FIR/IIR	Description
1	Order	7 / 5	ΣΔ Converter order
2	Quantizer	8 / 8	Quantizer bits
3	SNR	114 / 105	Signal-to-Noise Ratio (dB)
4	OOBG	11.2 / 8.2	Out of band gain (V/V)
5	OOBG(dB)	21 / 18.3	Out of band gain (dB)
6	F OOBG	136 / 140	Max OOBG freq (kHz)
7	Band Edge	24 / 24	Audio band edge (kHz)
8	OSR	8 / 8	Oversampling ratio
9	F SW	384 / 384	Switching freq (kHz)
10	F OP	192 / 192	Master clock (MHz)
11	Adders	1 / 1	Adders used
13	Multipliers	7 / 5	Multipliers used
14	Delay	6 / 4	Delay elements
15	Cost	14 / 10	Implementation cost
16	MSA	0.95 / 0.97	Max signal amplitude
17	ENOB	19 / 17	Effective bits

X. PWM GENERATOR

In an analog audio amplifier, a continuous triangle wave is compared to the signal input to generate PWM. However, in case of a digital amplifier, the samples are precisely timed and the triangular wave also needs to be discreet in time to generate the PWM. In each sample space the counter has to go from 0 to 2 to the power n and count all the way back to 0 in 1 sampling cycle, where n is the number of bits in the quantizer of the sigma delta modulator.

XI. SYSTEM INTEGRATION RESULTS

The blow graph shows the effective outputs of different architectures along with modem BD mode of operation.

A. IIR

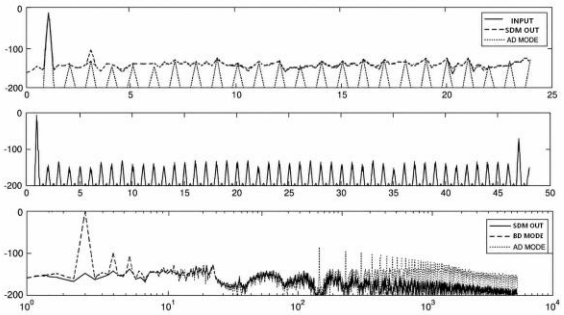

Fig. 27. FFT of SDM output and BD mode for IIR interpolation path

B. FIR

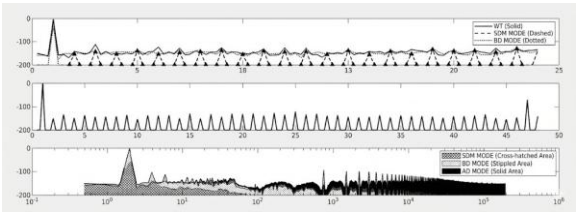

Fig. 28. FFT of SDM output and BD mode for FIR interpolation path

Parameter	IIR+SDM	FIR+SDM
Signal SNR (dB)	135.06	135.06
Interp. SNR (dB)	115.54	111.26
SDM SNR (dB)	121.62	121.16
MSA	0.965	0.956
MSA fixed	0.955	0.955
THD %	0.00002	0.00002
SNR (AD mode)	120.44	119.79
SNR (BD mode)	120.95	120.90
SDM ENOB	20.2	20.12

TABLE II
COMPARISON OF IIR AND FIR INTERPOLATOR SYSTEM PERFORMANCE.

Parameter / Path	Value
Overall Delay	
IIR + SDM (BD/AD)	60 μs
FIR + SDM (BD/AD)	370 μs
Group Delay (Interpolator)	
IIR Interpolator	24
FIR Interpolator	129
Implementation Cost	
IIR Interpolator	8M+16A
FIR Interpolator	44M+41A
Sigma Delta Modulator	8M+9A
Summary	
Total Cost	60M+66A
Total Used	52M+57A

TABLE III
SYSTEM PERFORMANCE AND IMPLEMENTATION COST SUMMARY.

XII. AUTOMATIC GAIN LIMIT

A novel method of automatic limit or has been proposed here using an averaging in circuit. If the average of input signal courses beyond the set limit, the gain Limiter goes into attack mode. During attack mode the gain of the audio amplifier is ready for to in small steps of 50 ms. similarly, if the gain has been reduced for prolonged time the audio average is below a certain set limit then recovery mode kicks in. during the recovery Mode gain increases from lower threshold to 1 or zero dbfs from the set lower limit in total steps of 300 milliseconds. this ensures that the gain of the amplifier is automatically adjusted depending upon the attack and recovery thresholds of the automatic gain limiter.

In improved application of the proposed architecture differ-ent high pass low pass and Band pass circuits can be used and average individually to remove specific frequency noises or specific frequency spikes in the audio.

After the attack face is triggered, hold face comes into action to ensure that the attack circuit has enough time to execute The Attack operation. Once after the whole time is complete the circuit decides whether to continue in the hold Phase or to Trigger recovery depending up on the average of the input signal this automatic gain limiter is not part of the audio processing path however the gain control bits part of the audio processing path and can be inserted before the

RMS >Atk	RMS >Rec	Gain=1	Action
0	0	0	Recover
0	0	1	Continue (no Action required)
0	1	0	Recover
0	1	1	Continue (no Action required)
1	0	0	Condition Doesn't exist
1	0	1	Condition Doesn't exist
1	1	0	Continue (no Action required)
1	1	1	Attack

TABLE IV
LOGIC TABLE FOR RMS THRESHOLDS AND GAIN

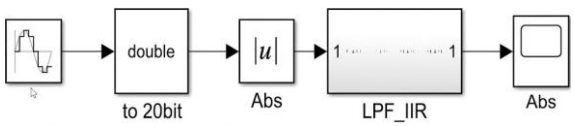

Fig. 29. Averaging filter design

the below point show the implementation of the automatic gain limiter and the corresponding action taken by each stage during attack phase, recovery phase and continuation phase; and the time consume during the action of each phases.
Attack Hold Recovery Continue [Precedence order]
If attack is triggered. Decrease the gain from 1 to 0.875 or (0.75) in 50ms
Na = Gain Bits*(1-0.75)*50m*fs clock cycles.
If recovery is triggered. Increase the gain from 0.75 to 1 in 300ms
Nr = Gain Bits*(1-0.75)*300m*fs clock cycles.

XIII. CLASS D AMPLIFIER

A Class-D audio amplifier or switching amplifier is a non-linear amplifier with very high power efficiency due to high switching frequency and switching losses. The advantage of using class D amplifiers is no liner elements are required for power amplification, thus no biasing and no power leakage from VDD source to ground.
The below figure shows the first order closed loop Class D amplifier where the D stage represents the power stage or the driver stage.

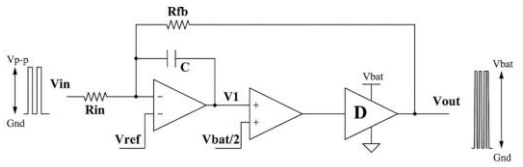

Fig. 30. 1st order class D amplifier

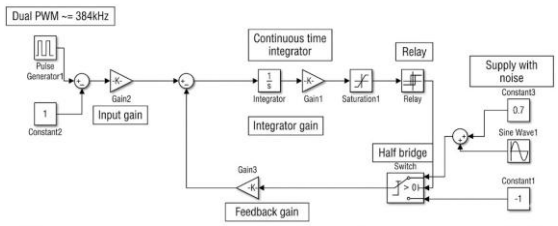

Fig. 31. Closed loop class D with supply noise

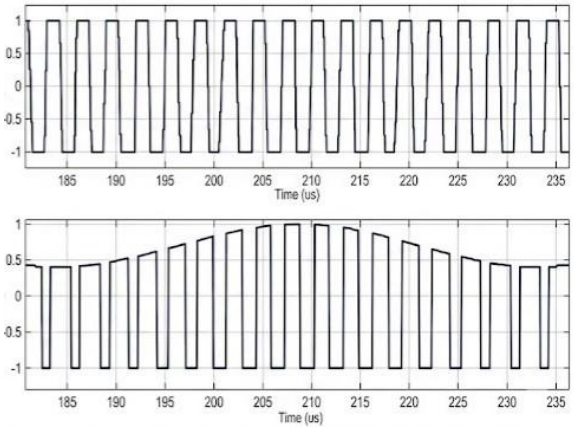

Fig. 32. Class D input and output PWM adjusting to supply noise

Above image shows how the closed loop class D amplifier does power supply noise correction in terms of pulse width. This feature ensures there is decent SNR at the output at the audio amplifier.
Since, the Matlab model for audio processing is mathemat-ical, a linearized closed loop class D model is demonstrated below. The design process is explained in detail in the refer-ence below.

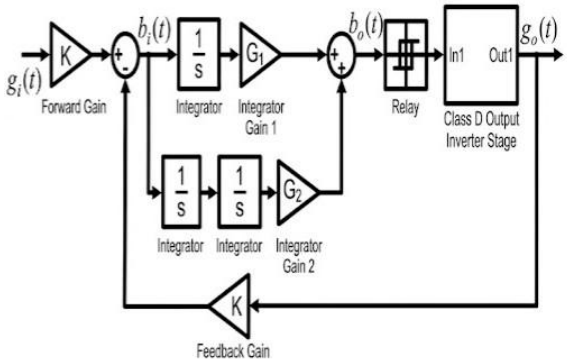

Fig. 33. second order Class D amplifier linearized model

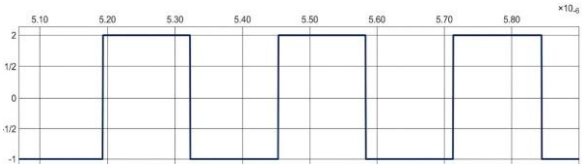

Fig. 34. second order Class D input

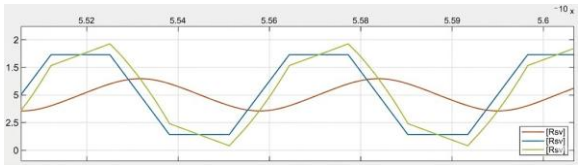

Fig. 35. second order Class D output

Using Class D amplifier of second order ensures higher THD and improves SNR. However, the modern cases even fourth order solutions are also in development.

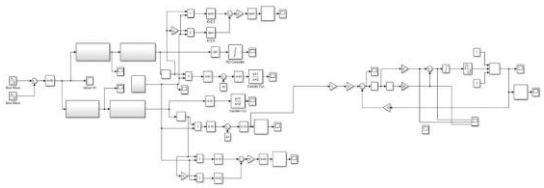

Fig. 36. Total DSP MATLAB MODEL

XIV. CONCLUSION

The fully digital closed Loop class D amplifier with dual channel Interpolation and noise shaping has been simulated and the results are tabulated. A novel and simplified automatic gain limiter has been introduced. All, parameters of weightage like SNR, THD, ENOB etc., have been measured. All simu-lations are verified in Matlab Simulink.

XV. FUTURE SCOPE

The future scope lies in implementing the FPGA for the proposed architecture using RTL code generation and verifi-cation alongside a separately implemented PCB of closed loop class D amplifier, testing the results in terms of SNR, THD, EMI and other standardized parameters and then proceeding with Silicon implantation. To improve on architecture and implementation methodology in individual phases and top level integration if and where necessary.

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