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Design of Low Noise and Low Power BGR Current Reference for Bio-Medical Applications

Vishwanath D Tigadi
Lead Design Engineer Tessolve Semiconductor PVT LTD
Hubballi, India

Gautami Karkun
Senior Lead Design Engineer Tessolve Semiconductor PVT LTD Hubballi, India

Laxman Patil Kulkarni
Lead Design Engineer Tessolve Semiconductor PVT LTD
Hubballi, India

Abstract*—With rapid advancement in biomedical technology especially on the neurology and neuro-electronic sensors, the bionics industry has been seeing a boom. These bionic sensor chips with high precision ADCs sensing voltages of the order of few hundred µV require constant bias and references immune to their own noise as well as the external noise. This paper discusses in detail about the high Power Supply Rejection Ratio (PSRR) (of the order of 60dB) and low noise (of the order 100pA/Hz²) current references for these ADC and Amplifiers. An improved method to supress 1/f noise of the circuit using pseudo resistor based lowpass filter has been implemented. A statistical data has been analysed using Monte-Carlo analysis. The proposed architecture has been designed in TSMC 180nm technology and the results have been discussed.*

Index Terms*—Total integrated noise, ADC, PSRR, PVT, MC*

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I. INTRODUCTION

The evolution of Bio medical science in the past two decades has been exponential. These are the specialized tools designed to diagnose, monitor, treat and alleviate diseases and injuries which tremendously increases the quality of life as well as quality of patient care. Electronics taking over the mechanical systems in medicine has been possible due to improvement in the field of electrical sensors and data processing. High precision sensors and data converters and processors enable proper monitoring of patient health leading to low risks and low mortality overall in the medical industry. The advancing Biomedical applications enabling continuous monitoring of wearable personalized healthcare, which enable continuous monitoring of physiological signals like EEG, ECG etc., today's biomedical devices sense, monitor and control heart rate, oxygen consumption, blood pressure and more from a device as small as a wearable digital wrist band. People who are completely paralyzed have been able to play complex computer games due to advancement in EEG systems. Central to all these lie the analog front-end sensors and signal processors. High precision signal amplifiers and ADCs make the heart of these AFE systems, and these systems are only as good as the reference signals that are provided to them. This paper will discuss in detail design process of de-signing of a BGR core. Mitigating temperature drift. Low frequency PSRR implementation using low gain architecture of a modified folded cascode amplifier and process based current trimming using thermometric decoder. This paper will also discuss in detail about the noise mitigation by source degeneration and noise filtering using pseudo resistor.

II. PROPOSED ARCHITECTURE

A. BANDGAP REFERENCE CORE

A bandgap reference circuit is a precision reference gener-ation circuit to provide constant DC reference typically across temperature and power supply variations. This works on the principal of cancellation of opposing temperature coefficients. The BJT has a CTAT voltage response.

$$\frac{\delta V_{CTAT}}{\delta T} \approx \frac{-2mV}{C} \quad (1)$$

And pumping same current in a larger BJT gives CTAT voltage response of different slope. Subtracting these 2 voltages gives a PTAT response.

$$\Delta V_{PTAT} = V_T \ln(n) \quad (2)$$

$$\frac{\delta V_{PTAT}}{\delta T} \approx \frac{0.087mV}{C} \quad (3)$$

In the end PTAT branch current and CTAT branch current are added to create a ZTAT current in the BGR core. This is embedded within the chip to ensure that high sensitivity elements like ADCs and DACs are given proper reference voltages or currents. The architecture shown below represents a low noise current reference generation topology.

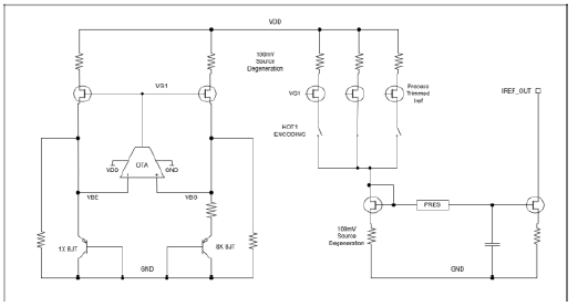

Fig. 1. BGR Core with Hot 1 encoding

$$I_{ZTAT} = \frac{\Delta V_{BE}}{R1} + \frac{V_{BE}}{R2} \quad (4)$$

The architecture above shows a typical ZTAT reference generation core. Additional resistances are added with 100mV drop across them to add source degeneration and mitigate noise. The ZTAT current in the core is then mirrored to the reference branch which is designed with HOTONE encoding method to scale the current from 0.5µA to 1.5µA in steps of 0.5µA. These three HOTONE encoded branches are trimmed with 3:7 thermometric decoder branch currents carrying 5 % of each branch current. This trimmed, low noise current is then pumped into diode connected N channel mosfet.

TABLE I
HOT 1 ENCODING FOR IREF OUT SELECTION

SL.NO	Iout	HOTCODE0	HOTCODE1	HOTCODE2
1	0.5µA	1	0	0
2	1µA	0	1	0
3	1.5µA	0	0	1

The N channel current mirror also contains a 100mV source degeneration to mitigate noise. Along with this, a low pass filter designed using MIM capacitor and a pseudo resistor is added to filter all frequency noise above 0.1Hz. This filters out all the high frequency noise from the core and the trim branches. On the output side, the only noise comes from the mirror mosfet itself and that is mitigated by source degeneration as mentioned above.

B. MODIFIED FOLDED CASCODE OTA

The OTA forms the center part of the BGR core which maintains the CTAT Voltage at both its input terminals such that the slope of the current in the BGR core's current mirror can be controlled through a resistor. The OTA also helps in maintaining the PSRR of the BGR at desired levels by having high DC gain.

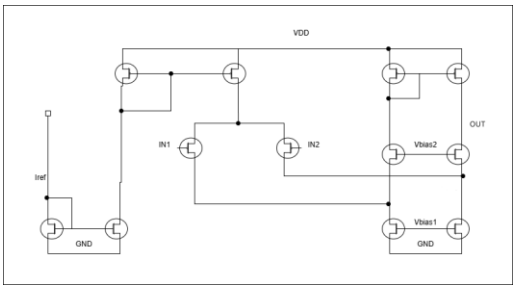

Fig. 2. Modified Folded Cascode OTA

The proposed OTA is a modified version of the folded cascode amplifier where the gain is sacrificed to get proper bias at low currents. This is achieved by discarding the cascode part of the current source on the output legs of the OTA. This action reduces the gain by an order of internist gain of the mosfet. This will also directly affect the PSRR of the BGR.

However, if the reference generated is designed to be used in bio medical implants, power consumption becomes crucial. The noise that is generated due to the decreased PSRR is filtered away using a low pass filter designed using MIM capacitors and pseudo-resistors as discussed in section below.

C. THERMOMETRIC DECODER FOR PROCESS TRIM

A Thermometric Decoder in simple words measures how many 1s are in a binary representation of a number. This is an important part of the BGR process trim design. In this design the main branch is expected to carry 80 % of the expected current and a 3-bit thermometric decoder controls 7 branches that carry 5 % of the expected output current. Hence the output can be increased or decreased by +20 % in slow corners and –15 % in the fast corners.

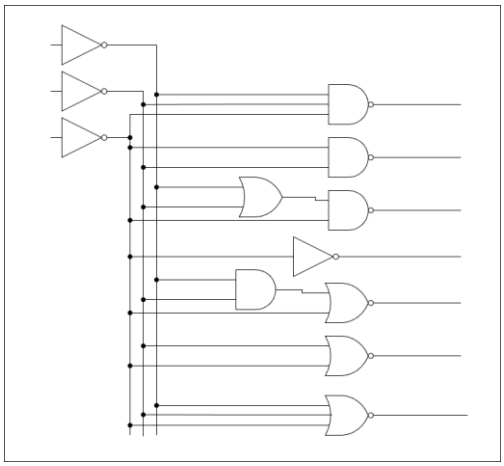

Fig. 3. Thermometric Decoder

In this case, the output current of trimmed branch is directly increased or decreased by adding and removing the current branches in parallel. And thermometric decoder provides proper scaling using a 3:7 decoder implementation.

TABLE II
THERMOMETRIC DECODER TRUTH TABLE

Trim2	Trim1	Trim0	O6	O5	O4	O3	O2	O1	O0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

This is used to fine tune the reference currents across Process Voltage and Temperature(PVT) and Monte Carlo mismatch (MC) as shown above in fig.1 to generate process trimmed Iref.

D. PSEUDO RESISTOR AND LOW PASS FILTER

Pseudo resistors are used to set common mode feedback in the PGA. Also, it eliminates the offsets in the low frequency range of the biomedical signals is between 0.1 Hz and 10 kHz, while the amplitude range is around 20 µV – 10 mV. But the offset of the amplifier itself ranges between 1 mV and 50 mV. In such cases a high pass filter needs to be implemented using a pseudo resistor and capacitor combination. The body diode of the mosfet under 0.2 V forward bias acts as a large resistance. And since the allowed capacitors to pack on chip cannot exceed few pF. By this relation a low pass filter is designed using the relation f=1/(2 * Pi * RC).

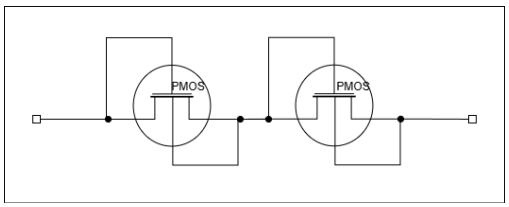

Fig. 4. P mos based Pseudo Resistor

$$I = I_s(e^{\frac{V}{nV_T}} - 1) \qquad (5)$$

These pseudo resistors offer resistance from order of MΩ to TΩ. depending upon the technology, fabrication, and the design node. Separate experimental tests with ideal capacitor needs to be run with simple 1st order filters to determine the pseudo resistance. It is also crucial to ensure the body diode models are accurate. A low pass filter of the order of 0.1Hz is added with this pseudo resistor. Generally, MIM cap of the order of few pF is preferred for this filter design.

III. SIMULATION RESULTS

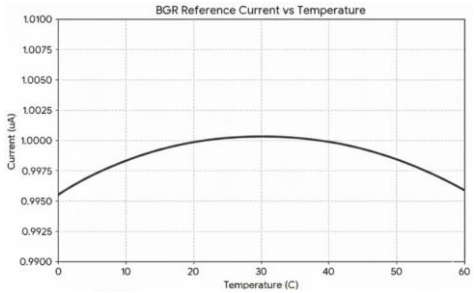

Fig. 5. Typical corner Temperature sweep graph Iout vs Temp

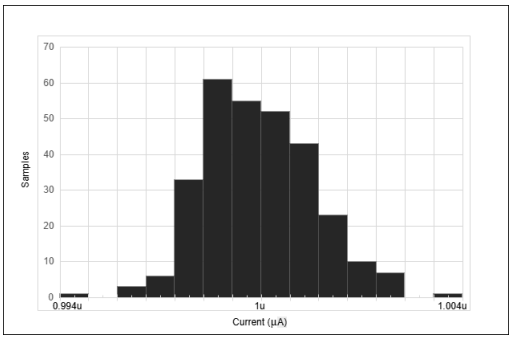

Fig. 6. MC simulation for Iout Spread

TABLE III
SPECIFICATION COMPLAIN ACE MATRIX

Parameter	Description	Min	Typical	Max	Units
VDD	Supply Voltage	1.62	1.8	1.98	V
TEMP	Ambient Tempe	0	25	60	℃
IQ	VDD Current	4.12	4.44	5.12	µA
PD	Power Dissipation	7.91	7.99	8.29	µW
Iout	Output Current	0.994	1.001	1.006	µA
STEP	Step Size	0.5	1	1.5	µA
Noise	2Hz to 250Hz	17.5	51.3	102.1	pA/Hz²
PSRR	DC PSRR	59.1	60.25	64.12	dB
PSRR	PSRR 250Hz	59.09	60.25	64.11	dB
Area	Layout area	-	0.24	-	mm²

TABLE IV
COMPARISON WITH EXISTING DESIGNS

Parameter	This work	[13]	[10]	[11]	[12]
Technology(µm)	0.18	0.18	0.04	0.16	0.13
Voltage(V)	1.8	1.8	1.8	1.8	3.3
IQ(µA)	5.12	50	25	55	120
Vref(V)	1.12	0.6	1.2	1.0875	1.16
TC (ppm/°C)	1.2-10.5	0.33-12.5	9.6	12	13.5
TEMP(°C)	0,60	-40,125			
Noise(µV RMS)	102pA/Hz²	3	1.9	6.1	175
Chopper	NO	NO	YES	YES	YES

IV.CONCLUSION

The BGR based current reference design for low noise and low power applications has been implemented. The component selection and design methodology has been explained. The fig-ures of merit and simulation results have been discussed. The advantages of the techniques introduced and the drawbacks of traditional amplifiers have been discussed in detail.

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