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Modeling and Simulation of Single Phase Half Bridge Shunt APF

V. R. Gaikwad¹, S. N. Kore²

¹(Department of Electronics Engineering, Walchand College of Engineering, Sangli, Maharashtra, India) ²(Department of Electronics Engineering, Walchand College of Engineering, Sangli, Maharashtra, India)

ABSTRACT: Domestic electrical appliances like compact fluorescent lamp (CFL), television (TV), personal computer (PC), etc. use electronic switching technique. They create harmonics on power supply lines and are classified as Nonlinear loads. These harmonics are harmful to other loads and contribute to power loss. The power quality can be maintained by using an efficient Active Power Filter (APF). An expression for the ON time of MOSFET, in single phase half bridge shunt APF, was derived and expressed as a function of phase voltage, compensating current and dead time. The expression was tested by building an APF model in Matlab - Simulink. Simulation results show that, the Total Harmonic Distortion (THD) is reduced below 5%.

Keywords: Fourier transforms, Power quality, Pulse width modulation (PWM), Rectifiers, Total harmonic distortion (THD)

INTRODUCTION

Electricity is generated, transmitted and distributed in the form of Alternating Current (AC). Loads on the AC power supply lines are of two types, Linear load and Nonlinear load. A linear non resistive load causes phase difference between phase voltage and line current (Fig. 1). On the other hand, a nonlinear load creates harmonics on the power supply lines (Fig. 2 and Fig. 3). The harmonics created by a nonlinear load on the power supply lines cause serious effects like, overheating of distribution transformer, overheating of power factor correction capacitor, interference with communication equipments, etc. The end result is reduction in efficiency of power transmission, distribution and utilization. THD is a measure of the effective value of the harmonic components of a distorted waveform. IEEE 519-1992 recommendation allows a THD of 5% in low voltage grids. The Power factor (pf) and THD for domestic loads is presented in table 1. The table clearly indicates that, the THD due to domestic loads like, Fluorescent lamp, Television and Personal Computer, is beyond the limit proposed in the IEEE 519-1992 recommendation. APF is one of the solutions to eliminate harmonics and improve power factor [1]-[3].

| Load | pf | THD (%) |
|-----------------|------|---------|
| Florescent Lamp | 0.89 | 39.5 |
| TV | 0.63 | 121 |
| PC | 0.58 | 140 |
| | | |

Table 1. Domestic Electrical Loads



Figure 1. Phase voltage and current with linear load



Figure 2. Current drawn by nonlinear load



Figure 3. FFT of current drawn by nonlinear load

A single phase half bridge shunt APF is connected in parallel with the nonlinear load (Fig. 4). The nonlinear load draws current i_l (Fig. 5). When APF is not connected, the nature of source current i_s is same as i_l . When APF is connected, in shunt with the nonlinear load, it generates compensating current i_c such that i_s becomes sinusoidal. The fundamental current component of i_l is calculated using Fast Fourier Transform (FFT) [2] and is used as reference current i_{ref} (Fig. 6). The compensating current i_c , is obtained by subtracting i_{ref} from i_l (Fig. 7). It is generated by controlling the ON time of MOSFET's M1 and M2, in the half bridge.



Figure 4. Single phase half bridge shunt APF

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Figure 7. Compensating Current (i_c)

0.23 Time (s)

0.25

0.26

0.24

0.21

0.22

ANALYSIS II.

Let the instantaneous source, nonlinear load and compensating current be $i_s(t)$, $i_l(t)$ and $i_c(t)$ respectively. Applying KCL at node A, : 4

$$i_{s}(t) + i_{c}(t) = i_{l}(t)$$

$$i_{c}(t) = i_{l}(t) - i_{s}(t)$$
The shunt APF makes,
(1)

 $i_s(t) = i_{ref}(t)$ (2)

where,

 $i_{ref}(t) = I_m \sin(2\pi f t)$

 I_m is peak value of fundamental in load current

From (1) and (2)

$$i_c(t) = i_l(t) - i_{ref}(t)$$

Sampling at frequency f_s ,

$$i_c(n) = i_l(n) - i_{ref}(n)$$
where,
(3)

$$i_{ref}(n) = I_m \sin\left(2\pi\left(\frac{n}{N}\right)\right)$$

 I_m is calculated using Discrete Fourier Transform (DFT),

$$I_m = 2 \left| \frac{1}{N} \sum_{n=1}^{N} i_l(n) e^{-j2\pi \left(\frac{n-1}{N}\right)} \right|$$

The sampling frequency f_s determines the accuracy of i_c . Therefore, f_s is selected to be at least 250 times the fundamental frequency *f*. Equation (3) is used to model the compensating current generator block.

 $v_s(t)$ is a sinusoidal function with period T = (1/f). It can be approximated as a linear function, during switching period $T_{sw} = (1/f_s) \ll T$ (Fig. 8).



Figure 8. Phase Voltage and VSI Output

In the interval,
$$0 \le t \le T_{sw}$$

 $v_s(t) = \frac{v_s(T_{sw}) - v_s(0)}{T_{sw}}t + v_s(0)$
(4)

let,

$$k = \frac{v_s(T_{sw}) - v_s(0)}{T_{sw}}$$
(5)

From (4) and (5)

$$v_s(t) = kt + v_s(0) \tag{6}$$

During the interval, $0 \le t \le T_{sw}$, the output of VSI is,

$$v_{o}(t) = 0 \qquad 0 \le t < t_{1} \quad M1 \; OFF \; M2 \; OFF$$

$$= V_{c} \qquad t_{1} \le t < t_{2} \quad M1 \; ON \; M2 \; OFF$$

$$= 0 \qquad t_{2} \le t < t_{3} \quad M1 \; OFF \; M2 \; OFF$$

$$= -V_{c} \qquad t_{3} \le t < T_{sw} \quad M1 \; OFF \; M2 \; ON$$

 V_c is the voltage across capacitor. It is assumed to be constant during the switching interval because of large value of capacitor and small switching period [1]. So, the capacitor is modeled as a DC voltage source. However, in practice the charge lost by the capacitor is restored by periodically pumping charge in capacitor.

In the interval, $0 \le t \le T_{sw}$, MOSFET M1 is ON for time T_{on} , MOSFET M2 is ON for time T_{off} and both are OFF for time $2T_d$. $T_{sw} = T_{on} + T_{off} + 2T_d$ (7)

The inductor connected between the AC voltage source and the Voltage Source Inverter (VSI) converts the VSI into current source inverter. Applying Kirchhoff's voltage law to the loop formed by the AC voltage source, inductor and VSI,

$$v_o(t) = v_s(t) + i_c(t)R + L\frac{di_c}{dt}$$

Integrating both the sides taking limits from $0 \le t \le T_{sw}$

$$\int_{0}^{T_{sw}} v_{o}(t)dt = \int_{0}^{T_{sw}} v_{s}(t)dt + \int_{0}^{T_{sw}} i_{c}(t)Rdt + \int_{0}^{T_{sw}} Ldi_{c}(t)$$

$$\int_{1}^{t_{2}} V_{c}dt - \int_{t_{3}}^{T_{sw}} V_{c}dt = \int_{0}^{T_{sw}} (kt + v_{s}(0))dt + \int_{0}^{T_{sw}} i_{c}(t)Rdt + \int_{0}^{T_{sw}} Ldi_{c}(t)$$

$$V_{c}\int_{t_{1}}^{t_{2}} dt - V_{c}\int_{t_{3}}^{T_{sw}} dt = k\int_{0}^{T_{sw}} tdt + v_{s}(0)\int_{0}^{T_{sw}} dt + R\int_{0}^{T_{sw}} i_{c}(t)dt + L\int_{0}^{T_{sw}} di_{c}(t)$$
(8)

The area under the compensating current waveform during the interval $0 \le t \le T_{sw}$ is,

$$\int_{0}^{T_{sw}} i_c(t)dt = \frac{T_{sw}}{2} \left(i_c(T_{sw}) + i_c(0) \right)$$
(9)

From (5), (8) and (9)

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$$\begin{split} V_{c}(t_{2}-t_{1})-V_{c}(T_{sw}-t_{3}) &= \left(\frac{v_{s}(T_{sw})-v_{s}(0)}{T_{sw}}\right) \left(\frac{T_{sw}^{2}}{2}\right)+v_{s}(0)(T_{sw})+\frac{T_{sw}}{2}\left(i_{c}(T_{sw})+i_{c}(0)\right)R+L\left(i_{c}(T_{sw})-i_{c}(0)\right)\\ V_{c}(T_{on}-T_{sw}+2T_{d}+T_{on}) &= T_{sw}\left(\left(\frac{v_{s}(T_{sw})-v_{s}(0)}{2}\right)+v_{s}(0)+\frac{R}{2}\left(i_{c}(T_{sw})+i_{c}(0)\right)+\frac{L}{T_{sw}}\left(i_{c}(T_{sw})-i_{c}(0)\right)\right)\\ 2T_{on} &= T_{sw}-2T_{d}+\frac{T_{sw}}{V_{c}}\left(\left(\frac{v_{s}(T_{sw})+v_{s}(0)}{2}\right)+\frac{R}{2}\left(i_{c}(T_{sw})+i_{c}(0)\right)+\frac{L}{T_{sw}}\left(i_{c}(T_{sw})-i_{c}(0)\right)\right)\\ T_{on} &= \frac{T_{sw}}{2}-T_{d}+\frac{T_{sw}}{2V_{c}}\left(\left(\frac{v_{s}(T_{sw})+v_{s}(0)}{2}\right)+\frac{R}{2}\left(i_{c}(T_{sw})+i_{c}(0)\right)+\frac{L}{T_{sw}}\left(i_{c}(T_{sw})-i_{c}(0)\right)\right)\\ T_{on} &= \frac{T_{sw}}{2}\left(1+\frac{1}{V_{c}}\left(\left(\frac{v_{s}(T_{sw})+v_{s}(0)}{2}\right)+\frac{R}{2}\left(i_{c}(T_{sw})+i_{c}(0)\right)+\frac{L}{T_{sw}}\left(i_{c}(T_{sw})-i_{c}(0)\right)\right)\right)-T_{d} \end{split}$$

Converting the above equation to discrete time domain,

$$T_{on} = \frac{T_{sw}}{2} \left(1 + \frac{1}{V_c} \left(\left(\frac{v_s(n) + v_s(n-1)}{2} \right) + \frac{R}{2} (i_c(n) + i_c(n-1)) + \frac{L}{T_{sw}} (i_c(n) - i_c(n-1)) \right) \right) - T_d$$
(10)

Equation (10) is used to model the PWM block.

III. MODELING

The single phase half bridge shunt APF model with a nonlinear load is shown in Fig. 9. The nonlinear load is a 200W full wave bridge rectifier with capacitor filter and a resistive load. The nonlinear load is driven by a 230 V, 50 Hz power supply. In order to capture the line current with APF not connected and connected, in a single simulation, a switch is placed between the AC power supply and the inductor. This switch is kept open for the first ten cycles of $v_s(t)$ and then it is closed. The line current with APF not connected is as shown in Fig. 10. FFT of this line current (Fig. 11) shows that, the THD is 50.54%. The line current with APF connected is as shown in Fig. 12. FFT of this line current (Fig. 13) shows that, the THD is 4.15%. The compensating current generated is as shown in Fig. 14. The values of model parameters are tabulated in table 2.



Figure 9. Single phase half bridge shunt APF model with a nonlinear load



Figure 10. Line current (APF OFF)



Figure 11. FFT of line current (APF OFF)



Figure 12. Line current (APF ON)



Figure 13. FFT of line current (APF ON)



Figure 14. Actual compensating current

Table 2. Model parameters

| Parameter | Value | |
|-----------|--------|--|
| T_{sw} | 80 µs | |
| T_d | 1 μs | |
| V_{c} | 650 V | |
| L | 130 mH | |
| R | 163 Ω | |

IV. SIMULATION RESULTS

The simulation results obtained for other nonlinear loads with this APF model is tabulated in table 3.

Table 3. Simulation results



V. CONCLUSION

Simulation results obtained for, single phase half bridge shunt APF model with fix load, show that the THD is reduced below 5% and pf is improved. Simulation results meet the IEEE 519-1992 recommendation. Therefore, the expression for ON time of MOSFET, in single phase half bridge shunt APF, is suitable to be implemented as an embedded system.

REFERENCES

- Sergio Serena, Chongming Qiao and Keyue M. Smedley, A Single Phase Active Power Filter with Double Edge Integration Control IECON'01: The 27th Annual Conference of the IEEE Industrial Electronics Society, 2001, pp. 949 - 953
- [2] R. B. Oliveria, F. B. Libano, R. A. M. Braga and J. C. Lima, Low Cost Single Phase Active Power Filter Controlled by DSP, 10th International Conference on Harmonics and Quality of Power, 2002, pp. 524-529.
- [3] Chongming Qiao, Keyue M. Smedley and Franco Maddaleno, A Single Phase Active Power Filter With One Cycle Control Under Unipolar Operation, *IEEE Transactions on Circuits and Systems*, 2004, pp. 1623-1630.

BIBLIOGRAPHY



Mr. V. R. Gaikwad born in Maharashtra, in India on December 29, 1977. He graduated from Dr. J. J. Magdum College of Engineering, Jaysingpur and post graduated from Walchand College of Engineering, Sangli. He received B.E and M.Tech. degree in Electronics Engineering from Shivaji University, Kolhapur. He is working as Assistant Professor in the department of electronics engineering at walchand college of engineering, sangli. His fields of interest include circuits and systems, embedded systems and VLSI.



Mr. S. N. Kore born in India on May 10, 1959, is M.E. in Electronics Engineering. He is working as Associate Professor at Walchand College of Engineering, since 1990, in the department of electronics engineering. His areas of interest are digital signal processing and communication networks. He is a member of the board of studies in electronics at shivaji university, kolhapur and solapur university, solapur. He is recipient of Annasaheb Benare's Charitable Trust's Best Teacher award, in 2005.