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Design and Optimum Arrangement Of 3-phase Cascade Multilevel Inverter for Control of DTC Induction Motor

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Abstract : *In present days the Multi level inverter increasing popularly especial in high power and high voltage applications. The Multi level inverter having new set of features. When the level is increasing and output become nearly sinusoidal. When the sinusoidal means the output voltage having less losses the more levels of output voltage produces different methods is there the cascade H bridge is the most efficient method .In my project cascade H bridge used to producing more levels of output voltages in cascade H bridge. In this cascade H bridge two types of arrangement they are symmetrical and asymmetrical .In this cascade H bridge I find out experimentally that the asymmetrical Multi level inverter is most efficient method than the symmetrical method by using DTC technique. The DTC technique provides ripple losses and friction losses reduce. So the induction motor having the most efficient .Here we are using IGBT switching and for the controlling purpose uses the state vector modulation.*

The cascade out experiment show that an asymmetrical configuration provides nearly sinusoidal voltages with low distortion using less switching devices moreover torque ripples are reduced.

Keywords: *State Vector Modulation (SVM),Direct Torque Control(DTC),Induction Motor(IM),Multi Level Inveter (MLI)*

I. Introduction

Multilevel voltage-source inverters are intensively studied for high-power applications and standard drives for medium-voltage industrial applications have become available Solutions with a higher number of output voltage levels have the capability to synthesize waveforms with a better harmonic spectrum and to limit the motor winding insulation stress. However, their increasing number of devices tends to reduce the power converter overall reliability and efficiency. On the other hand, solutions with a low number of levels either need a rather large and expensive LC output filter to limit the motor winding insulation stress, or can only be used with motors that do withstand such stress. The various voltage stages have been chosen after considering the real-power contribution of the highest voltage stage. The maximum power supplied by highest voltage stage is maintained below the load power.

One of the methods that have been used by a major multilevel inverter manufacturer is direct torque control (DTC), which is recognized today as a high-performance control strategy for ac drives. Several authors have addressed the problem of improving the behaviour of DTC ac motors, especially by reducing the torque ripple. Different approaches have been proposed. Although these approaches are well suitable for the classical two-levels inverter, their extension to a greater number of levels is not easy. Throughout this paper, a theoretical background is used to design a strategy compatible with hybrid cascaded H-bridge multilevel inverter; symmetrical and asymmetrical configuration are implemented and compared. Experimental results obtained for an asymmetrical inverter-fed induction motor confirm the high dynamic performance of the used method, presenting good performances and very low torque ripples. Multilevel power conversion has been receiving increased attention recently, especially for high-power, high-voltage applications. To date, many inverter topologies have been reported in the literature with particular interest focused on cascaded topology. The conventional cascaded topology has many inherent benefits with one particular advantage being its modular structure, which enables higher-level inverters to be easily implemented through the series connection of identical H-bridges. This flexibility has resulted in its applications in medium-voltage industrial drives , electric vehicles and the grid connection of photovoltaic-cell generation systems. A modified form of cascaded inverter is the hybrid (binary,quasilinear or tri-nary) inverter . The hybrid inverter is basically a cascaded inverter in which each of the cascaded H-bridges utilises different power devices and is supplied from an isolated DC source of a different potential.The design intention of the hybrid inverter is to attain an optimal trade-off in the selection of power devices in terms of switching frequency and voltage-sustaining capability, since the trends in power semiconductor technology are that the voltage-blocking capability of fast-switching devices (e.g. insulated-gate bipolar transistors) and the switching speed of high-voltage thyristor-based devices (e.g. integrated- gate commutated thyristors) are limited. An optimized hybrid inverter is therefore more efficient as it can generate the same number of output voltage levels using fewer power devices and DC sources as compared with conventional cascaded inverter.

II. Cascade H Bridge Operation

A single-phase structure of an m-level cascaded inverter is illustrated in. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$$

The cascaded H-bridge inverter consists of power conversion cells, each supplied by an isolated dc source on the dc side, which can be obtained from batteries, fuel cells, or ultra capacitors and series-connected on the ac side. The advantage of this topology is that the modulation, control, and protection requirements of each bridge are modular. It should be pointed out that, unlike the diode-clamped and flying-capacitor topologies, isolated dc sources are required for each cell in each phase.

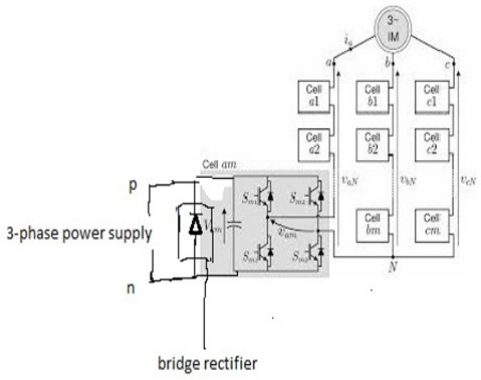

Figure :- 3-phase three cells cascade H bridge

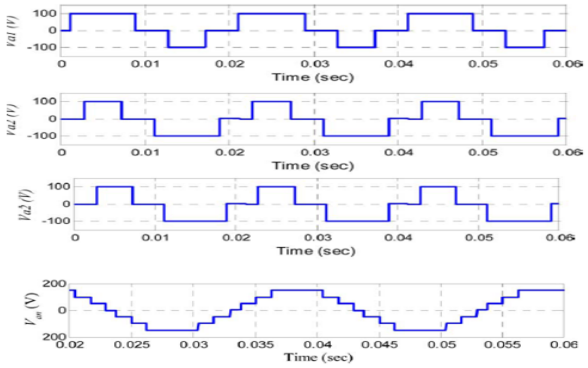

Figure : Symmetric multilevel inverter with seven-levels output voltage synthesis.

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TABLE I
COMPARISON OF MULTILEVEL INVERTERS

	Symmetrical inverter	Asymmetrical inverter	
		Binary	Ternary
N	$2N+1$	$2^{N+1}-1$	3^N
DC sources number	N	N	N
Switches number	$4N$	$4N$	$4N$
$V_{o,MAX}$ [pu]	N	2^N-1	$(3^N-1)/2$

$$V_{o,\mathrm{MAX}} = \sum_{j=1}^{N} V_{\mathrm{dc},j}.$$

$$\begin{cases} V_{o,\mathrm{MAX}} = \left(2^N - 1\right) V_{\mathrm{dc}}, \\ \quad \text{if } V_{\mathrm{dc},j} = 2^{j-1} V_{\mathrm{dc}}, \qquad j = 1, 2, \ldots, N \\ V_{o,\mathrm{MAX}} = \left(\dfrac{3^N - 1}{2}\right) V_{\mathrm{dc}}, \\ \quad \text{if } V_{\mathrm{dc},j} = 3^{j-1} V_{\mathrm{dc}}, \qquad j = 1, 2, \ldots, N. \end{cases}$$

The cascaded H-bridge inverter consists of power conversion cells, each supplied by an isolated dc source on the dc side, which can be obtained from batteries, fuel cells, or ultracapacitors and series-connected on the ac side. The advantage of this topology I that the modulation, control, and protection requirements of each bridge are modular.

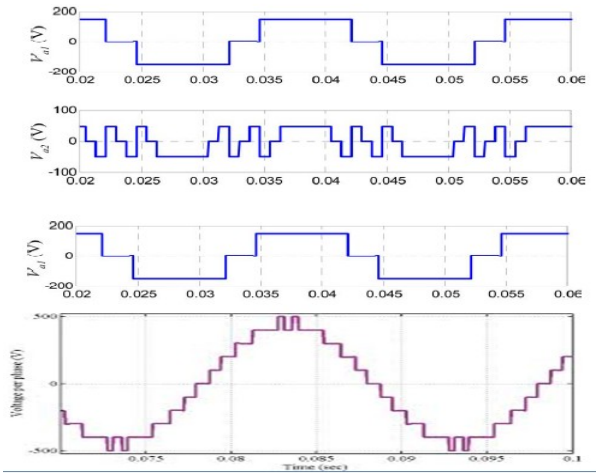


Figure:- Asymmetric multilevel inverter with eleven-levels output voltage synthesis.

It should be pointed out that, unlike the diode-clamped and flying-capacitor topologies, isolated dc sources are required for each cell in each phase. Fig. 1 shows a three-phase topology of a cascade inverter with isolated dc-voltage sources. An output phase-voltage waveform is obtained by summing the bridges output voltages

$vo\ (t) = vo,1\ (t) + vo,2\ (t) + \cdots + vo,N\ (t)$ (1)

where N is the number of cascaded bridges. The inverter output voltage $vo\ (t)$ may be determined from the individual cells switching states

$vo\ (t) = \_N j{=}1(\mu j - 1)\ V\mathrm{dc},j,\ \mu j = 0,\ 1, \ldots .$ (2)

If all dc voltage sources in are equal to Vdc, the inverter is then known as a symmetric multilevel one. The effective number of output voltage levels n in symmetric multilevel inverter is related to the cells number by

$n = 1{+}2\ N$ (3)

For example, Fig. 2 illustrated typical waveforms of Fig. 1

multilevel inverter with two dc sources (five-levels output). The maximum output voltage Vo,Max is then

Vo,MAX = NVdc. (4)

To provide a large number of output levels without increasing the number of inverters, asymmetric multilevel inverters can be used.

In it is proposed to chose the dc-voltages sources according to a geometric progression with a factor of 2 or 3. For N of such cascade inverters, one can achieve the The insulated-gate bipolar transistor or IGBT is a three-terminal power semiconductor device, noted for high efficiency and fast switching. It switches electric power in many modern appliances: electric cars, variable speed refrigerators, air-conditioners, and even stereo systems with digital amplifiers. Since it is designed to rapidly turn on and off, amplifiers that use it often synthesize complex waveforms with pulse width modulation and low-pass filters. The IGBT combines the simple gate-drive characteristics of the MOSFETs with the high-current and low–saturation-voltage capability of bipolar transistors by combining an isolated-gate FET for the control input, and a bipolar power transistor as a switch, in a single device. The IGBT is used in medium- to high-power applications such as switched-mode power supply, traction motor control and induction heating. Large IGBT modules typically consist of many

devices in parallel and can have very high current handling capabilities in the order of hundreds of amps with blocking voltages of 6,000 V. The IGBT is a fairly recent invention. The first-generation devices of the 1980s and early 1990s were relatively slow in switching, and prone to failure through such modes as latch up and secondary breakdown.

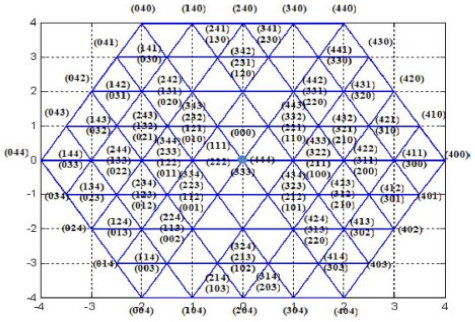
III. Direct Torque Control Of Multilevel Inverterfed Induction Machine:-

Direct Torque Control with Multilevel Inverter (DTC-MLI) has emerged recently in high dynamics AC drives fields for induction machines or permanent magnet machines application. In this paper, a review on a variety of techniques and concepts of direct torque control of multilevel inverter-fed induction machines is presented. The techniques and concept involved are classified as follows: Look-up table hysteresis based DTC-MLI, DTC-MLI with space vector modulation, predictive control strategy of DTC-MLI, hybrid modulation and hybrid inverter strategy of DTC-MLI and DTC-MLI with fuzzy logic controller. From this review, the properties of the discussed controller techniques together with advantages and disadvantages are presented.

Induction Machines (IMs) have been widely used in the industry due to the fact that it is maintenance free, simple in terms of construction, reliable and rugged. In contrast to the commutation DC motors,induction machines can be used in an explosive, corrosive or any harsh environment. This is because the latter has no problem with spark and corrosion which is due to the commutator and the brushes as in the former. Despite these advantages IM however, suffers from control problems when used in high performance Adjustable Speed Drive (ASD) applications. Based on the commonly adopted space phasor dynamics model equations related to the dynamics model

When a multilevel inverter is used in the DTC configuration to feed the IM, the number of available voltage space vectors is increased proportionally to the voltage levels of the inverter. having this extra flexibility in selecting the optimum voltage vector, a more precise control both torque and flux can be obtained.

To feed a three-phase IM, a three-phase multilevel inverter is required. The three-phase multilevel inverter is composed of three multilevel inverter legs.There are three prominent multilevel inverter topologies: Diode-clamped multilevel



. 5. Voltage vectors of various states of the symmetrical five-levels inverter.

Torque and Flux Estimation:

The stator flux vector an induction motor is related to the stator voltage and current vectors by

$$\frac{d\phi_s\,(t)}{dt} = v_s\,(t) - R_s i_s\,(t)$$

Maintaining vs constant over a sample time interval and neglecting the stator resistance, the integration of (10) yields

$$\Delta\phi_s\,(t) = \phi_s\,(t) - \phi_s\,(t-\Delta t) = \int_{t-\Delta t}^{t} v_s \Delta t.$$

Above Equation reveals that the stator flux vector is directly affected by variations on the stator voltage vector. On the contrary, the influence of vs over the rotor flux is filtered by the rotor and stator leakage inductance, and is, therefore, not relevant over a short-time horizon. Since the stator flux can be changed quickly while the rotor flux rotates slower, the angle between both vectors θsr can be controlled directly by vs .

A graphical representation of the stator and rotor flux dynamic behavior is illustrated in Fig. The exact relationship between stator and rotor flux shows that keeping the amplitude of *φs constant will* produce a constant flux *φr*

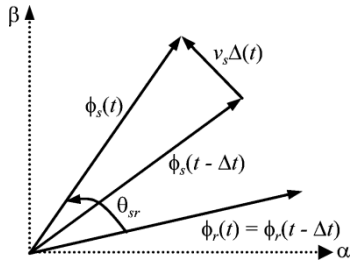


Fig. Influence of *vs over φs during a simple interval Δt.*

Voltage Vector Selection:

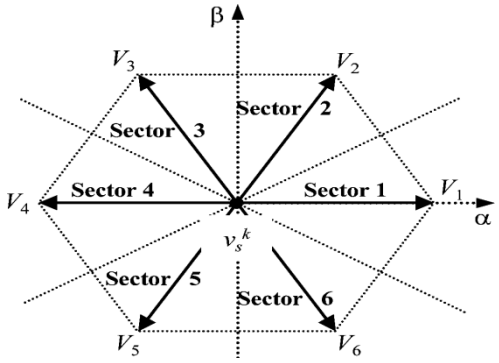


Fig. Possible voltage changes Δ*vks that can be applied from certain vks*

Above Fig.illustrates one of the 127 voltage vectors generated by the inverter at instant t=k, denoted by vks (central dot). The next voltage vector, to be applied to the load v(k+1)s , can be expressed by

v(k+1)s = vks +Δvks

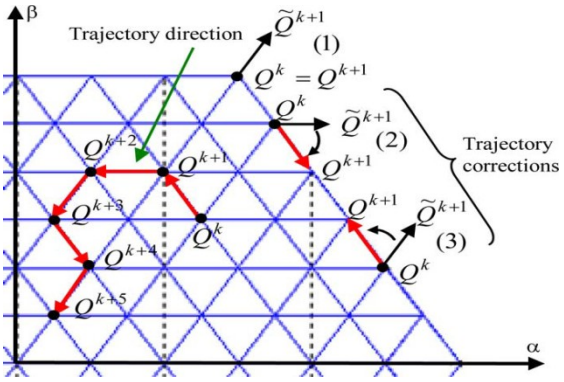
where Δvks = {vi |i = 1, . . . , 6}. Each vector vi corresponds to one corner of the elemental hexagon illustrated in gray and by the dashed line in above Fig. The task is to determine which v(k+1)s will correct the torque and flux responses, knowing the actual voltage vector vks , the torque and flux errors ekφ and ekT , and the stator flux vector position (sector determined by angle θs). Note that the next voltage vector v(k+1)s applied to the load will always be one of the six closest vectors to the previous vks ; this will soften the actuation effort and reduce high dynamics in torque response due to possible large changes in the reference.

Table II summarizes vector selections for the different sectors and comparators output (desired φs and Te corrections). To implement the DTC of the induction motor fed by a hybrid H-bridge multilevel inverter, one should determine at each sampling period, the inverter switch logic states as a function of the torque and flux instantaneous values for the selection of the space vector in the α–β frame. The proposed control algorithm was divided into two major tasks, which are independent and executed in cascade.

Table II Voltage-Vector-Selection Lookup Table

Sector	sign(e_ϕ^k,e_T^k)			
	(+,+)	(+,–)	(–,+)	(–,–)
1	V_2	V_6	V_3	V_5
2	V_3	V_1	V_4	V_6
3	V_4	V_2	V_5	V_1
4	V_5	V_3	V_6	V_2
5	V_6	V_4	V_1	V_3
6	V_1	V_5	V_2	V_4

1) First task: It aims at the control of the electromagnetic state of the induction motor. The torque and flux instantaneous values, and their variations will be taken into account for the space vector selection in the α–β. Once the space is chosen, the phase levels sequence can be selected. To ensure this task, one should detect the space vector position in the α–β frame (Qk at sampling time k). The algorithm must then select the next position Q(k+1) to be achieved before next sampling instant k + 1 (see Fig. 8) in order to reduce voltage steps magnitude. Only one step displacement



In the α–β frame is authorized per sampling period Ts . Hence, in the absence of inverter saturation, Qk+1 must coincide with one of the six corners of the elementary hexagon centered at Qk . The same procedure will be carried out at the next period in order to determine the next trajectory direction, yielding Qk+2, which in turn will coincide with one of the six corners of the new elementary hexagon centered at Qk+1. In case of inverter saturation (if Qk gives an unreachable point for Q(k+1), a trajectory correction is necessary (see Fig. 8).

In cases (2) and (3), the closest displacement direction is selected. Case (1) illustrates a particular situation in which no switching should be performed, since the nearest reachable trajectory goesroughly toward the opposite sense of the favored one given by the lookup table (see Table II).

2) Second task:

It exploits the degree of freedom related to the multilevel topology to choose the phase levels sequence that synthesizes the voltage vector selected previously. There are several phase levels sequences that are able to generate the same vector illustrated in Fig. 9; this degree of freedom can, therefore, be exploited to reduce voltage steps magnitude according to one of the following criteria: a) minimize the commutation number per period; b) distribute commutations for the three-phases per period; or c) choose a vector which minimizes the homopolar voltage. This task allows losses and torque ripple minimization

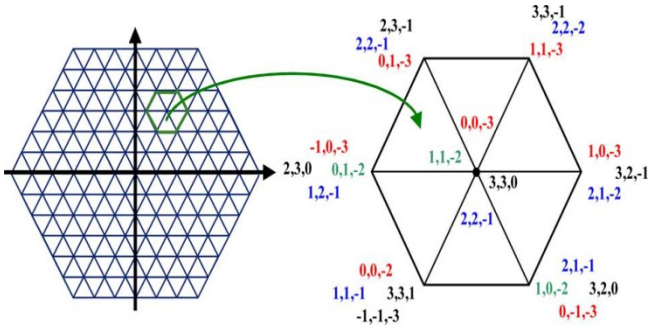


Fig. Space vector and sequences of a seven-levels cascaded H-bridge inverter.

`Simulation circuites designs

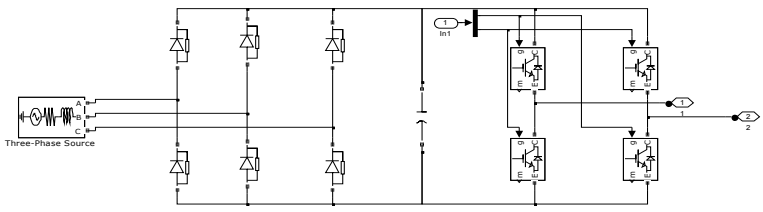


Fig:- 3-phase power supply bridge circuite

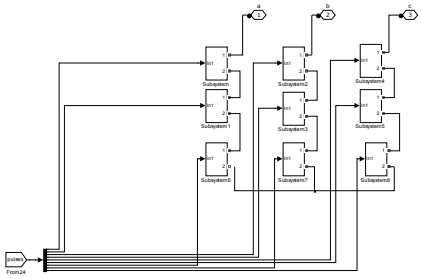
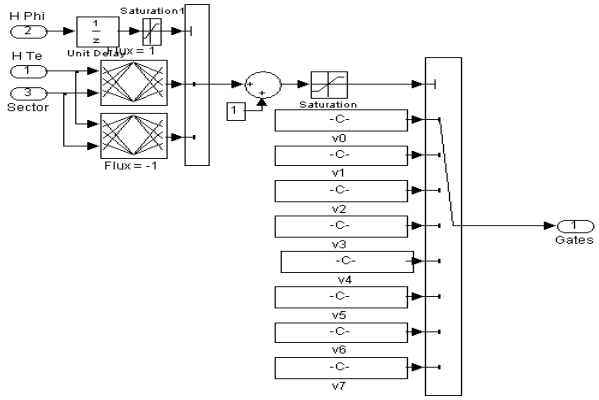


Fig:-3-phase 3-cell bridge circuites



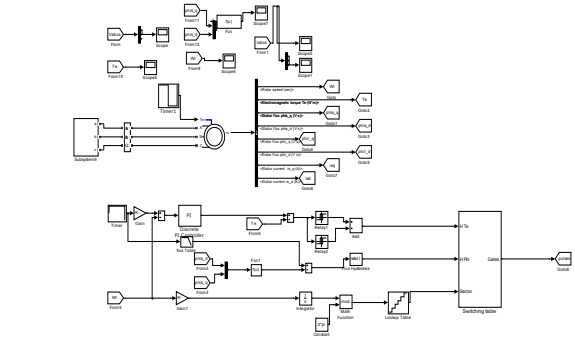


Fig:- Block diagram Project outputs

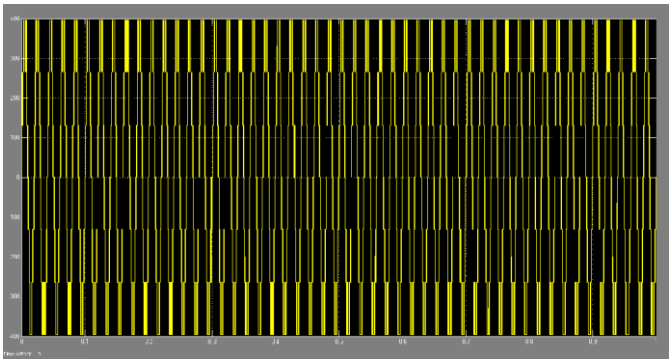


Fig seven level cascade H Bridge symmetrical output waveform

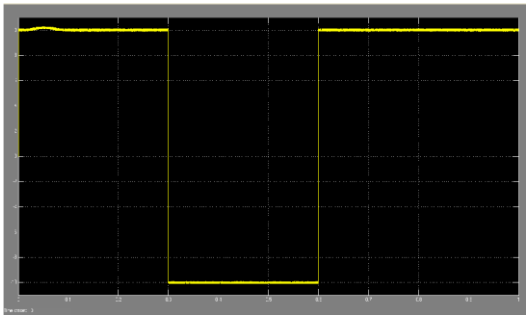


Fig eleven level cascade h bridge inverter torque waveform

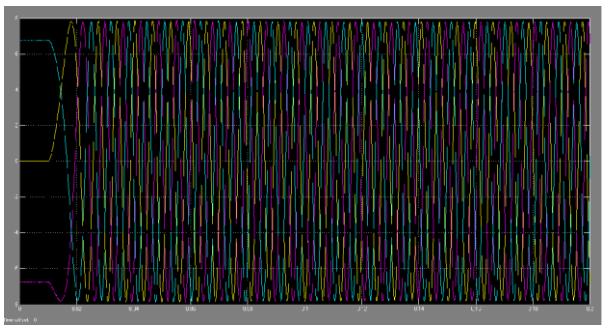


Figure 1eleven level cascade h bridge inverter current waveform

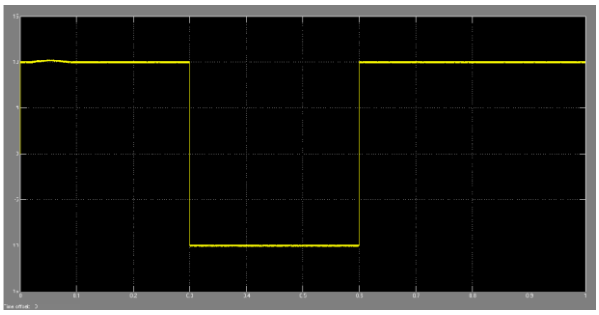


Fig seven level cascade h bridge inverter current waveform

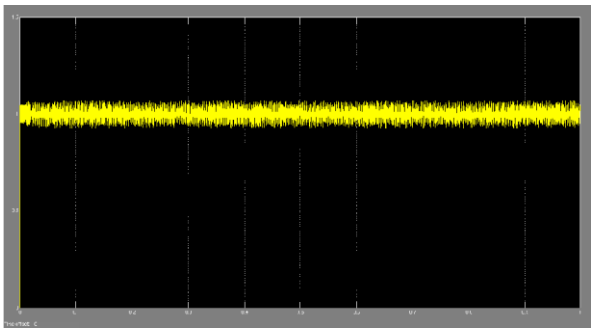


Fig Seven level cascade h bridge inverter stator flux wave form

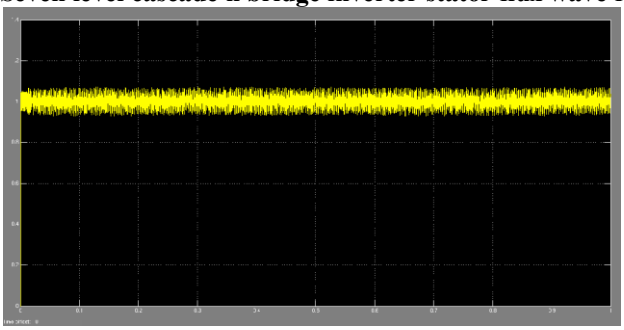


Fig eleven level cascade h bridge inverter stator flux wave form

IV. Conclusion

The paper dealt with a optimum arrangement for a cascade H bridge multi level inverter DTC Induction motor. indeed symmetrical and asymmetrical arrangement of seven and eleven levels H bridge inverters have been optimum arrangement in order to find with lower switching losses and optimized output voltage quality the carried out experiments shows that an asymmetrical configuration provides nearly sinusoidal voltages ith very low distortion using less switching devices. in addition torque ripples are greatly reduced asymmetrical multi level inverter enables a DTC solution for high power induction motor drives not only due to the higher voltage capability provided by multilevel inverter but mainly due to the reduced switching losses and improved output voltage quality which provides sinusoidal current without filter

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