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Modified three phase Unified Power Quality Conditioner with capacitor midpoint topology

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Abstract*—Two different topologies of three phase Unified Power Quality Conditioner (UPQC) namely 3P3W/ 3P4W UPQC are analyzed. For better performance of UPQC, DC link voltage have to be maintained. If it is energized through solar photovoltaics, a modified UPQC structure employing capacitor midpoint (dual capacitor) is employed to accommodate its dc voltage variation. Simulations are carried out for the above topologies with single and dual capacitor (dc sources) and 3P4W UPQC with dual capacitor at its mid point is found to produce better results.*

Index Terms*—Active Power Filter (APF), four-leg voltage-source inverter (VSI) , three-phase four-wire system, unified power quality conditioner, Capacitor Mid point (CMP) .*

I. Introduction

The use of sophisticated equipment/loads at distribution level has increased considerably in recent years due to the development in the semiconductor device technology. The equipment needs clean power in order to function properly. At the same time, the switching operation of these devices generates current harmonics resulting in a polluted distribution system. The power-electronics based devices have been used to overcome the major power quality problems. To provide a balanced, distortion-free and constant magnitude power to sensitive load and at the same time, to restrict the harmonic unbalance and reactive power demanded by the load and to make the overall power distribution system more healthy, the unified power quality conditioner(UPQC) is one of the best solutions. UPQC consists of two Active Power Filters (APF) connected back-to-back on the dc side which deals with both load current and supply voltage imperfections.

II. Operation of 3p3w Upqc

Fig. 1 gives the circuit of 3P3W UPQC. The shunt component is responsible for mitigating the power quality (PQ) problems caused by the consumer: poor power factor, load harmonic currents, load unbalance, DC offset, etc. The shunt active filter is responsible for power factor correction, compensation of load current harmonics and unbalances. It maintains constant average voltage across the dc storage capacitor C_{dc}. The shunt part of UPQC consists of a VSI connected to the common dc storage capacitor C_{dc} on the dc side and on the ac side it is connected in parallel with the load through the shunt interface inductors L_{SH} and a star-connected three-phase shunt coupling auto-transformer T_{SH}. The shunt interface inductors L_{SH} together with the shunt filter capacitors C_{SH} are used to filter out the switching frequency harmonics produced by the shunt VSI. T_{SH} is used for matching the network and VSI voltages.

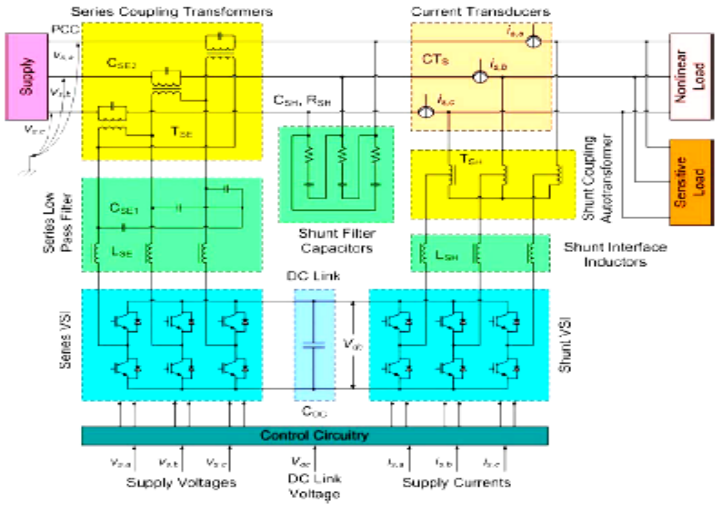

Fig.1. Power circuit of 3P3W UPQ

The series component of UPQC is responsible for mitigation of supply side disturbances: voltage sags/swells, flicker, voltage unbalance and harmonics. It inserts voltages so as to maintain the load voltages at a desired level balanced and distortion free. And also series active filter is responsible for voltage compensation during supply side disturbances.

The series part of the UPQC also consists of a VSI connected on the dc side to the same energy storage capacitor C_{dc} and on the ac side, it is connected in series with the feeder through the series low-pass filter (LPF) and three individual single-phase series coupling transformers T_{SE}.

II. 3p4w Distribution System Utilizing Upqc

A 3P4W distribution system is realized by providing a neutral conductor along with three power conductors from generation station or by utilizing a three-phase Δ–Y transformer at distribution level. Fig. 3 shows a 3P4W network in which the neutral conductor is provided from the generating station itself. Assume a plant site where three-phase three-wire UPQC is already installed to protect a highly sensitive load and to restrict any entry of distortion from load side toward utility. If we want to upgrade the system now from 3P3W shown in

Fig.2 to 3P4W shown in Fig.3 due to installation of some single-phase loads and if the distribution transformer is close to the plant under consideration, utility would provide the neutral conductor from this transformer without major cost involvement. In certain cases, this may be a costly solution because the distribution transformer may not be situated in close vicinity.

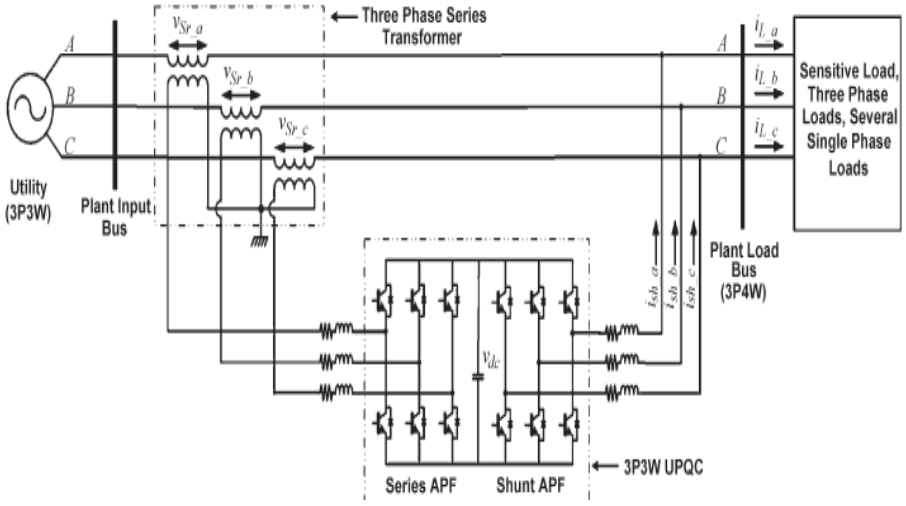

Fig.2. 3P3W UPQC structure

The 3P4W UPQC topology can be realized from 3P3W system, which has all the advantages of the latter including the easy expansion of 3P3W system to 3P4W system.

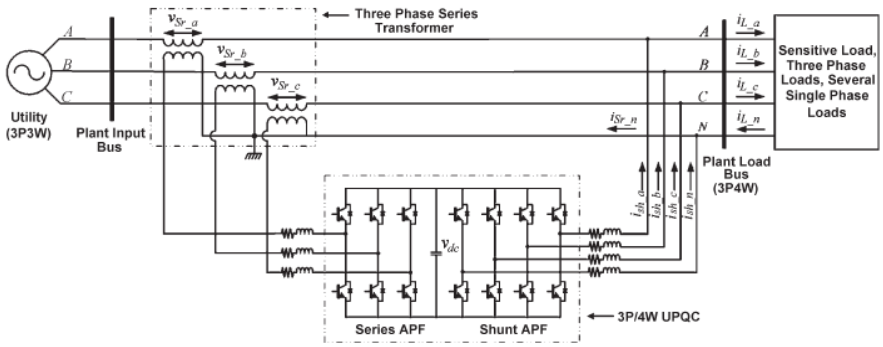

Fig.3 3P4W UPQC Structure

The four-leg VSI topology requires one additional leg as compared to the split capacitor topology. The neutral current compensation in four-leg VSI structure is much easier than that of split capacitor because split capacitor topology essentially needs two capacitors and an extra control loop to maintain a zero voltage error

difference between both the capacitor voltages, resulting in a more complex control loop to maintain the dc bus voltage at constant level. In this paper, four-leg VSI topology is considered to compensate the neutral current flowing towards the transformer neutral point. A fourth leg is added to the existing 3P3W UPQC, such that the transformer neutral point will be at virtual zero potential. Thus, the proposed structure would help to realize a 3P4W system from a 3P3W system at distribution load end. This would eventually result in easy expansion from 3P3W to 3P4W systems.

IV. Upqc Controller

A control strategy is proposed to compensate the current unbalance present in the load currents by expanding the concept of single phase *p–q* theory. According to this theory, a single phase system can be defined as a pseudo two-phase system by giving $\pi/2$ lead or $\pi/2$ lag, i.e., each phase voltage and current of the original three-phase system can be considered as three independent two-phase systems. Here, $\pi/2$ lead is considered to achieve a two-phase system for each phase. The major disadvantage of *p–q theory* is that it gives poor results under distorted and/or unbalanced input/utility voltages. In order to eliminate these limitations, the reference load voltage signals extracted for series APF are used instead of actual load voltages.

A. Control of Shunt Active Power Filter

The shunt active power filter is controlled as a current controlled VSI. When the UPQC supplies a nonlinear/inductive load, objective of the shunt converter is to compensate for the load current harmonics, reactive power and unbalance, such that the supply currents are balanced sinusoids (i.e., the distortion is within the limits prescribed by standards) in-phase with the voltages at the point of common coupling (PCC). The shunt APF current is controlled indirectly by controlling the source current to be sinusoidal and in-phase with the fundamental positive sequence component of the source voltage. Thus, the system tracks source current instead of tracking the shunt APF current. Combined with a hysteresis current controller, this control technique involves only the source current measurement. The simulation is started with 50-Hz as source frequency. For this purpose, supply voltage is measured and passed through a scaling and filter circuit to eliminate the high frequency noise. The zero crossing of the "A" phase source voltage at negative to positive half-cycle transition is detected

with a simple threshold comparison method. A noisy zero crossing is a potential threat for this method of synchronization. To avoid detection of multiple zero crossing, any successive zero crossing detected is discarded for next 30

Samples after the first one is detected. The number of samples for one power cycle is counted. This is compared with a fixed

number of samples every time the zero crossing is detected. If the grid frequency is higher than 50 Hz, a positive difference is calculated..

B. Control of the Series Active Power Filter

The series active power filter is controlled as a voltage controlled VSI. It maintains the load voltage at a predetermined level during source voltage abnormal conditions, such as voltage sag and unbalance. A sequence analysis-based compensation strategy has been developed to compensate balanced and/or unbalanced incoming voltage to regulate the load voltage. The advantage of the scheme is that under most of the practical cases of unbalance, the series APF controller is able to fully compensate the unbalance, provided the voltage rating of the series APF is higher than the negative sequence voltage magnitude. A feed-forward control loop measures the source voltage continuously and it is compared with the reference voltage to be maintained at the load. The voltage to be injected is calculated and the appropriate switching signals are sent to the insulated gate bipolar transistor switches.

V. Capacitor Mid Point Topology

In place of three single-phase converters, a four-leg approach is proposed. The four-wire converter can take either of the two forms shown in Fig.4. The first approach utilizes a standard three-phase converter (Fig.4) where the dc-side capacitor is split and the midpoint of the capacitor connection provides the return path for the neutral wire currents. An alternative approach is to use a fourth switching pole as shown in Fig.5. Here, three of the switch poles are connected to the three phase conductors through a series inductance (also used for filtering) while the fourth switch pole is connected (through an optional inductor) to the neutral conductor.

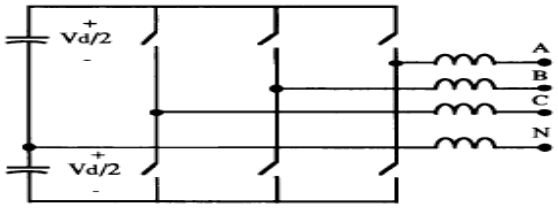

Fig.4 Capacitor-Midpoint Topology

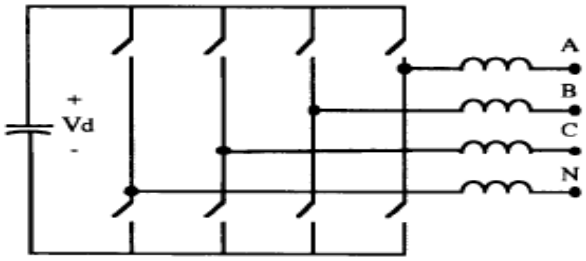

Fig.5 Four Switch-Pole Topology

In the case of the filter with the fourth switch pole, the current reference is simply the negative sum of the three phase current references. In such a scheme the switching frequency varies continuously and takes high frequency filtering difficult. To charge and maintain adequate charge on the dc-side capacitor, a PI regulator will be used to control the flow of real power from the ac-side towards the dc-side of the converter. Since the converter is designed only to compensate for harmonics, which don't include the fundamental, this real power transfer merely compensates for the losses in the various filter components, switches and interconnections.

VI. Simulation Results

Simulations are carried for the 3P4W UPQC topology along with 3P3W UPQC. The UPQC should maintain the voltage at

Load bus at a desired value and free from distortion. The plant load is assumed to be a three phase RLC load with unbalance. The shunt APF is turned ON first at time t = 0.1s such that it maintains the dc-link voltage at a set reference value. At time t = 0.2 s, the series APF is put into operation. The series APF injects the required compensating voltages through

Series transformer, making the load voltage free from distortion. Since the load on the network is unbalanced in nature, the neutral current may flow through neutral conductor

toward the series transformer neutral point. The shunt APF effectively compensates the current flowing towards the transformer neutral point. Thus, the series transformer neutral point is maintained at virtual zero potential. MATLAB/SIMULINK model of 3P3W & 3P4W UPQC with proposed topology having same/different valued capacitors incorporating the concept of solar PV dc link energization and its respective waveforms are shown from fig. 6 to 15. Table .1 compares the Total Harmonic Distortion w.r.t to various topologies of UPQC.

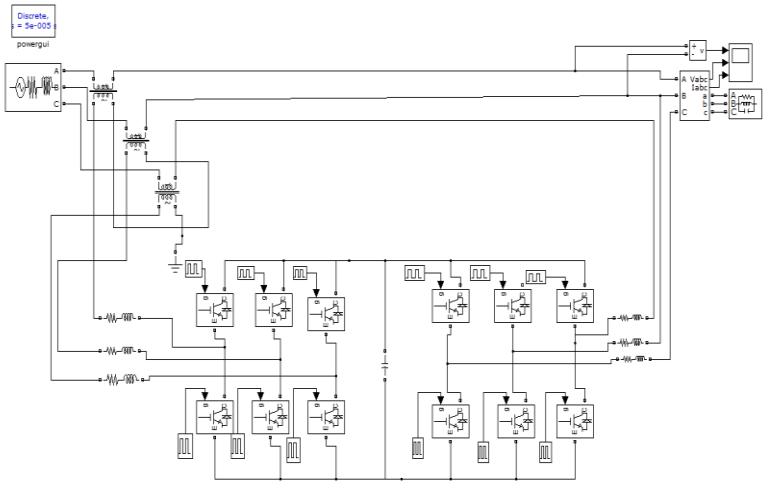

Fig.6. 3P3W UPQC simulation model

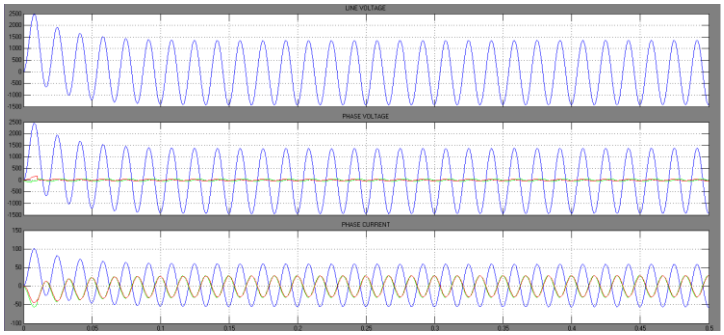

Fig.7 Output waveform of 3P3W UPQC

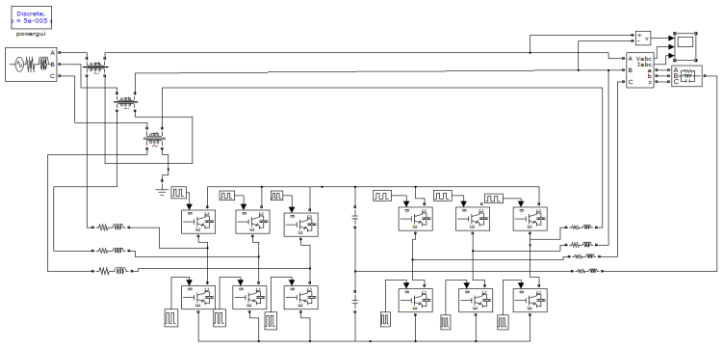

Fig.8 3P3W UPQC with Capacitor Midpoint Topology

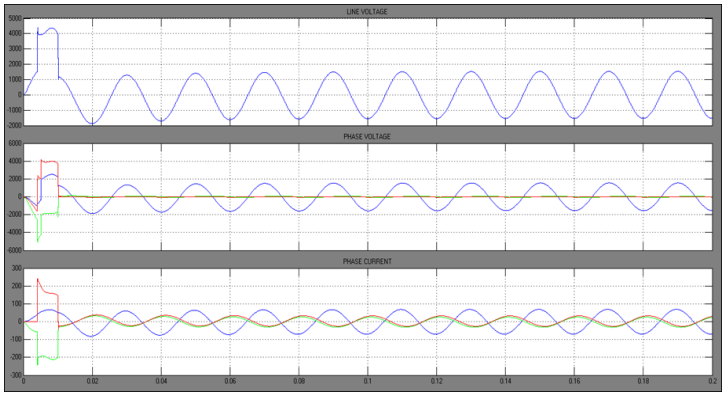

Fig.9 Simulation of fig.8 with same value of capacitors

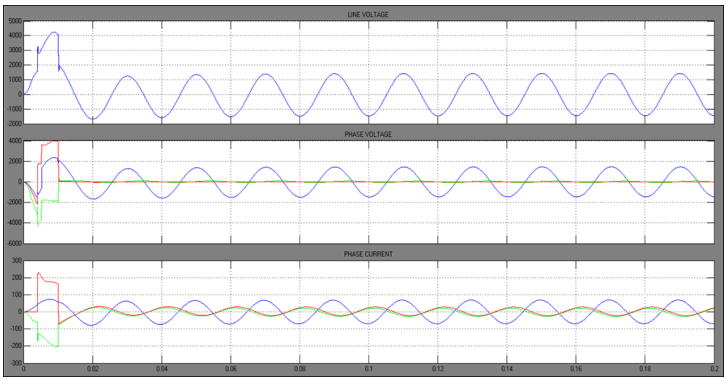

Fig.10. Simulation of fig.8 with different value of capacitors

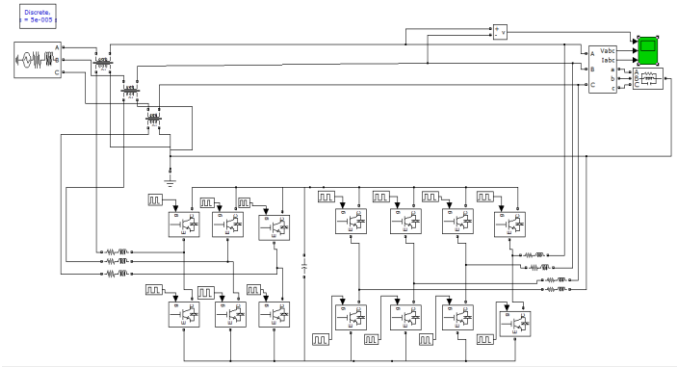

Fig.11 3P4W UPQC simulation model

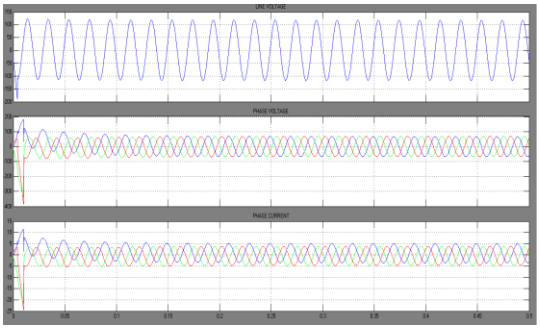

Fig.12. Simulation result for 3P4W UPQC

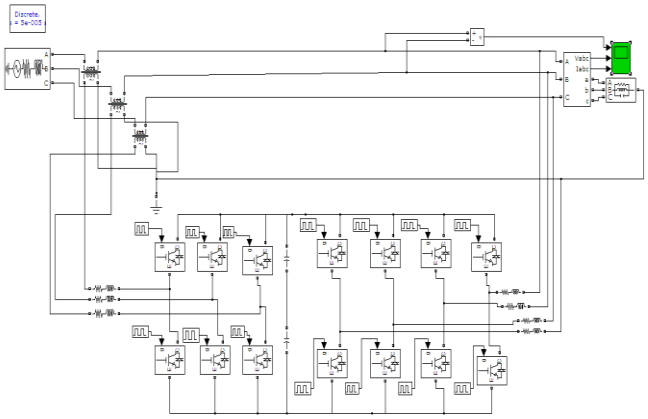

Fig.13.3P4W UPQC with Capacitor mid- Point Topology

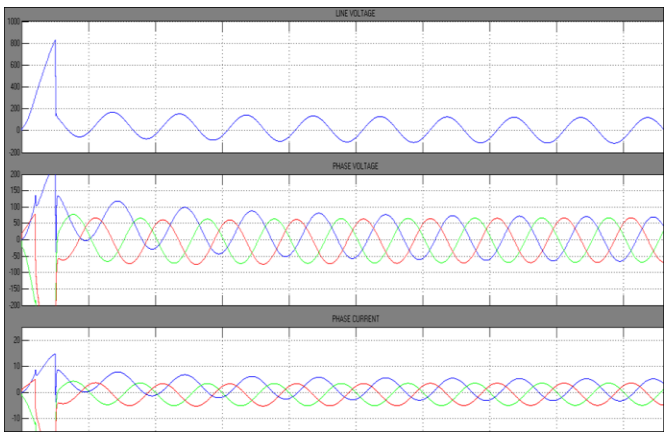

Fig.14 Simulation of fig. 11 with same value of capacitors

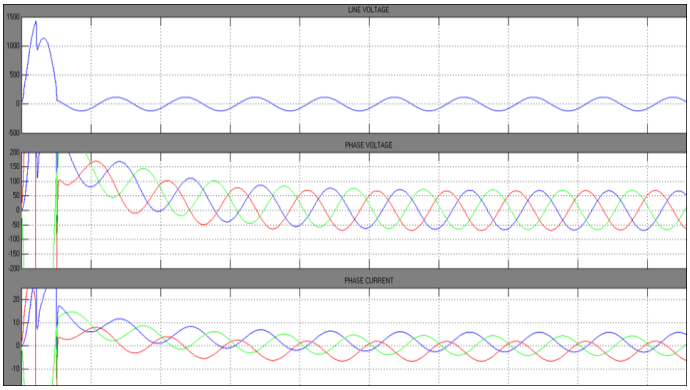

Fig.15 Simulation of fig.11 with different value capacitors

Table:1 Total Harmonic Distortion analysis of various topologies of UPQC

		3P3W UPQC	3P3W UPQC WITH CMP	3P3W UPQC with CMP (Different values)	3P4W UPQC	3P4W UPQC WITH CMP	3P3W UPQC with CMP (Different values)
THD (%)	Va	49.01	42.75	48.83	81.46	82.33	91.36
	Vb	56.41	56.51	57.66	69.91	68.66	67.83
	Vc	99.43	94.88	100.36	78.78	83.83	82.33
	Ia	10.03	12.37	11.321	83.83	64.04	93.60
	Ib	50.22	44.94	36.29	70.20	69.42	68.32
	Ic	119.81	112.66	107.55	80.57	85.58	84.79

VII. Conclusions

DC link voltage have to be maintained to ensure the better performance of UPQC. If it is energized through solar, a modified topology is proposed to accommodate its dc voltage variation by using a capacitor midpoint at the dc link. Simulations are carried out for the 3P3W/3P4W UPQC topologies and 3P4W UPQC with capacitor midpoint is found to produce better results.

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