Simulation of SPWM based Z-Source Inverter

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Abstract : *This paper presents a single stage Z-source inverter (ZSI) that can either buck or boost the ac output voltage from a DC supply. This topology overcomes the short comings of the where the output ac voltage is either less or more than the input dc voltage. The ZSI also allows two switches of the same leg to be gated in the circuit thus eliminating the shoot through fault that normally occurs in the traditional converters. This feature of the inverter provides the elimination of dead time in the circuit, thus increasing the reliability and reducing the output distortion. To prove the effectiveness of ZSI in reducing THD, performance of ZSI is evaluated using MATLAB/SIMULINK model developed for ZSI feeding R, RL, Motor load. The simulation results are presented for various modulation indexes and compared with the simulation results of VSI and CSI. The results validate the effectiveness of ZSI over VSI and ZSI.*

Keywords -*Current source inverter, voltage source inverter, Z-source inverter, SPWM, THD.*

I. INTRODUCTION

An inverter is a class of power conversion circuits that operates from a dc voltage source or a dc current source and converts it into ac voltage or current. Depending upon the sources inverters are classified into three namely, current source inverter, voltage source inverter and impedance source inverter [1-2]. To overcome the conceptual and theoretical barriers and limitation of the traditional voltage source inverter and current source inverter an impedance source power converter is developed. Z-source inverter is an impedance network which links the converter main circuit to the load or other converter, it is for providing special feature is not available in the traditional voltage source and current source inverter in which capacitor or inductor is used [3]. The main exposure of the Z- source inverter is that it can overcome the limitation of the traditional converters. A Z-source converter can provide unique features that cannot be obtained in traditional voltage–source and current–source converters. Recently, the research on Z-source has mainly focused on the three-phase Z-source inverter in which the Z-source network is used as the front stage [4]–[6]. The battery is paralleled with the Z-source capacitor in the three-phase Z-source inverter proposed in [7-9], and the Z-source network also performs the voltage boost ability as the front stage.

In this paper, a single-phase Z-source inverter topology is presented based on the unique feature of the Z-source. The feasibility of the proposed topology sinusoidal pulse width modulation strategy is analyzed in detail and verified by simulation and the results are compared with current source and voltage source inverters.

II. SINGLE PHASE VOLTAGE SOURCE INVERTER

Fig.1 shows such circuit where a single dc supply has been split in two halves. In such circuits the voltages across the two capacitors may not remain exactly balanced due to mismatch in the loading patterns or mismatch in leakage currents of the individual capacitors. Also, unless the capacitors are of very large magnitude, there may be significant ripple in the capacitor voltages, especially at low switching frequencies.
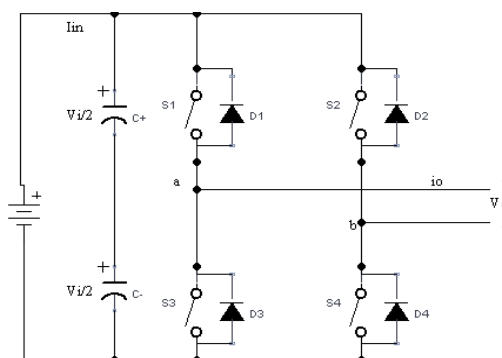

Fig.1 Topology of single phase voltage source inverter

These topologies require only a single dc source and for medium output power applications ('V_i' is the input dc supply and) a large dc link capacitor (C_{dc}) is required across the supply terminals. Capacitors and switches are

connected to dc bus using short leads to minimize the stray inductance between the capacitor and the inverter switches.

In the voltage source inverter the voltage remains constant with variations in the load. It is capable of supplying variable voltage for speed control of induction motor. Both the switches S_1 and S_2 or S_3 and S_4 cannot be simultaneously operated because short circuit across the dc link voltage V_i would be produced. There are four defined and one undefined state. The undefined state is avoided, in order to avoid the short circuit across the dc bus and the undefined ac output voltage condition. The modulating technique should ensure that either the top or the bottom switch of each leg is on at any instant. It can be observed that the ac output voltage can take values up to the dc link value V_i. Several modulating techniques have been developed that are applicable to the VSIs. Among them sinusoidal PWM technique is considered for VSI.

III.   SINGLE PHASE CURRENT SOURCE INVERTER

The circuit of a Single-phase Current Source Inverter (CSI) is shown in Fig. 2. A constant current source is assumed here, which may be realized by using an inductance of suitable value, which must be high, in series with the current limited dc voltage source. The thyristor pairs, Th_1 & Th_3, and Th_2 & Th_4, are alternatively turned ON to obtain a nearly square wave current waveform. Two commutating capacitors -C_1 in the upper half, and C_2 in the lower half, are used. Four diodes, D_1-D_4 are connected in series with each thyristor to prevent the commutating capacitors from discharging into the load. The output frequency of the inverter is controlled in the usual way, i.e., by varying the half time period, (T/2), at which the thyristor in pair are triggered by pulses being fed to the respective gates by the control circuit, to turn them ON. The inductance (L) is taken as the load in this case, the reason(s) for which need not be stated, being well known.
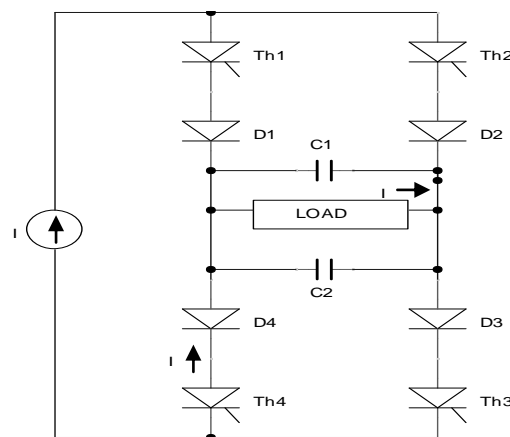

Fig.2 single phase current source inverter topology

At time, t = 0, thyristor pair, Th_1 & Th_3, is triggered by pulses at the gates. The conducting thyristor pair, Th_2 & Th_4, is turned OFF by application of reverse capacitor voltages. Now, thyristor pair, Th_1 & Th_3, conducts current (I). The current path is through Th_1, C_1, D_1, Load, C_2, D_3, Th_3, and source, I. Similarly the when the thyristor pairs, Th_2 & Th_4, is triggered by the pulses at the gates. The conducting thyristor pair Th_1 & Th_3 is turned OFF by the application of reverse capacitor voltages. Now, thyristor pair, Th2 & Th4, conducts current (I). The current path is through T_2, D_2, C_1, Load, C_2, D_4, T_4. The output frequency of the inverter is controlled in the usual way, i.e., by varying the half time period, (T/2), at which the thyristor in pair are triggered by pulses being fed to the respective gates by the control circuit, to turn them ON. The R, RL, Motor load is considered for analyzing the performance of the given CSI.

IV.   SINGLE PHASE Z-SOURCE INVERTER

A unique impedance network is used in the Z-source inverter that consists of two identical inductors L_1 and L_2 along with two identical capacitors C_1 and C_2 that couples the power supply to the inverter circuit. The shoot through period ie, the time period when the switch S_1 in fig 3(b) is gated allowing the voltage to be boosted to the required values when the input dc voltage is not up to the required level. Else otherwise the shoot through states is not used thus enabling the ZSI to operate as both a buck-boost inverter unlike the traditional VSI and CSI. Fig 3 shows the presence of the Z-source impedance network preceding the switch S_2 and succeeding switch S_1. There are two basic Z-source converter topologies [10], including voltage fed and current fed, as shown in Fig. 3(a) and 3b).
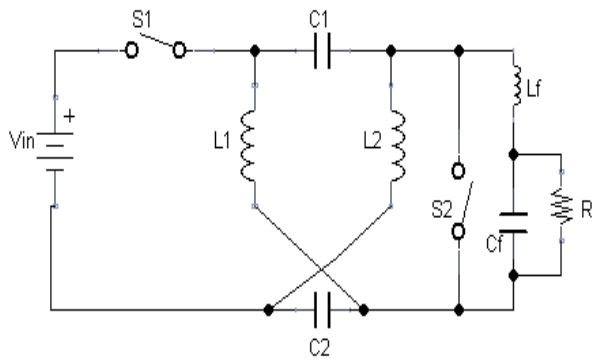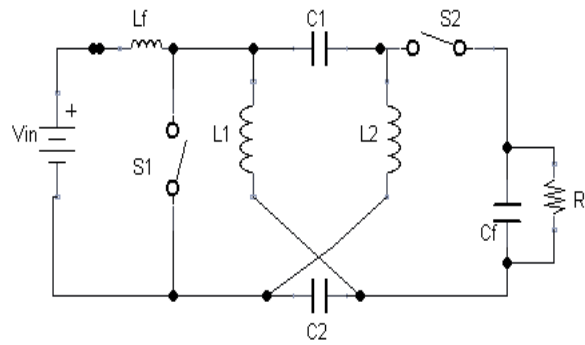
Fig. 3 (a) Voltage fed *Z*- source converter   Fig. 3 (b) Current fed *Z*- source converter

The *Z*-source networks are symmetric in these topologies. S_1 and S_2 are turned on and off in complement. Defining the duty ratio of S_1 as *D*, we can then get the relationship between voltage ratio and *D* of the voltage-fed and current-fed topologies, respectively, as

$$\frac{V_o}{V_i} = \frac{D}{2D-1} \cdot \frac{V_o}{V_i} = \frac{2D-1}{D-1} \tag{1}$$

For the voltage-fed topology, it clearly shows that there are two discontinuous operation regions. For the current-fed topology, we can see that the output voltage varies continuously. When *D* is less than 0.5, the output voltage is in phase with the input voltage. When *D* is greater than 0.5, the output voltage is out of phase with the input voltage. Fig. 4 (a) shows the basic single-phase Z-source inverter topology. $V_i= V_C$ can be derived easily in steady state from Fig. 4(a); then we can get the improved topology with input and output sharing the same ground, as shown in Fig. 4(b).
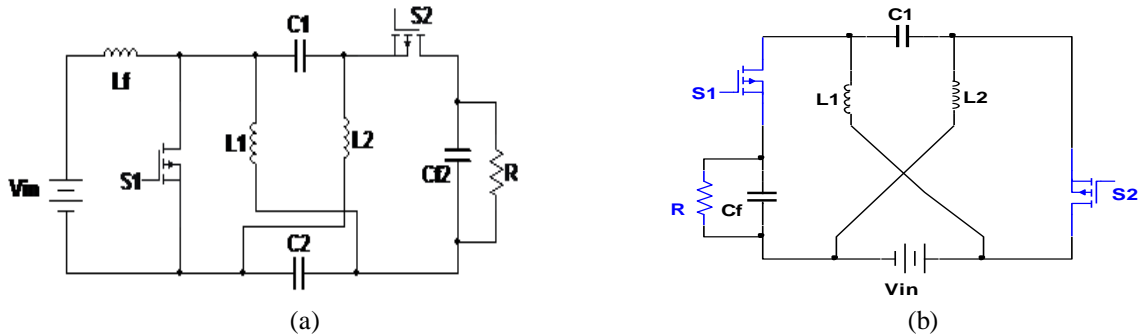

(a)   (b)

Fig. 4(a) Basic topology of Single-phase Z-source inverter, (b) Improved topology of Single-phase Z-source inverter

The unsymmetrical *Z*-source network is composed of input voltage source V_i , capacitor C_1 C_2, and inductors L_1 and L_2, where L_1 and L_2 can be coupled with required coupling factor.

V. OPERATING PRINCIPLE OF SINGLE PHASE Z-SOURCE INVERTER

The duty ratio of S_1 is D and the coupled inductor of L_1 and L_2 is M. Two states exist in one switching period, and Fig.4 shows their equivalent circuits.
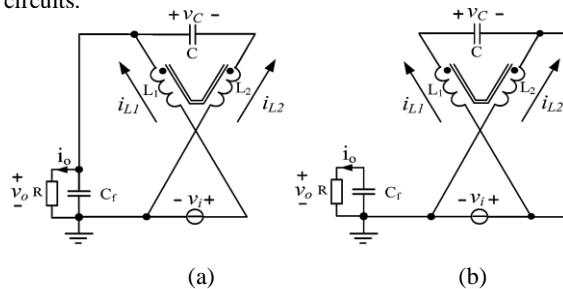

(a)   (b)

Fig. 5. Equivalent circuits in one switching period (a) State 1. (b) State 2.

In state 1, switch S_1 is turned on and S_2 is turned off. The time interval in this state is DT, where T is the switching period, as shown in Fig. 5(a). For active state of the switch S_1 the voltage induced in the inductors L_1 and L_2 are represented as

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} + M \dfrac{di_{L2}}{dt} = v_i - v_o \\ L_2 \dfrac{di_{L2}}{dt} + M \dfrac{di_{L1}}{dt} = v_c - v_o \\ C \dfrac{dv_c}{dt} = -i_{L2} \\ C_f \dfrac{dv_o}{dt} = i_{L1} + i_{L2} - i_o \end{cases} \tag{2}$$

In state 2, $S2$ is turned on and $S1$ is turned off. The time interval in this state is $(1–D)T$, as shown in Fig. 5(b). .For active state of the switch S_2 the voltage induced in the inductors L_1 and L_2 are represented as

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} + M \dfrac{di_{L2}}{dt} = -v_c \\ L_2 \dfrac{di_{L2}}{dt} + M \dfrac{di_{L1}}{dt} = -v_i \\ C \dfrac{dv_c}{dt} = i_{L1} \\ C_f \dfrac{dv_o}{dt} = -i_o \end{cases} \tag{3}$$

From (2) and (3), we can get the averaged equation

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} + M \dfrac{di_{L2}}{dt} = D(v_i - v_o) - (1 - D)v_c \\ L_2 \dfrac{di_{L2}}{dt} + M \dfrac{di_{L1}}{dt} = D(v_c - v_o) - (1 - D)v_i \\ C \dfrac{dv_c}{dt} = -Di_{L2} - (1 - D)i_{L1} \\ C_f \dfrac{dv_o}{dt} = D(i_{L1} + i_{L2}) - i_o \end{cases} \tag{4}$$

In steady state, we get

$$\begin{cases} V_c = V_i \\ \dfrac{V_o}{V_i} = \dfrac{2D - 1}{D} \\ i_{L1} = i_o \\ i_{L2} = \dfrac{1 - D}{D} i_{L1} \end{cases} \tag{5}$$

In the traditional three-phase *Z*-source inverter, the *Z*-source network works in the half region (*D* <0.5) to perform only voltage boost conversion. The proposed topology performs an unsymmetrical characteristic. As can be derived from (5), when *D* <0.5, the converter performs the buck–boost conversion and the polarity of output is inverse. When *D* >0.5, the converter performs only the buck conversion and the polarity of output is the same. As we know, a small *D* will cause parasitic effects to be more prominent and degrade the inverter performance. The chosen topology, it performs as a buck inverter when *D* is varied from 1/3 to 1. *D* is always greater than 1/3, so the parasitic effects are not prominent. Equation (5) also infers that unbalance of i_{L1} and i_{L2} is related to *D*. To perform the dc–ac conversion, *D* is varied between 1/3 and 1

VI.   Sinusoidal Pulse Width Modulation

SPWM is one of the most popular and simple methods utilized in power inverter and motor control fields. Its main features can be summarized as sine-triangle wave comparison. As shown in Fig.6, a sine wave (modulated wave) is compared with a triangle wave (carrier wave) and when the instantaneous value of the triangle wave is less than that of the sine wave, the PWM output signal is in high level (1). Otherwise it is turned into the low level (0). The level switching edge is produced at every moment the sine wave intersects the triangle wave. Thus the different crossing positions result in variable duty cycle of the output waveform. Sine and triangle waves are respectively generated by specially designed circuits and then fed to the properly selected comparator which can output the desired SPWM signal.
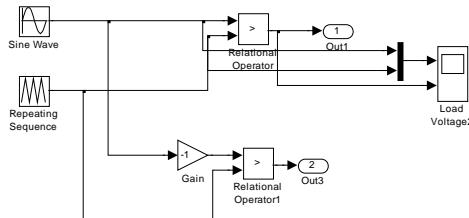

Fig.6. Sinusoidal pulse width modulation for proposed system
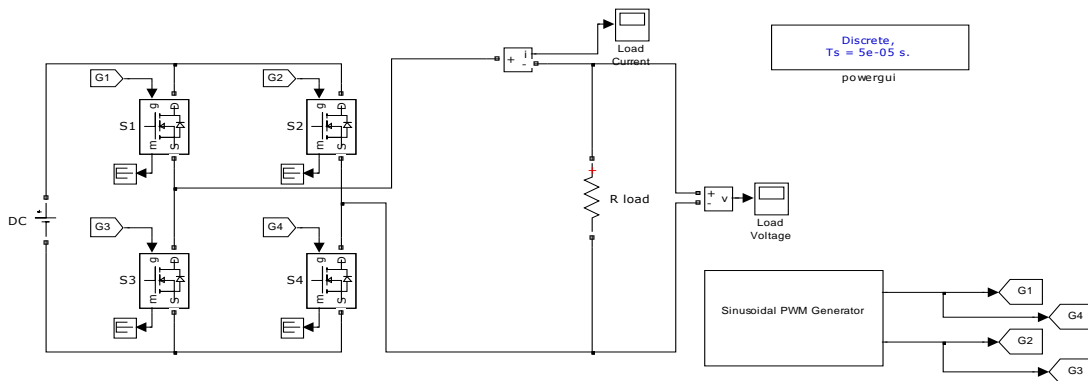
VII.   Simulation Results

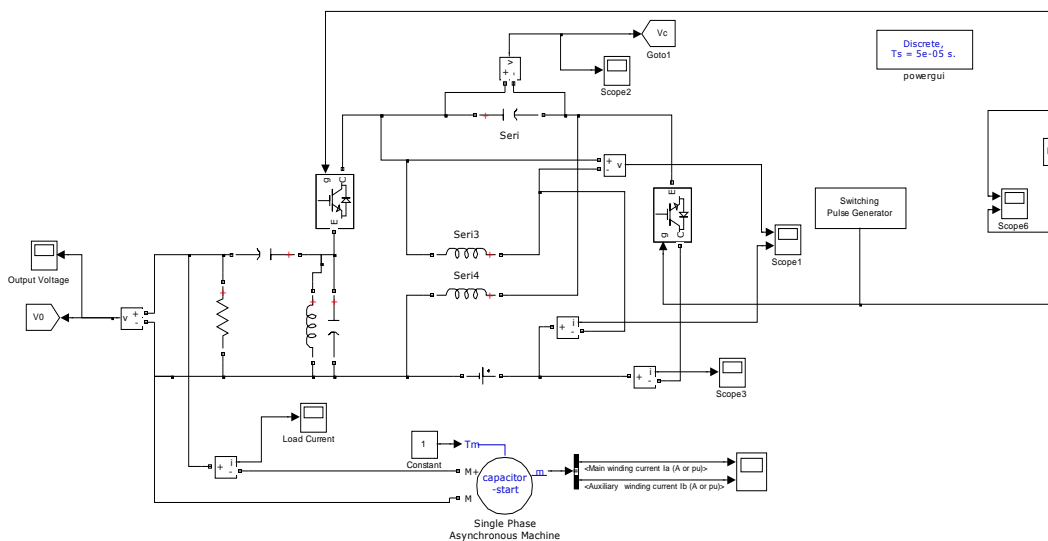Fig.7. Simulink of Voltage source inverter with R-Load

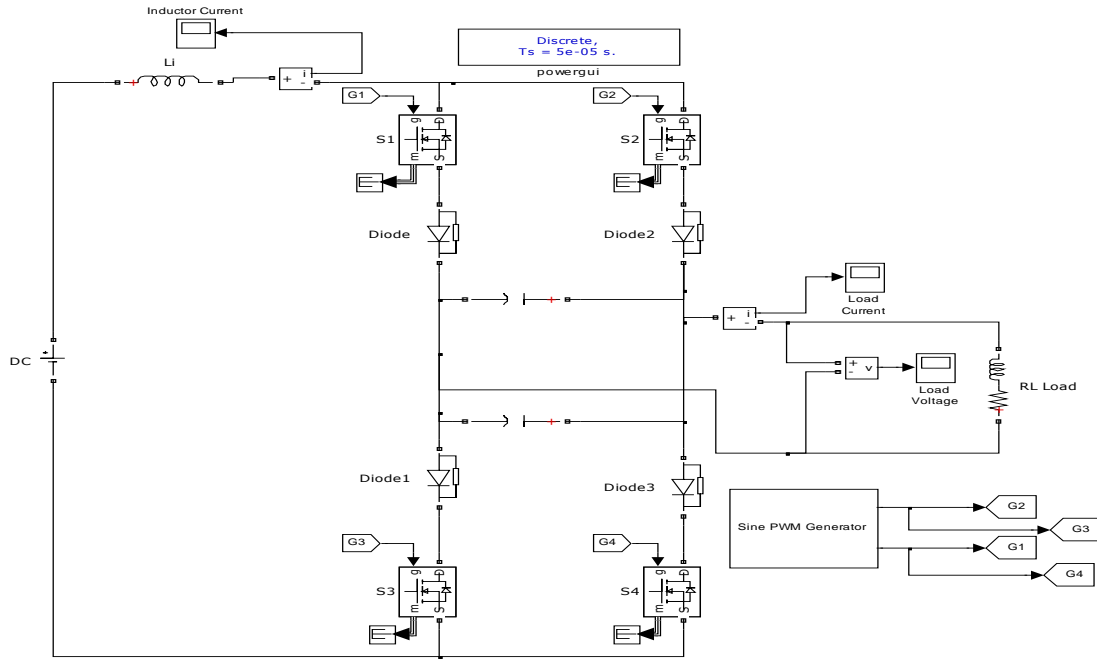Fig.8. Simulink of Current source inverter with RL- Load

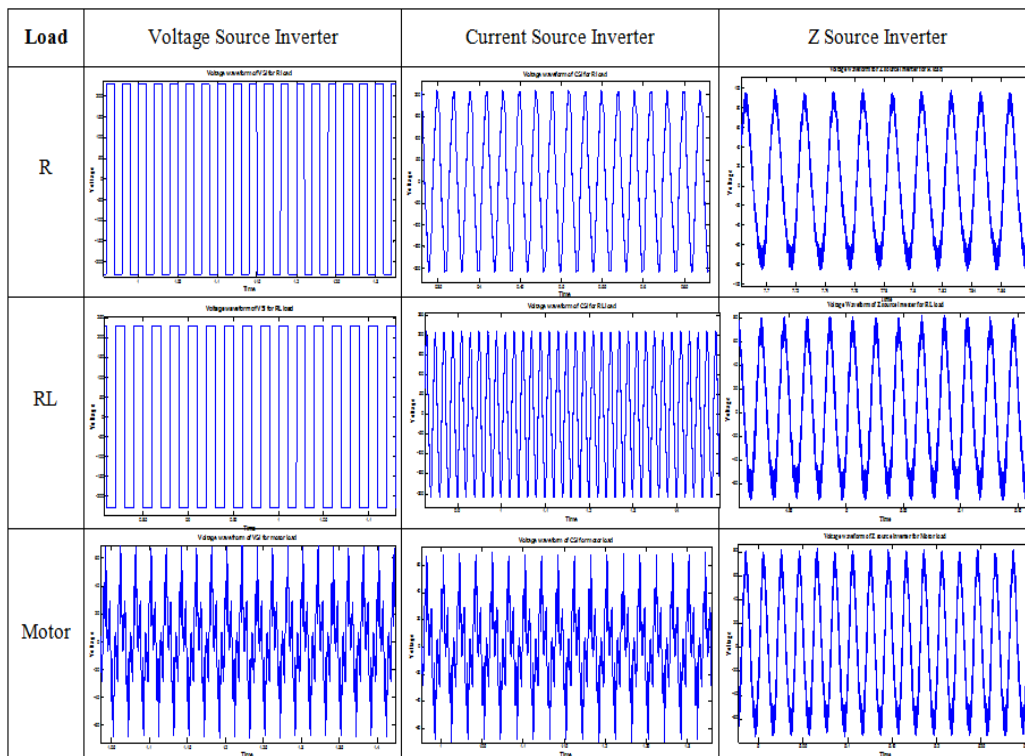Fig.9. Simulink of Z- source inverter with Motor-Load

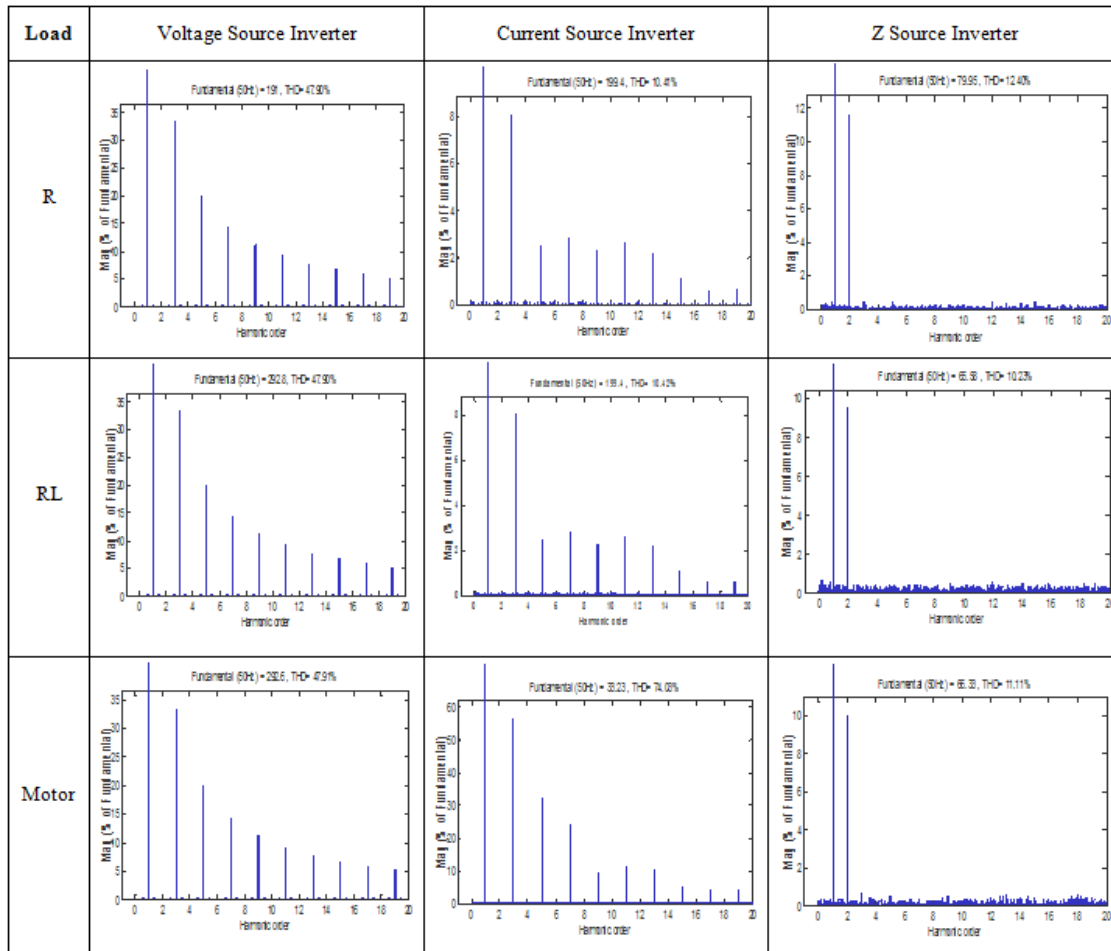Fig.10. Output Voltage of VSI, CSI and ZSI for various Load conditions

Fig.11. FFT analysis of VSI, CSI and ZSI for various Load conditions

Table.1. % Total Harmonic Distortion for RL load

Modulation Index (mₐ)	% THD for RL Load		
	Voltage Source Inverter (VSI)	Current Source Inverter (CSI)	Z- Source Inverter (ZSI)
1.0	47.90	10.42	10.23
0.9	78.47	11.78	10.23
0.8	127.81	12.43	10.23
0.7	269.05	14.21	10.23
0.6	981.25	14.71	10.23

Table.2. % Total Harmonic Distortion for Motor load

Modulation Index (mₐ)	% THD for Motor Load		
	Voltage Source Inverter (VSI)	Current Source Inverter (CSI)	Z- Source Inverter (ZSI)
1.0	47.91	74.03	11.11
0.9	56.78	65.79	11.11
0.8	96.23	66.14	11.11
0.7	156.12	93.99	11.11
0.6	3851.25	170.71	11.11

VIII. Conclusion

Conventional single-phase inverter topologies cannot achieve a common ground between the input and output, so they cannot be used in conditions where dual grounding is needed. To solve this problem, a novel single-phase Z-source inverter topology with an inherent common ground for input and output has been given. The operation principle and sinusoidal pulse width modulation control strategy are analyzed in detail and verified by simulation results. The results were compared with Voltage and Current Source Inverter, and it is observed that THD are relatively less in ZSI when compared with VSI and CSI.

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