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Efficient Design of Transceiver for Wireless Body Area Networks

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Abstract : *This paper investigates the efficient design of the PHY layer architecture for wireless body area networks (WBAN), which targets on ultra-low power consumption with reliable quality of service (QoS). A low cost baseband transceiver specification and a data processing flow are proposed with a comparatively low-complexity control state machine. A multifunctional digital timing synchronization scheme is also proposed, which can achieve packet synchronization and data recovery.*
Keywords *– Transceiver, TX Baseband, RX Baseband, WBAN*

I. INTRODUCTION

Wireless sensor networks are poised to transform the way society interacts with the physical world, driven by an explosion of systems research in sensor networks. The pursuit of higher quality of life motivates people to be more concerned about their health and potential diseases. At the same time, many patients can benefit from continuous monitoring of their diagnostic procedures. All these require a convenient healthcare surveillance system to monitor people's health status anytime anywhere, especially when people suffer an acute event, such as a sudden heart attack. The tracking capability of such a system should also be able to provide optimal maintenance after a surgical procedure and support early detection of abnormal health conditions.

Recent years have seen a burgeoning interest in embedded wireless sensor networks with applications ranging from habitat monitoring to medical applications.Recent advances in sensors, integrated circuits, and wireless communication are paving the way for developing miniature, lightweight, ultra-low power physiological healthcare surveillance and monitoring devices for the improvement of human lives. These devices can be integrated into wireless body area networks (WBANs) for health monitoring [1]. A WBAN topology consists of a series of miniature invasive/non-invasive physiological sensors and is able to communicate with other sensor nodes or with a central node [2]. The central node has higher computational capability and communicates wirelessly with a personal server and subsequently the outside world through a standard telecommunication infrastructure, such as wireless local area networks and cellular phone networks. Potential applications of WBANs include chronic disease management, medical diagnostics, home-monitoring, biometrics, and sports and fitness tracking, etc. [3], [4]. The power budget is quite strict for WBAN applications because the wireless device is powered by a battery.

In this paper, an optimized low power low data rate digital baseband IC is proposed, and its performance is analyzed in detail. The complete system requirements are illustrated in Table I. This chip is designed for low data rate and low power consumption. The working environment is the indoor WBAN application with 1 5 m working range. The specified raw data rate is 250 kb/s. The required signal-to-noise ratio (SNR) for 1% PER is 17 dB. The target power consumption is less than 100 W. Benefiting from the novel low complexity hardware architecture design and optimized hardware implementation, the proposed application-specific integrated circuits (ASIC) can achieve lower power consumption as compared with [5]. The proposed baseband transceiver is configured with a frequency-shift keying (FSK) modulation/demodulation module. Specified physical layer (PHY) architecture is developed, which reduces the complexity of baseband processing but maintains satisfactory performance

To recover precisely the timing and data information from an FSK demodulator, a novel synchronization and data recovery (SDR) scheme is proposed that has comparatively low complexity. To overcome the timing drift between the transmitter and receiver, a low-complexity sampling point realignment scheme is proposed. This scheme shares the same hardware with the SDR scheme and can automatically adjust to the correct sampling point during data transmission

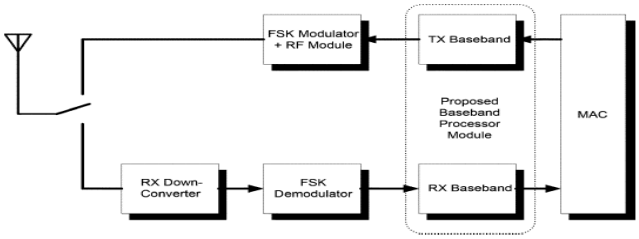

Fig.1. Block diagram of a complete WBAN radio transceiver

II. TX BASEBAND

The complete system diagram of a WBAN radio transceiver is shown in Fig. 1. In the transmitter block, the physical layer service data unit (PSDU) from the MAC layer is processed in the proposed transmitter (TX) baseband processor module to generate a physical layer protocol data unit (PPDU) packet. The channel coding and signal processing are performed on the PPDU in the TX baseband processor module, and the raw data rate of the TX baseband processor module output is 250 kb/s. The baseband raw data is modulated by FSK and then directly up-converted to a 2.45 GHz RF signal. In the receiver (RX) block, the received RF signal is down-converted to a 2 MHz intermediate frequency (IF) signal and then demodulated by a low power FSK demodulator. The demodulated signal is processed by the proposed RX baseband processor module. Following that, the received PSDU is fed into the MAC layer.

To achieve ultra low power consumption, a low-complexity PHY specification is proposed. The signal processing flow for TX and RX are presented in Figs. 2 and 3, respectively. In the TX module, the baseband processor receives the PSDU from the MAC layer and constructs the PPDU. The permitted length of the PSDU within one packet should be no larger than 127 octets, and this information is contained in the PHY header (PHR) in octets. Once one packet of the PSDU is generated by the MAC layer, it is fed into TXFIFO and ready for transmission. There is a Prefix MUX block controlled by the TX state control block to select the input of the Hamming encoder block.

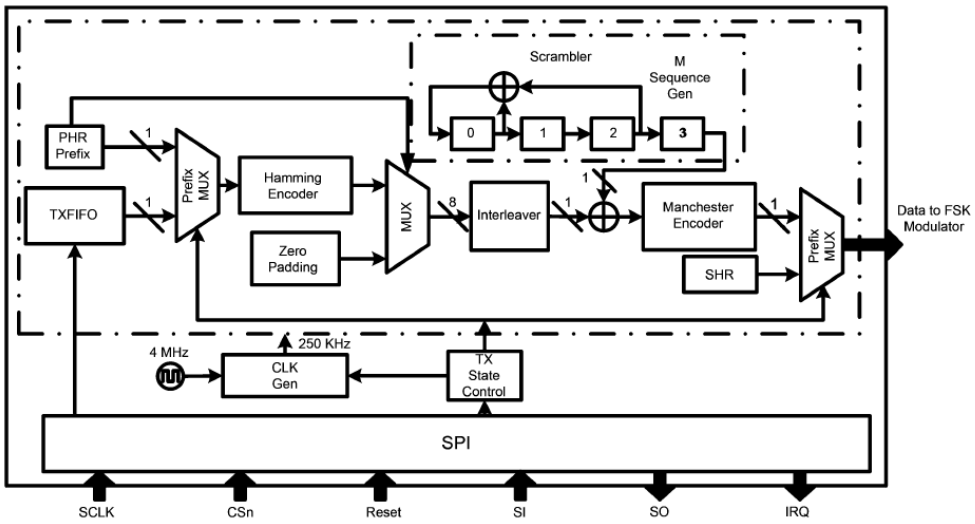

Fig.2. Block diagram of baseband TX

When a transmission command is sent from the MAC layer, the PHR is prefixed to the PSDU and sent into the Hamming encoder block first. The input data of the Hamming encoder block is in serial sequence with 1 bit word-length. In our design, (8, 4) Hamming coding and 8 4 matrix interleaving are used as forward error correction (FEC) coding and will be introduced in Section III.

For each consecutive 4 bits of input data, the Hamming encoder block generates 8 bits of output data simultaneously, and thus the word-length of the Hamming encoder block output is 8 bits. The output data of the Hamming encoder block is fed into the 8 4 matrix interleaving block to suppress the burst error. To eliminate long strings of like bits that might impair receiver synchronization and to eliminate most periodic bit patterns that could produce undesirable frequency components (including the dc component), the interleaved data payload is first fed into a scrambling block and then coded by a Manchester encoder. The scrambling block generates the scrambling code in serial sequence with 1 bit word-length. Here we use the sequence generator with as the scrambler to achieve satisfactory performance and comparatively low complexity. The output data of the interleaving block is in serial sequence with 1 bit word-length and is XORed with the generated scrambling code. The scrambled data payload is fed into the Manchester encoder. The Manchester encoder converts the bit "0" to bits "01" and converts the bit "1" to bits "10," and thus the total number of "0" and "1" can be balanced. The output of the Manchester encoder is prefixed with the synchronization header (SHR) and is sent to the FSK modulator for transmission.

III. RX BASEBAND

In the receiver module, the received data stream is the demodulated binary signals from the FSK demodulator. We use the D flip-flop provided by the technology library to sample and to restore the analog input. If the voltage of the input signal is higher than of the D flip-flop, the output of the D flip-flop will be "1." If the voltage of the input signal is lower than of the D flip-flop, the output of the D flip-flop will be "0." As

illustrated in Fig. 3, the signals are first serially fed into the synchronization and data recovery (SDR) block to achieve synchronization and to recover the received data. The SDR block over-samples the incoming signal using a shift register matrix block and calculates the correlation between the incoming data and the predefined preamble sequence to achieve bit synchronization. The peak of the calculated correlation is continuously detected. Once the peak value is found, the start-of-frame delimiter (SFD) Correlates block calculates the correlations between the incoming data and the predefined SFD sequence, and the peak value is searched by the following peak detector block. Once the peak value is found, the packet synchronization is confirmed.

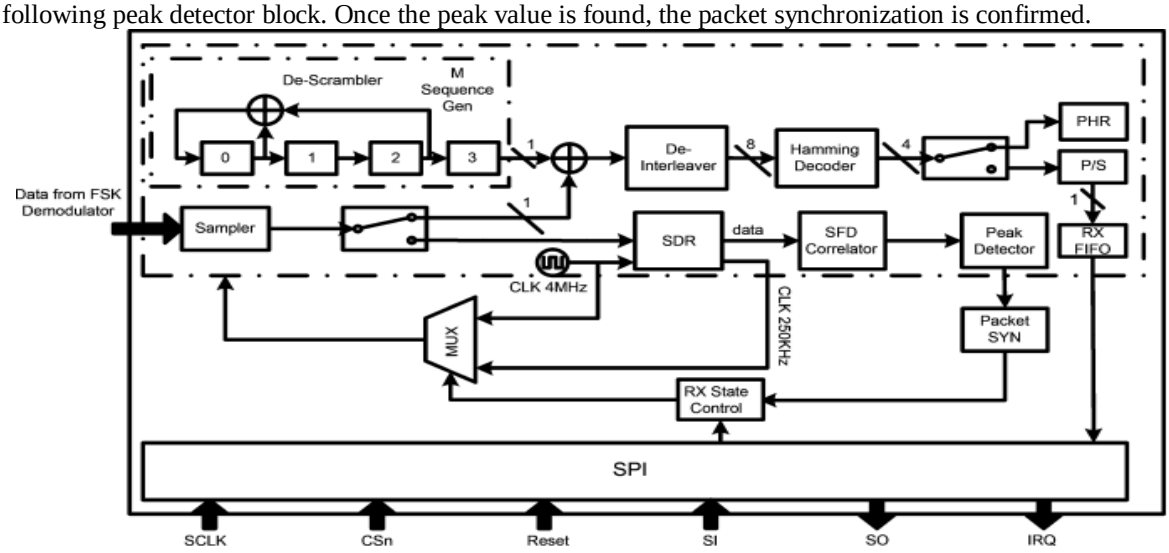

Fig.3. Block diagram of baseband RX

The preamble sequence and SFD are removed and the Packet SYN block indicates to the RX State Control block that the PHR and PSDU can be received. The SDR block also generates the 250 kHz clock, and the RX State Control block selects the operation clock frequency of the RX baseband processor module which can be between 4 MHz clock and 250 kHz clock. Manchester decoding is first performed on the received PHR and PSDU data stream by detecting the first bit for every two continuous received bits.

Following that, the incoming data is descrambled, and the structure of the descrambling block is identical to that of the scrambling block. The output of the descrambling block has a 1-bit word-length, and XOR operations are completed with the incoming data bit by bit. Following that, the PHR and PSDU are fed into the FEC decoding block, which includes the deinterleaving block and Hamming decoder block. The output of the deinterleaving block has an 8-bit word-length and is fed into the Hamming decoder block. The Hamming decoder block checks whether there is any error in the incoming data and corrects the error. If the Hamming decoder block detects an error but cannot correct it, the receiver will stop receiving any data and the MAC layer will request a retransmission of this packet. The PHR is decoded first and thus length information about the PSDU can be obtained by the RX state control block. The word-length of the Hamming decoder block output is 4 bits, and there is a parallel to serial buffer, so that bits in the PSDU are fed into the RXFIFO in serial sequence with 1 bit word-length, and is read by the MAC layer.

IV. RESULTS

To achieve performance optimization and a short design period, the proposed baseband transceiver design requires a smooth and highly efficient design flow. VHDL RTL code is created to describe the PHY system and SPI and is verified on a Xilinx field-programmable gate array (FPGA) test platform. It can be observed that the derived analysis result can serves as an upper bound. From this figure, it can be found that there is a significant performance gain after using FEC coding in terms of BER performance. Note that in this section, we mainly focus on the performance comparison of analysis and measurement in an AWGN channel due to the space limitation. However, the comparison for fading channels can easily be verified using similar derivations. Our targeted operation clock frequency is 4 MHz, however, the fabricated baseband chip can still work properly at the maximum clock frequency of 100 MHz, and thus the maximum accepted raw data rate is 6.25 Mb/s. The comparison of power consumption between the proposed chip and existing baseband transceivers is provided in chart. Note that in this table, the power consumption of our proposed chip also includes the operation of the TX/RX FIFO and the SPI control module.

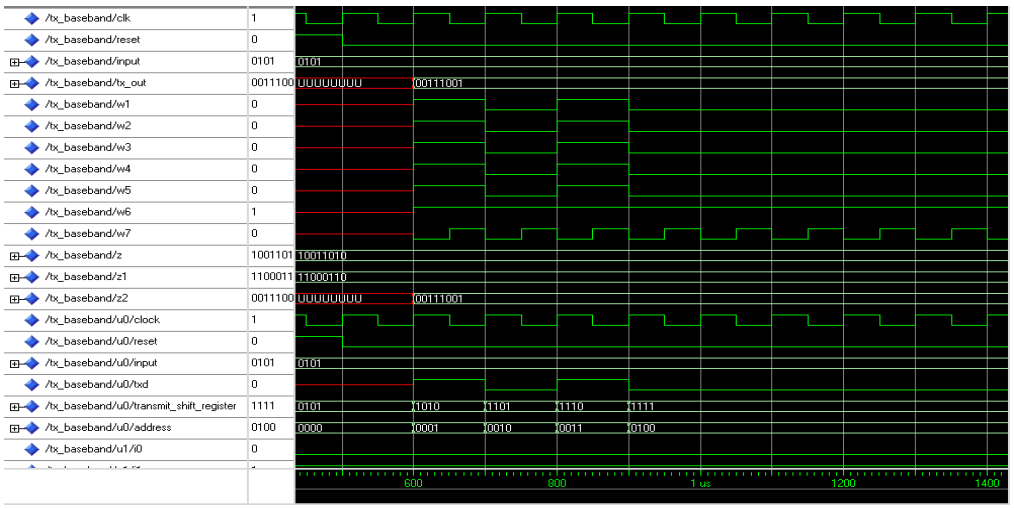

Fig. 4 Simulated waveform of TX baseband

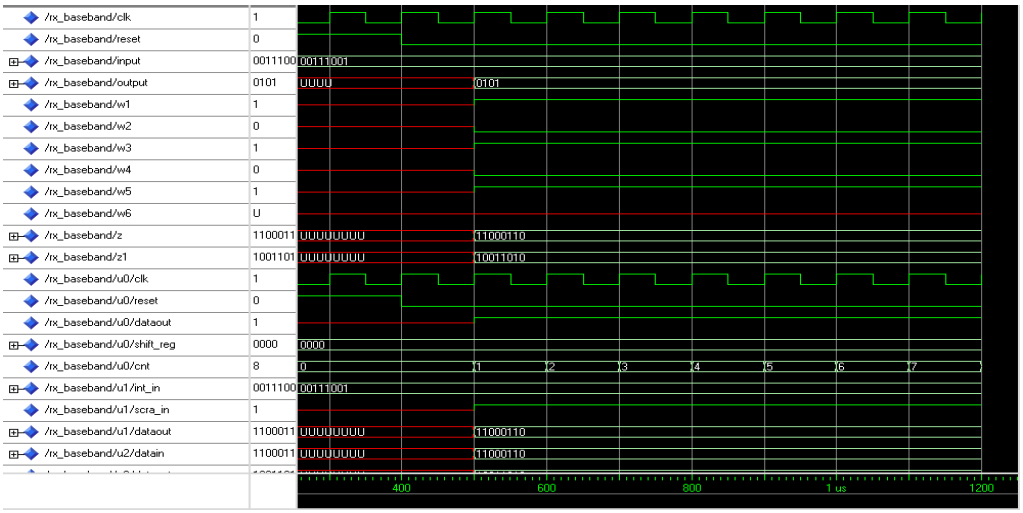

Fig. 5 Simulated waveform of RX baseband

V. CONCLUSION

In this paper, we proposed a low complexity baseband PHY transceiver IC. It is implemented in Xilinx FPGA and consumes only 58mW and 59mW for TX and RX respectively at a 4 MHz operation clock frequency. The measured PER performance and power consumption verify the satisfactory performance of the proposed design. This digital baseband chip is extremely suitable for low-rate WBAN applications and can also be used for other communication baseband PHY processing with scalable data rate.

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