

Application of SVM Technique for Three Phase Three Leg Ac/Ac Converter Topology

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Abstract: Ac-ac power conversion, the most popular topologies are indirect ac-ac converters with a dc link matrix converters and direct pulse width modulation (PWM) ac-ac converters. The indirect ac-ac converters and matrix converters can provide variable output voltage and variable frequency. However, for applications, where only voltage regulation is needed, the direct PWM ac-ac converters are used to perform as ac choppers or power line conditioners with the following features: the provision of a better power factor and efficiency, low harmonic current in line, single-stage conversion, simple topology, ease of control, smaller size, and lower cost. The ac-ac conversions or ac-ac line conditioners can also perform conditioning, isolating, and altering of the incoming power in addition to voltage regulation. The direct PWM ac-ac converters can be derived from the dc-dc topologies, where all the unidirectional switches are substituted by bidirectional devices.

This paper presents simulation of a Three-phase Three-leg Ac/Ac Converter simulation design using reduced number of power semiconductor devices, here nine IGBTs are used. This converter features sinusoidal inputs and outputs, unity power factor, and more importantly, low manufacturing cost. The experimental results from a 5kVA prototype system are provided.

Index Terms -AC/AC converter, reduced switch count topology, SVPWM

I. Introduction

THREE-PHASE ac/dc/ac and ac/ac converters with variable frequency (VF) and variable voltage operation have found broad applications in the industry. The most popular configuration uses voltage source inverter (VSI) with a diode rectifier as the front end for adjustable speed drives (ASDs), uninterruptible power supplies (UPS), and other industrial applications. This configuration features low cost and reliable operation due to the use of a diode rectifier, but it generates highly distorted input line currents and does not have regenerative or dynamic braking capability. These problems can be mitigated by using a back-to-back two-level voltage source converter, shown in Fig.1, where a PWM voltage source rectifier is used to replace the diode rectifier the back-to-back converter configuration requires 12 active switches such as IGBTs with increased manufacture cost. In addition, it needs a large size dc capacitor. To reduce the device count and minimize/eliminate the dc capacitor filter, various converter topologies have been proposed in the literature.

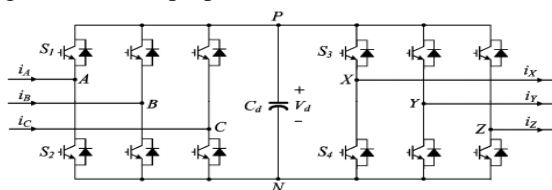


Fig.1 Conventional back-to-back converter topology

One of the promising converter topologies is the matrix converter. This converter presents a radical change in topology and directly converts a fixed ac input voltage to an adjustable ac output voltage. It is capable of bi-directional energy transfer for the supply to the load or vice versa. There is no dc link circuit, and therefore the dc capacitor filter in the back-to-back converter is not required. However, the matrix converter normally requires 18 IGBT switches and its switching scheme is complex. The high cost and complex control have made this topology less attractive.

The proposed three-phase nine-switch converter topology has only three legs with three switches installed on each of them. The novelty here is that the middle switch in each individual leg is shared by both the rectifier and the inverter, thereby reducing the switch count by 33% and 50% in comparison to the B2B 2L-VSC. The input power is delivered to the output partially through the middle three switches and partially through a quasi-dc-link circuit. The circuit can be considered that the rectifier of the nine-switch converter is composed of the top three and middle three switches, whereas the inverter consists of the middle three and bottom three switches. The converter uses space vector PWM (SVM) method which is an advanced

computation-intensive PWM method and is possibly the best among all the PWM techniques for variable-frequency drive applications.

II. Space Vector Modulation

The space vector PWM (SVM) method is an advanced computation-intensive PWM method and is possibly the best among all the PWM techniques for variable-frequency drive applications. Because of its superior performance characteristics, it has been finding wide speed applications in recent years. The desired three phase voltages at the output of the inverter could be represented by an equivalent vector \mathbf{V} rotating in the counter clock wise direction as shown in Fig.3. The magnitude of this vector is related to the magnitude of the output voltage (Fig.4) and the time this vector takes to complete one revolution is the same as the fundamental time period of the output voltage.

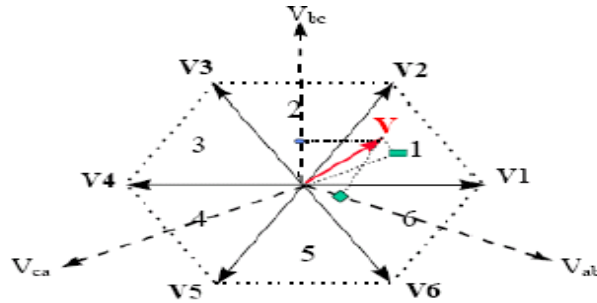


Fig.2 Output voltage vector in the α - β plane

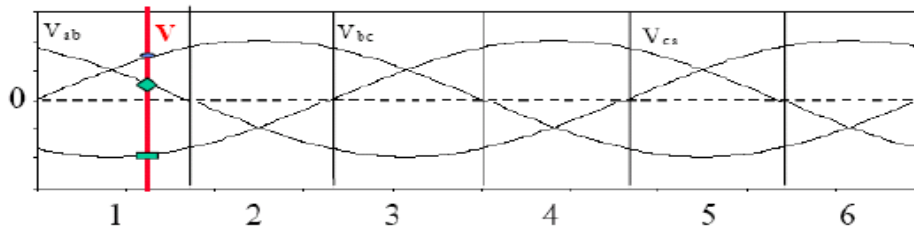


Fig.3 Output line voltages in time domain

Let us consider the situation when the desired line-to-line output voltage vector \mathbf{V} is in sector 1 as shown in Fig.3. This vector could be synthesized by the pulse-width modulation (PWM) of the two adjacent SSV's $\mathbf{V1}$ (pnn) and $\mathbf{V2}$ (ppn), the duty cycle of each being d_1 and d_2 , respectively, and the zero vector $\mathbf{V7}$ (nnn) / $\mathbf{V8}$ (ppp) of duty cycle d_0 :

$$d_1 V_1 + d_2 V_2 = V = m V_g e^{j\theta} \dots\dots\dots(1)$$

$$d_1 + d_2 + d_0 = 0 \dots\dots\dots(2)$$

Where, $0 \leq m \leq 0.866$, is the modulation index. This would correspond to a maximum line-to-line voltage of $1.0V_g$, which is 15% more than conventional sinusoidal PWM as shown.

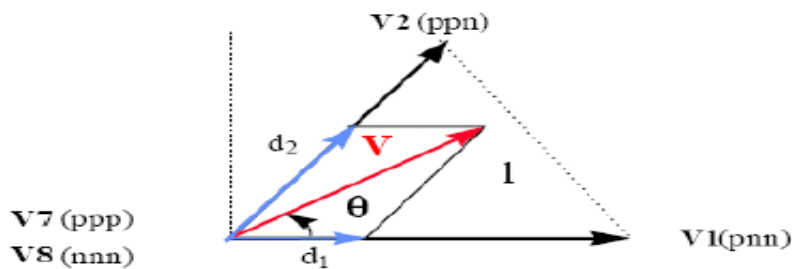


Fig.4 Synthesis of the required output voltage vector in sector 1

All SVM schemes and most of the other PWM algorithms use Eqns. (1) and (2) for the output voltage synthesis. The modulation algorithms that use non-adjacent SSV's have been shown to produce higher THD and/or switching losses and are not analyzed here, although some of them, e.g. hysteresis, can be very simple to implement and can provide faster transient response. The duty cycles d1, d2, and d0, are uniquely determined, and Eqns. (1) and (2), the only difference between PWM schemes that use adjacent vectors is the choice of the zero vector(s) and the sequence in which the vectors are applied within the switching cycle.

The degrees of freedom we have in the choice of a given modulation algorithm is:

- 1) The choice of the zero vector; whether we would like to use **V7**(ppp) or **V8**(nnn) or both,
- 2) Sequencing of the vectors
- 3) Splitting of the duty cycles of the vectors without introducing additional commutations.

2.1 Output voltages of three-phase inverter

S1 through S6 are the six power transistors that shape the output voltages. When an upper switch is turned on (i.e., a, b or c is “1”), the corresponding lower switch is turned off (i.e., a', b' or c' is “0”).

Eight possible combinations of on and off patterns for the three upper transistors (S1, S3, S5)

Line to line voltage vector [V_{ab} V_{bc} V_{ca}]^t

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}, \text{ where switching variable vector } [a \ b \ c]^t .$$

(3)

Line to neutral (phase) voltage vector [V_{an} V_{bn} V_{cn}]^t

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{1}{3} V_{dc} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} .$$

------(4)

Table1. Tabulation of Output voltages of three-phase inverter

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V _{an}	V _{bn}	V _{cn}	V _{ab}	V _{bc}	V _{ca}
V ₀	0	0	0	0	0	0	0	0	0
V ₁	1	0	0	2/3	-1/3	-1/3	1	0	-1
V ₂	1	1	0	1/3	1/3	-2/3	0	1	-1
V ₃	0	1	0	-1/3	2/3	-1/3	-1	1	0
V ₄	0	1	1	-2/3	1/3	1/3	-1	0	1
V ₅	0	0	1	-1/3	-1/3	2/3	0	-1	1
V ₆	1	0	1	1/3	-2/3	1/3	1	-1	0
V ₇	1	1	1	0	0	0	0	0	0

(Note that the respective voltage should be multiplied by V_{dc})

2.2 Basic switching vectors and Sectors

- 6 active vectors (V₁, V₂, V₃, V₄, V₅, V₆)
 1. Axes of a hexagonal.
 2. DC link voltage is supplied to the load.
 3. Each sector (1 to 6): 60 degrees.
- Two zero vectors (V₀, V₇)
 1. At origin
 2. No voltage is supplied to the load

III. Nine-Switch Converter Topology

Fig.5 shows the proposed three-phase nine- switch converter topology. This converter has three legs with three switches per leg. The novelty of this converter is that the middle switch in each of the three converter legs is shared by the rectifier and inverter, thereby reducing the switch count by 33% and 50% in comparison to the back-to-back converter and matrix converter, respectively. The input power is delivered to the output partially through the middle three switches and partially through a *quasi* dc link circuit. For the convenience of discussion, we can consider that the rectifier of the nine-switch converter is composed of top three and middle three switches.

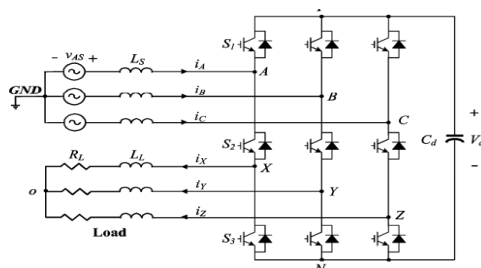


Fig.5 proposed three-phase nine- switch converter topology

IV. Simulation Analysis

The performance of the proposed nine-switch converter topology is simulated by simulink software. The utility supply is rated 208V and 60Hz with a supply inductance of $L = 2.5\text{mH}$. The converter is loaded with a three phase RL load of $R_s = 8$ ohms and $L = 2.5\text{mH}$. The dc capacitor C_{dl} is $2350 \mu\text{F}$. The rectifier is controlled by a vector control scheme with unity power factor operation. The inverter output voltage is not detected and therefore is not tightly controlled. The switching frequency of both rectifier and inverter is 3240Hz. Both CF and VF modes of operation are investigated.

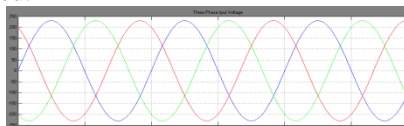


Fig.6 Three phase Input voltage

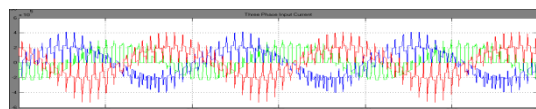


Fig7. Three phase input Current

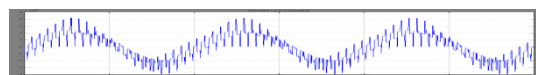


Fig8. Rectifier Line current(Ix)

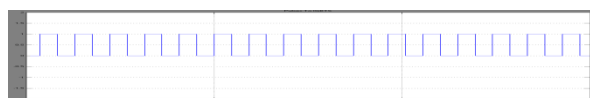


Fig9. Pulses to IGBTs

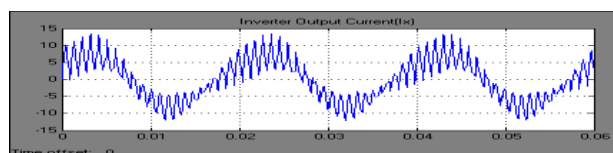


Fig10. Inverter Output current(Ix)

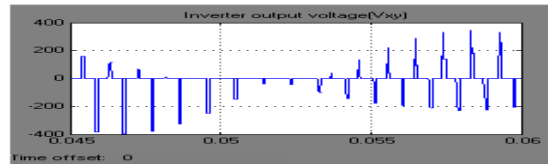


Fig11. Inverter output voltage(v_{xy})

V. Conclusion

A novel nine-switch PWM ac/ac converter topology using SVM technique was proposed in this paper. The topology uses only nine IGBT devices for ac to ac conversion through a quasi dc-link circuit. Compared with the conventional back-to-back PWM VSC using 12 switches and the matrix converter that uses 18, the number of switches in the proposed converter is reduced by 33% and 50%, respectively. The proposed converter features sinusoidal inputs and outputs, unity input power factor, and low manufacturing cost. The operating principle of the converter was elaborated, and modulation schemes for constant and VF operations were developed. Simulation results including a semiconductor loss analysis was provided, which reveal that the proposed converter, while working in CF mode, has an overall higher efficiency than the B2B 2L-VSC at the expense of uneven loss distribution. However, the VF-mode version requires IGBT devices with higher ratings and dissipates significantly higher losses, and thus, is not as attractive as its counterpart. Experimental verification is carried out on a 5-kVA prototype system.

This paper analyzed the Back to Back inverter topology, and the more complex three-phase-leg topologies with the modulation concepts and derived carrier-based reference equations verified in simulation for all presented voltage-type -source inverters, and experimentally for a three-phase-leg -source inverter. The paper presents the Three-phase Three-leg Ac/Ac converter topology using Space vector Modulation technique for IGBT pulses. Experiments have been carried out to verify the validity of the proposed scheme.

Reference

- [1] B. Wu, *High-power Converters and AC Drives*. Piscataway, NJ:IEEE/Wiley, 2006.
- [2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Ko thari, "A review of three-phase improved p ower quality AC – DC converters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, Jun. 2004.
- [3] F. B laabjerg, S. Frey sson, H. H. Hansen, and S. Hansen, "A new op-timized space-vector m odulation strategy for a component-minimized vo ltage source inverter," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 704–714, Jul. 1997.
- [4] R. L. A. R ibeiro, C. B. Jacobina, E. R. C. d a Silva, and A. M. N. Lima, "AC/AC converter with four switch three phase structures," in *Proc. IEEE PESC*, 1996, vol. 1, pp. 134–139.
- [5] K. Gi-Taek and T. A. Lipo, "VSI-PWM rectifier/inverter system with a reduced switch count," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1331– 1337, Nov./Dec. 1996.
- [6] A. B ouscayrol, B. Francois, P. Delarue, and J. Niiranen, "Control imple- mentation o f a five-leg AC–AC converter to supply a three-phase induction machine," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 107–115, Jan. 2005.
- [7] C. B. Jacobina, I. S. de Freitas, E. R. C. da Silva, A. M. N. Lima, and R. L. A. Ribeiro, "Reduced switch count DC-link AC–AC five-leg converter," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1301–1310, Sep. 2006.
- [8] C. B. Jacobina, I. S. de Freitas, and A. M. N. Lima, "DC-link three-phaseto- three-phase four-leg converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, pp. 1953–1961, Aug. 2007.
- [9] J. Minibock and J. W. Kolar, "Novel concept for mains voltage proportional input current shaping of a VIENNA rectifier eliminating controller multipliers," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 162–170, Feb. 2005.
- [10] T. Nussbaumer, M. Baumann, and J.W. Kolar, "Comprehensive design of a three-phase three-switch buck-type PWM rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 551–562, Mar. 2007.
- [11] F. A. B. Batista and I. Barbi, "Space vector modulation applied to threephase three-switch two-level unidirectional PWMrectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2245–2252, Nov. 2007.
- [12] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: A technology review," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 276–288, Apr. 2002.
- [13] L. Wei, T. A. Lipo, and H. Chan, "Matrix converter topologies with reduced number of switches," in *Proc. IEEE PESC*, 2002, vol. 1, pp. 57–63.
- [14] J.W. Kolar, F. Schafmeister, S. D. Round, and H. Ertl, "Novel three-phase AC–AC sparse matrix converters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1649–1661, Sep. 2007.