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Optimization of Threshold Voltage for 65nm PMOS Transistor using Silvaco TCAD Tools

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Abstract *: In this paper, a 65nm scaled channel of PMOS is fabricated and studied its electrical characteristics. Athena module of SILVACO software was use. The two characteristics such as Id – Vg and Id – Vd reading Vth parameters for both characteristics for different process parameters like: gate oxide thickness, channel doping and channel implantation. From the simulation result of VTH value is achieved -2.55427v for 65nm PMOS transistor. That is well known within ITRS(international technology roadmap for semiconductor) for a 65nm PMOS transistor.*

Keywords *- Include 65nm PMOS, Threshold voltage, Channel length, Silvaco TCAD*

I. INTRODUCTION

A MOSFET may also be referred to as a unipolar device due to the nature of its design. Specifically, the majority carriers in the channel region can be of only one type (electrons or holes). The MOSFET with electrons as the majority carriers in the channel is entitled an n-channel MOSFET or NMOS. Similarly, the MOSFET with holes as the majority carriers in the channel is a p-channel MOSFET or PMOS.There are many reasons why the MOSFET has been the most popular device for a vast array of applications. Since the 1970s the MOSFET has been the prevailing device in microprocessors, memory circuits and logic applications of many kinds . The fabrication process for MOSFET has become very mature over the 25 to 30 year lifetime of this device [1]. These mature fabrication processes leads to less errors and discrepancies in circuit construction and gives rise to a higher yield of good devices. This technology is now well-developed and similar processes of MOSFET fabrication are widely used in industry throughout the world [2].

Structural physical downscaling of Complimentary Metal-Oxide Semiconductor (CMOS) started in the early 1970s (Taur, 1995), and it has given us many challenges and technology discoveries. The speed of downscaling has been showing exponential growth since then, as end users crave for more new technologies in their daily life. One of the main complications in producing a smaller transistor is to control the threshold voltage (V_{TH}) [3]. To introduce the CMOS designer to the technology that is responsible for the semiconductor devices that might be designed. The basics of semiconductor manufacturing are first introduced. Following this, a number of enhancements to the basic CMOS technology are described. Next, layout design rules and the nature of CMOS latch are introduced. Finally, CAD issues related to process technology are covered [4].

V_{TH} is one of the important output parameter. It is one of a main factor in determining whether transistor works or not [5]. The three fabrication factors selected and analyzed are gate oxide thickness, implant doping concentration and channel doping concentration. The short channel effect and hot carrier reliability are controlled by lightly doped drain (LDD) [6]. Besides that, light doped drain (LDD) is designed to smear out the strong electric field between the channel and heavily doped source or drain, in order to reduce hot-carrier generation. Retrograde well is a form of vertical channel engineering that used to improve SCE and to increase surface channel mobility by creating a low surface channel concentration followed by a highly doped subsurface region [5].

II. MATERIALS AND METHODS

Threshold Voltage: Threshold voltage is defined as the minimum voltage that required to make the transistor ON. Transistor may be either nmos or pmos. For nmos the value of threshold voltage is positive value and for pmos the value of threshold voltage is negative value. It is a minimum gate voltage in the transistor at which the conduction of current begins. Threshold voltage(V_{TH}) is the voltage level at which the transistor turns ON and the drain to source (I_{ds}) current starts conducting. Threshold voltage can be defined as the voltage required to create a strong inversion.

Body Effect: The body effect describes the changes in the threshold voltage by the change in V_{SB}, thets source-bulk voltage. Since the body influences the threshold voltage (when it is not tied to the source), it can be thought of as a

second gate, and is sometimes referred to as the "back gate", the body effect is sometimes called the "back-gate effect".

Channel Length: It is also called gate length. I am talking about the channel length of a typical MOS transistor. However, there are 3 ways to measure gate length: 1) from the photo mask, 2) actual length between source and drain edges, and 3) the effective gate length which takes into account encroachment and LDD features underneath the gate.

Silvaco TCAD: TCAD refers to Technology Computer-Aided Design**.** This means that computer simulations are used to develop and optimize semiconductor processing technologies and devices. As TCAD simulations solve fundamental, physical partial differential equations, such as Poisson, Diffusion and Transport equations in a semiconductor device. This deep physical approach gives TCAD simulation predictive accuracy. It is therefore possible to substitute TCAD simulations for costly and time-consuming test wafer runs when developing and characterizing a new semiconductor device or technology.

Process Technology of TCAD: Produce small layout test structures, and Then fabricate these structures using initial guess values for unknown process parameters. Electrical device testing on complete structures are then perform to determine if the device meet the device fabrication. If not, the cycle is repeated with new sets of estimated process parameters. Usually, this whole cycle will be repeated for many times before the desired results are obtained [4].

- Basically, Silvaco TCAD Tools consists of 2 Main branches.
- They are the ATHENA process simulation and ATLAS device simulation.
- All these simulators works in a integrated environment know as the Virtual Wafer Fab Interactive Environment.

III. VAROATION FACTOR

There are three factors that influence the threshold voltage values (6). The purpose of this variation factor that more dominant in determine V_{th} value. The variations values as follow:

- Gate oxide thickness

  i. Variation 1 – 0.0020um
  ii. Variation 2 – 0.0025um
  iii. Variation 3 – 0.0060um

- Channel Implantation

  i. Variation 1 – phos (1.0x1013 atom cm1)
  ii. Variation 2 - phos (3.5x1013 atom cm-1)
  iii. Variation 3 – phos (7.0x1013 atom cm1)

- Channel doping

  i. Variation 1 – Boron ($1.0x10^{15}$)
  ii. Variation 2 – Boron ($2.0x10^{15}$)
  iii. Variation 3 – Boron ($4.0x10^{15}$)

For all three factors above, variation 2 is taken from the simulation. Variation 1 is the half of the variation 2 value and variation 3 is double of the variation 2 value.

IV. RESULT AND DISCUSION

The results of the fabrication and simulation of 65 nm PMOS can be viewed in the Tony Plot is shown below.

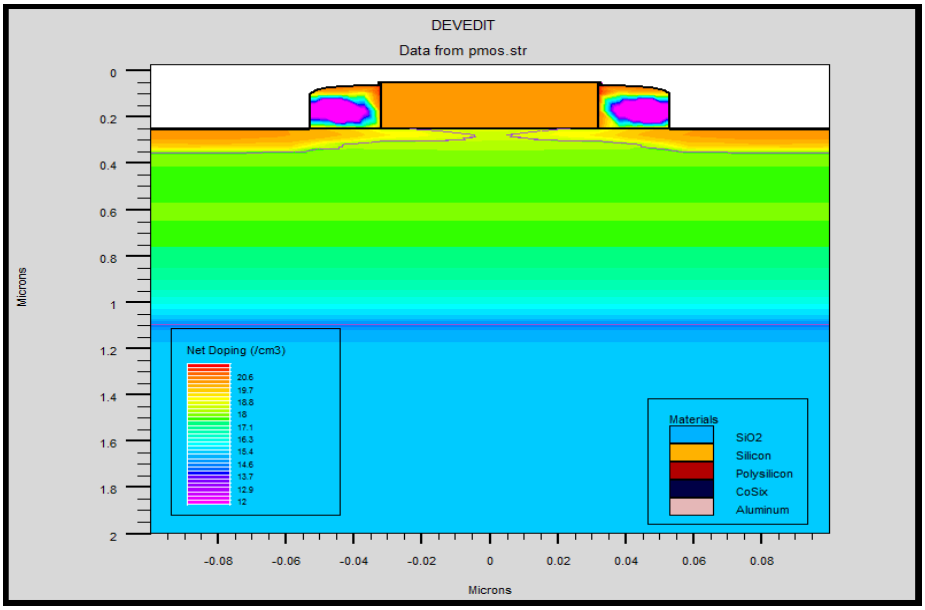

Figure 1: complete structure of 65 nm PMOS with net doping

Figure 1 show the electrodes are highlighted in this final structure of this MOSFET device. The complete structure now can be simulated in ATLAS to provide specific characteristics such as Id - Vg and Id - Vd curve.

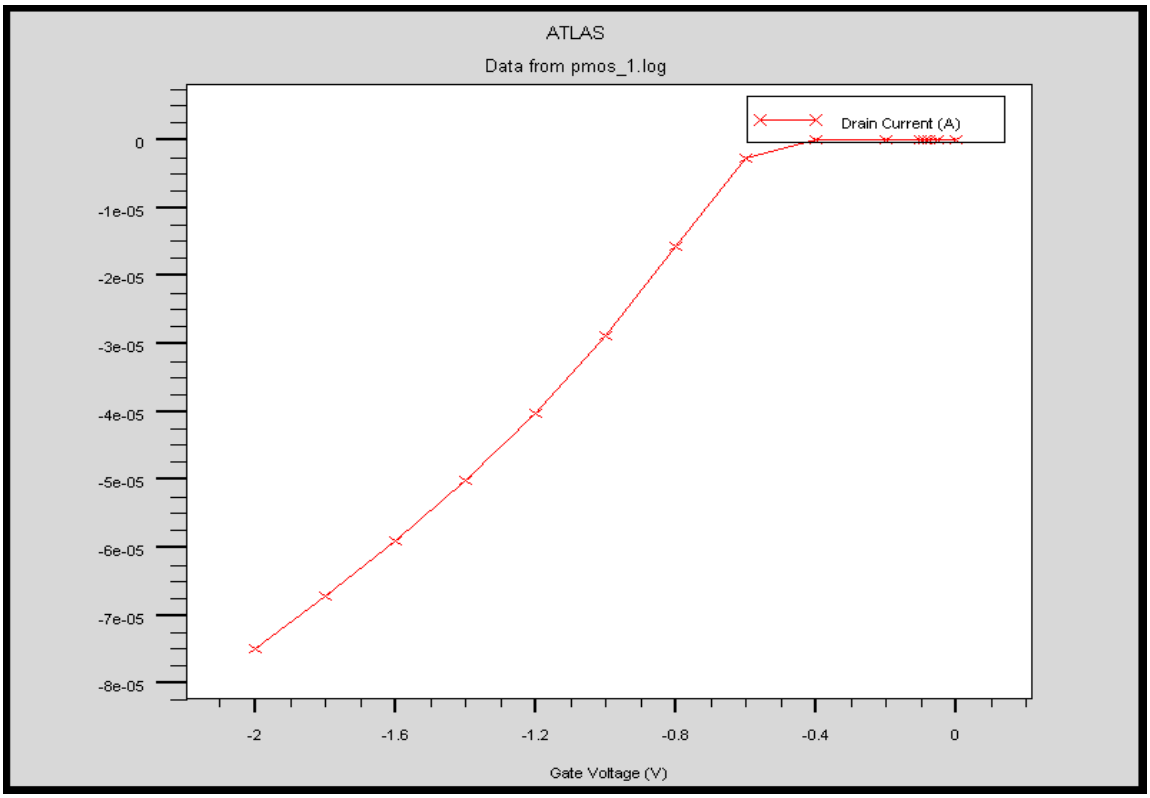

Figure 2: The Id versus Vg curve

Figure 2 shows that Id versus Vg curve for PMOS. By this curve, the value of threshold voltage (V_{TH}) can be extracted. In this operation the threshold voltage happens when current reaches zero. Vt = -0.5 is applied for this graph. When Vg> Vt, the current is zero but the current start increasing when Vg<Vt.

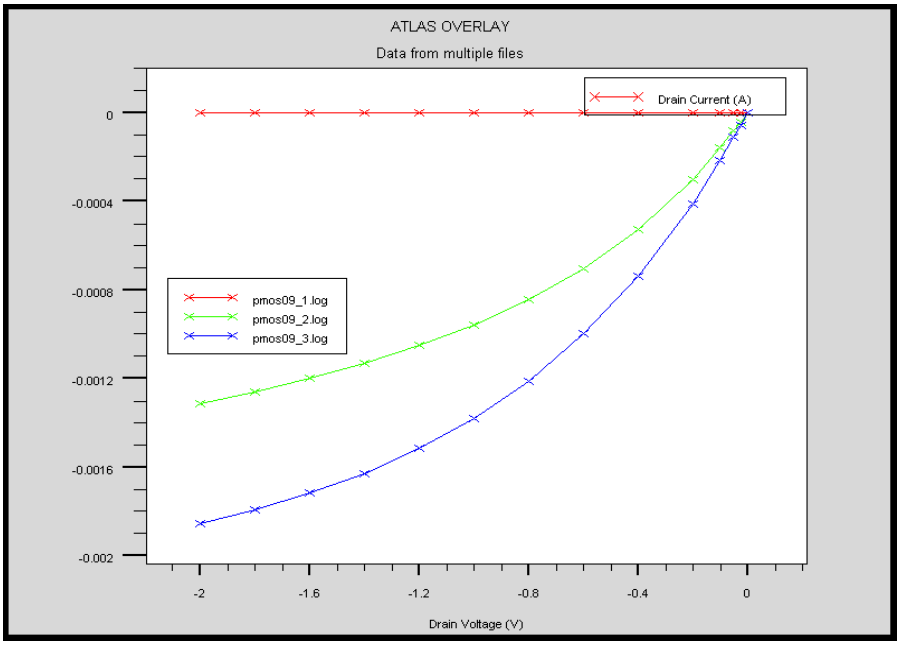

Figure 3: The Id versus Vd curve

Figure 3 shows that Id versus Vd curves for PMOS. Above curve is plotted by ATLAS simulator. The voltage that apply for red, green and blue line is -0.2V, -0.8V, and -1.2 V.

set	Factor 1	Factor 2	Factor 3	V_{TH}
1	1	1	1	-1.46993
2	1	1	2	-1.45928
3	1	1	3	-1.45237
4	1	2	1	-2.01034
5	1	2	2	-1.97892
6	1	2	3	-1.97752
7	1	3	1	-2.41923
8	1	3	2	-2.41901
9	1	3	3	-2.56869
10	2	1	1	-1.68352
11	2	1	2	-1.68197
12	2	1	3	-1.6947
13	2	2	1	-2.47151
14	2	2	2	-2.55427
15	2	2	3	-2.46328
16	2	3	1	-2.97793
17	2	3	2	-2.94688
18	2	3	3	-2.94588
19	3	1	1	-2.23176
20	3	1	2	-2.19486
21	3	1	3	-2.18582
22	3	2	1	-3.77602
23	3	2	2	-3.73584
24	3	2	3	-3.73412
25	3	3	1	-4.34154
26	3	3	2	-4.32963
27	3	3	3	-4.31922

Table 1: V_{TH} value from simulation

The table 1 shows 27 sets value of threshold voltage. From simulations, these results were obtained. The above table shows the best value of Vth is -2.55427. Above table, the Vth value is slightly different in set 2 and 3, 5 and 6, 7 and 8, 10 and 11, 17 and 18, 23 and 24. In this paper, there are three factors that have major effect on the value of threshold voltage. These three factors are gate oxide thickness, channel doping and Vth adjust implant. Each factors will be discussed in the below.

A. Effect of gate oxide thickness on threshold voltage

The figure 4 shows gate oxide thickness effect on threshold voltage. The first parameter was modified which is gate oxide thickness . The threshold voltage is effected by some parameter like: oxidation time, temperature and pressure. In this simulation the oxidation time and temperature was modified to gate the gate oxide thickness Value in line with ITRS guide line for 65 nm device. Increases the gate oxide thickness, Vth also increases(7). The gate capacitance is a reverse proportion of the gate oxide thickness. When the gate oxide capacitance increases then the gate oxide thickness goes down. It means that the gate less control to the channel. In order to invert the channel, the Vth will be increases (8).

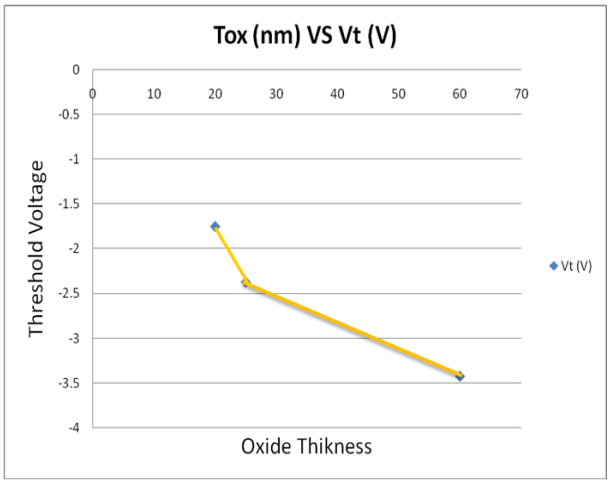

Figure 4: Threshold voltage at different gate oxide thickness

B. Effect channel implantation to the threshold voltage

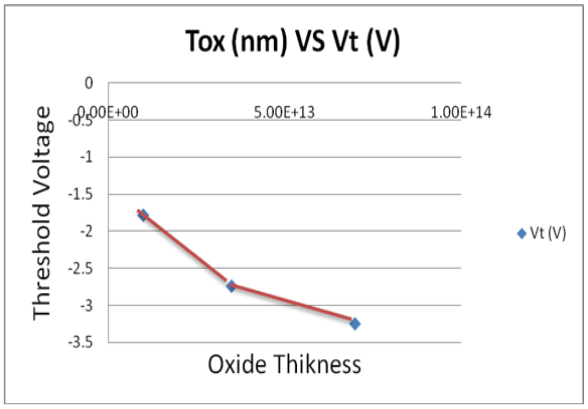

Figure 5: variation of threshold voltage at different channel implantation

Figure 5 shows the effect threshold voltage adjustment implantation to the threshold voltage. The Vth value adjust by using the threshold voltage adjust implantation. It also alters the doping profile near the surface of silicon substrate. In addition, the phosphorous implant acts to define the Vth of this device. If Vth increases then Vth adjust implantation doping also increases.

C. Effect channel doping to the threshold voltage

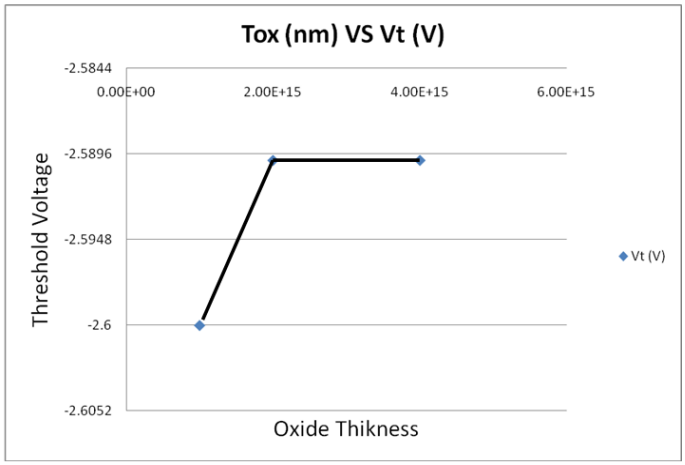

Figure 6: Threshold voltage at different channel doping

The figure 6 shows the channel doping increases then the threshold voltage increases, the Fermi potential increases and the channel depletion charge also increasing, it takes more effort to deplete the whole channel. Due to that region the Vth increases when the channel doping increases (8).

V. CONCLUSION

There are three factors that effect threshold voltage which is channel doping, gate oxide thickness and channel implantation. V_{TH} value of 2.55427 is achieved from this simulation. For 65 nm PMOS, the value is in line with international technology roadmap for semiconductor (ITRS) guideline. Due to punch through effect, the Id – Vd curve is not saturate.

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