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High Power Factor Boost Converter with Bridgeless Rectifier

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Abstract: A bridgeless power factor correction rectifier with boost converter is introduced. This converter substantially improves efficiency at low line of the universal-line range. By eliminating input bridge diodes during conduction, the proposed rectifier's efficiency is further improved. Moreover, the rectifier doubles its output voltage, which extends useful energy of the bulk capacitor after a dropout of the line voltage. Also second stage boost converter is included to maximize the output. The efficiency difference between low line and high line is less than 0.5% at full load. A second-stage half-bridge converter is also included to show that the combined power stages easily meet Climate Saver Computing Initiative Gold Standard.
Keywords— power factor (Pf), bridgeless rectifier, boost converter, phase difference.

I. Introduction

In universal-line (90–264V) applications, maintaining a high efficiency across the entire line range poses a major challenge for ac/dc rectifiers that require power factor correction (PFC). Driven by economic reasons and environmental concerns, maintaining high efficiency across the entire load and input-voltage range of today's power supplies is in the forefront of performance requirements. Specifically, meeting and exceeding U.S. Environmental Protection Agency's (EPA) Energy Star, and Climate Saver Computing Initiative (CSCI) efficiency specifications have become a standard requirement for both multiple- and single-output offline power supplies. Generally, the EPA and CSCI specifications define minimum efficiencies at 100%, 50%, and 20% of full load with peak efficiency at 50% load. For decades, a bridge diode rectifier followed by a buck converter has been the most commonly used PFC circuit because of its simplicity and good PF performance. This drop of efficiency at low line can be attributed to an increased input current that produces higher output voltage.

However, in practical application the Buck PFC converter has the following disadvantages: 1) The output voltage is below the limit of the input voltage. 2) There is the poor performance during the startup, the overloading and the non-load. 3) The high switching losses and EMI. They are resulted from the great ripple current flowing from the power switch and diode. 4) The bridge type converter increases the losses. 5) The control circuit is complex and high cost. In order to overcome these problems, in this paper, a single-phase bridgeless PFC rectifier with boost converter is presented.

In conventional method, a bridgeless buck PFC rectifier that further improves the low-line (115 V) efficiency of the buck front-end by reducing the conduction loss through minimization of the number of simultaneously conducting semiconductor components is introduced. It also works as a voltage doubler, it can be designed to meet harmonic limit specifications with an output voltage that is twice that of a conventional buck PFC rectifier. As a result, the proposed rectifier also shows better hold-up time performance. Although the output voltage is doubled, the switching losses of the primary switches of the downstream dc/dc output stage are still significantly lower than that of the boost PFC counterpart. Also the buck PFC converter does not shape the line current around the zero crossings of the line voltage, i.e., during the time intervals when the line voltage is lower than the output voltage, it exhibits increased total harmonic distortion (THD) and a lower PF compared to its boost counterpart. As a result, in applications where IEC61000-3-2 and corresponding Japanese specifications (JIS-C-61000-3-2) need to be met, the buck converter PFC employment is limited to lower power levels. The conventional buck converter operation and control is described in [1][2]and[3].

In proposed method PFC rectifier with boost converter is introduced to improve the PF furthermore, which is different from the normal bridge type rectifier and boost converter where, the operation consists of two diodes in conduction at each half cycle simultaneously ,one is in from upper leg and other is from lower leg. Here, the positive half cycle has two diodes and similarly the negative half cycle has two diodes. This type of operation requires high power to switching than the bridgeless operation. Also it increases the conduction loss. The bridgeless rectifier with boost converter increases the output nearly double the value or higher than that. When the supply is positive the first half cycle has one diode and one switch in conduction another will not conduct for a while this will continue until the switch is ON. When the switch is open another diode starts freewheels the current.

In the same way, for negative half cycle the diode in lower leg with second switch will conduct until the switch will open. When the switch is open another diode in the lower leg

will freewheels the energy through the closed path. Because of the bridgeless operation, number of conducting diodes simultaneously will reduced, which reduces the conduction losses and switching losses in the circuit. This will increase the efficiency and PF, back end of the rectifier consist boost converter to improve the voltage level furthermore. The bridgeless PFC converter operation is described first whereas additional circuit refinements and analysis were described in detail.

`The project work focuses on the power factor correction has the combination of the bridgeless rectifier with boost converter to the load. By comparing to the conventional method the proposed system provides improved power factor correction and it reduces the conduction and switching losses in circuit the proposed system increases the output voltage to get maximum output. Simulation presented to validate the proposed inverter configuration. The basic block diagram is shown in fig 1.

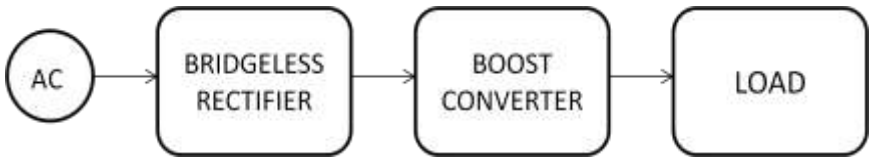


Fig.1.New topology block diagram

II. BRIDEGELESS RECTIFIER

The new topology consists of bridgeless converter and boost converter AC input, filter, load, and driver unit and pulse generator. Here the bridgeless rectifier is different from the normal rectifier which reduces input diodes during the operation.

The circuit diagram of proposed system is shown in fig 2. The bridgeless rectifier has normal bridge rectifier structure with two switches in between the legs which reduces the number of conducting diodes simultaneously.normal bridge rectifier has the two diodes during the conduction of each half cycle, in proposed circuit it is redused to one diode with the additional switch. After that second stage boost converter is added to maximise the output.The bridgeless converter is formed by the component D1, D2, D3, D4, L1, L2, C1, and C2. The boost converter is formed by the component L, D, Q and Co.

The peak output voltage in volts for the single phase bridge rectifier is given in following equation,

$$V_P(\text{out}) = V_P(\text{in}) - 2 * V_F \qquad (1)$$

Where, V_f is the forward-bias voltage drop across one diode.

Because there are two forward-biased diodes in the current path, the total drop would be twice the drop of one diode.

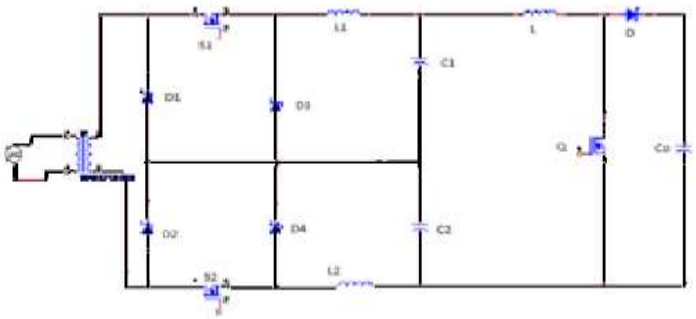


Fig.2.Proposed circuit configuration

III. Operation And Principle

Depending on the applied voltage the bridgeless rectifier has two modes in operation, the first one is during the positive voltage, and next one is during the negative voltage of the supply.when the applied voltage is positive. The buck converter operation and analysis is known from [5][7]and [8].

The converter illustrated in Fig.3, only operates during positive half-cycles of line voltage *V*ac and consists of a unidirectional switch implemented by diode *D*1 in series with switch *S*1, freewheeling diode *D*3, filter inductor *L*1, and output capacitor *C*1. During its operation, the voltage across capacitor *C*1, which must be selected lower than the peak of line voltage, is regulated by pulse width modulation (PWM) of switch *S*1. Similarly, the buck converter consisting of the unidirectional switch implemented by diode *D*2 in series with

switch *S*2, freewheeling diode *D*4, filter inductor *L*2, and output capacitor *C*2 operates only during negative half-cycles of line voltage *V*ac, as shown in Fig.4. During its operation, the voltage across capacitor *C*2 is regulated by the PWM of switch *S*2. Fig 3.

Operation of proposed bridgeless PFC rectifier is shown in Figs. 3 and 4 during the period when the line voltage is positive, negative. The input current always flows through only one diode during the conduction of a switch, i.e., either *D*1 or *D*2 . Efficiency is further improved by eliminating input bridge diodes in which two diodes carry the input current the waveforms are shown in fig 5. An additional advantage of the proposed circuit is its inrush current control capability. Since the switches are located between the input and the output capacitors, switches *S*1 and *S*2 can actively control the input inrush current during start-up. Output voltage *V*out of the PFC rectifier, which is the sum of the voltages across output capacitors *C*1 and *C*2 , is given by equation 2,

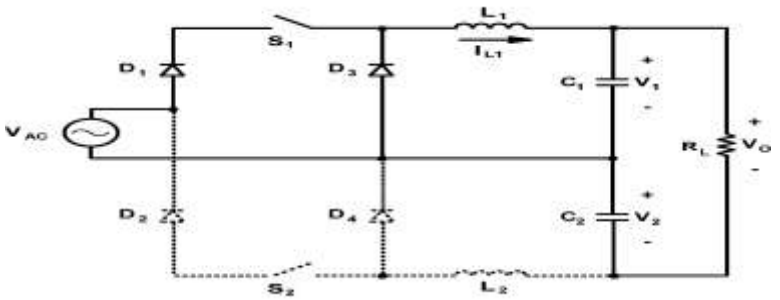


Fig. 3. Operation of the Bridgeless PFC Rectifier During The Period When the Line Voltage is Positive

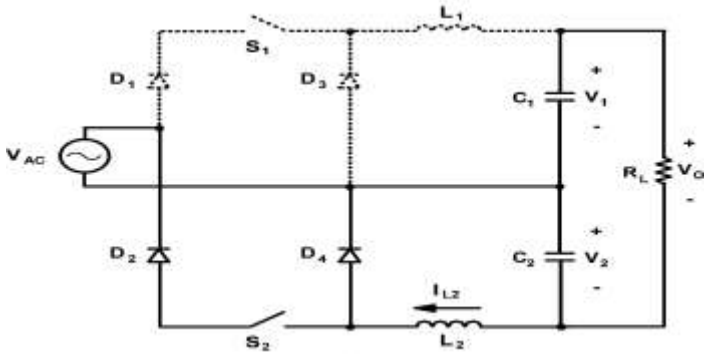


Fig. 4. Operation of the Bridgeless PFC Rectifier During The Period When the Line Voltage is negative

*V*out =2*DV*in (1) (2)

Where, *D* is the duty cycle and *V*in is the instantaneous rectified ac input voltage. The buck converter operation modes are explained in [4][6][9]and [10].

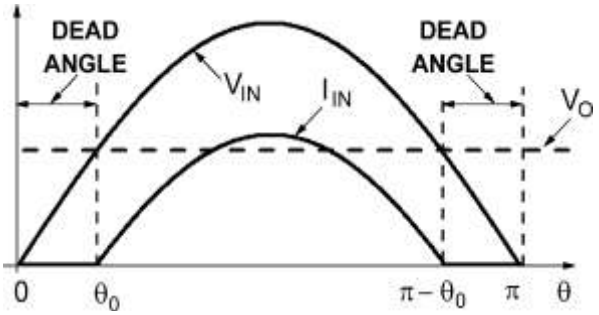


Fig. 5. Ideal Input Voltage and Input Current Waveforms of a PFC Rectifier

IV. Simulation And Experimental Results

Simulations were performed by using MATLAB and PSPICE to verify that the proposed converter. In the proposed bridgeless PFC rectifier, dc voltages across output capacitors *C*1 and *C*2 are automatically balanced. Namely, for a regulated output voltage *V*out, i.e., for a constant sum of the capacitor voltages *V*1 and *V*2 in Fig 2, any mismatching of capacitor voltages *V*1 and *V*2 will create differences in the input-current conduction angles during the positive and negative half of a line period, which will correct the mismatching of capacitor voltages. For example, if voltage *V*1 becomes greater than *V*2 for whatever reasons, the conduction

angle of the line current during the positive half of line cycle will be smaller than that during the negative half. Because of the extended conduction angle, capacitor *C*2, which has a lower voltage, will be charged more during negative half periods than capacitor *C*1, which has a higher voltage and is charged during positive half periods. This process will go on until the average voltages across capacitors *C*1 and *C*2 are balanced.

The simulation block diagram and result for the high power factor boost converter with bridgeless rectifier is given below.

Fig 6. Proposed converter circuit

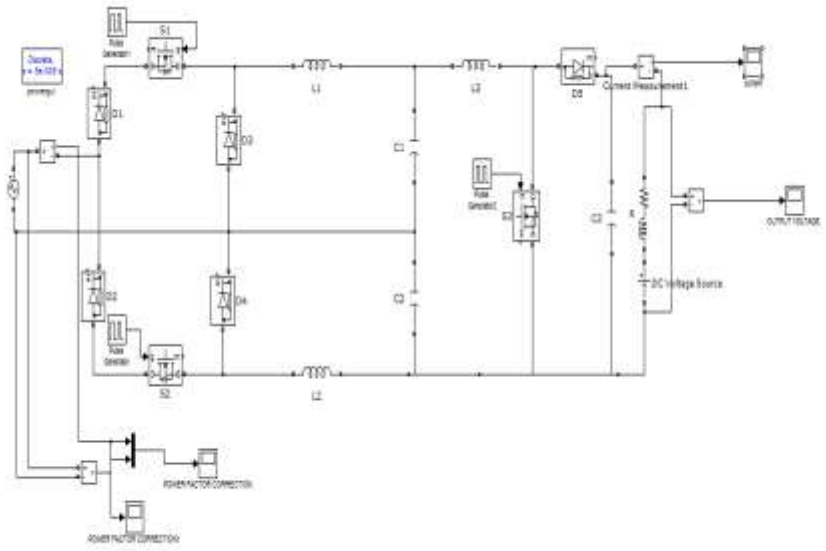


Fig 7. Input current and input voltage for proposed circuit

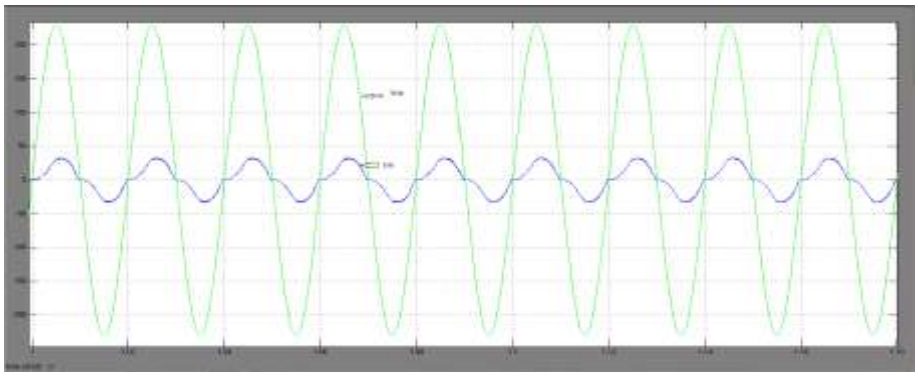


Fig.8. Output Voltage of Proposed Circuit

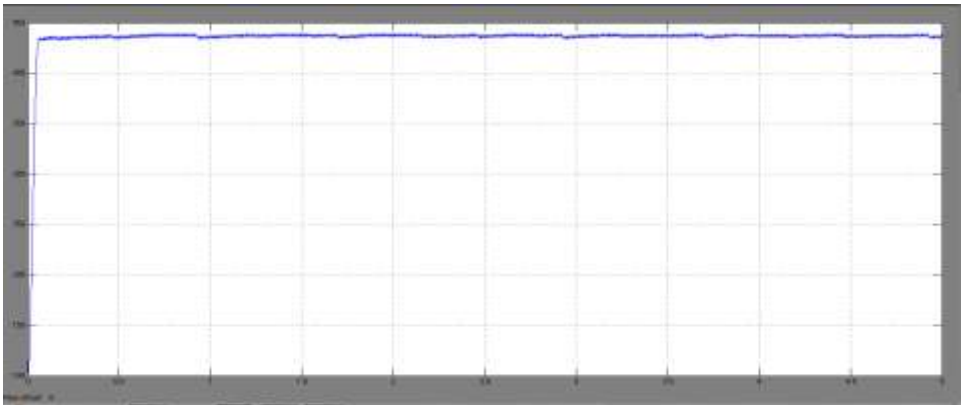
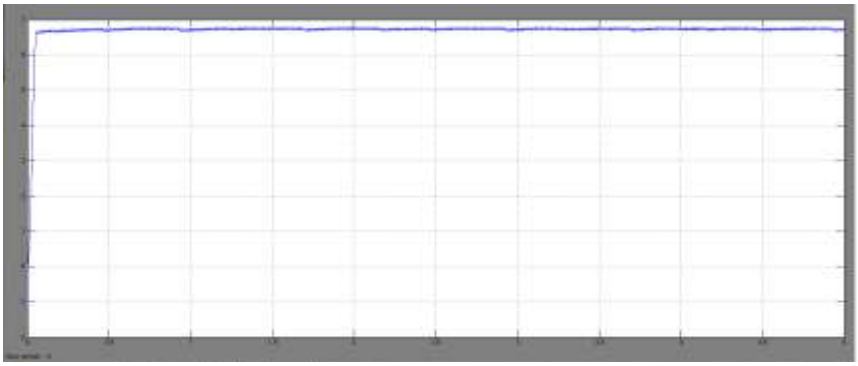


Fig.9. Output current of Proposed Circuit



The simulation is also done for the conventional circuit the result is shown in following fig 10,11. From the comparison the phase difference of the proposed circuit is reduced and the proposed circuit PF is increased to the value of 0.975.

Fig 10. Input current and input voltage for conventional circuit

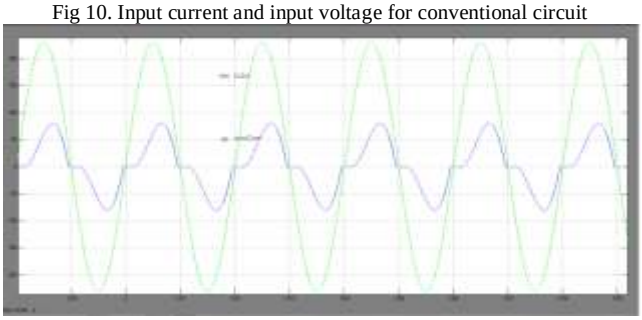


Fig.11. Output Voltage of conventional circuit

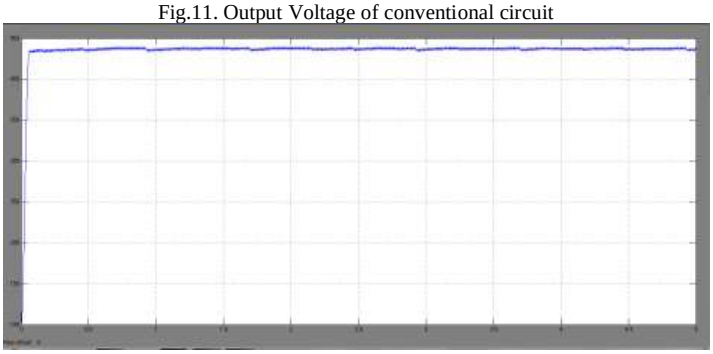
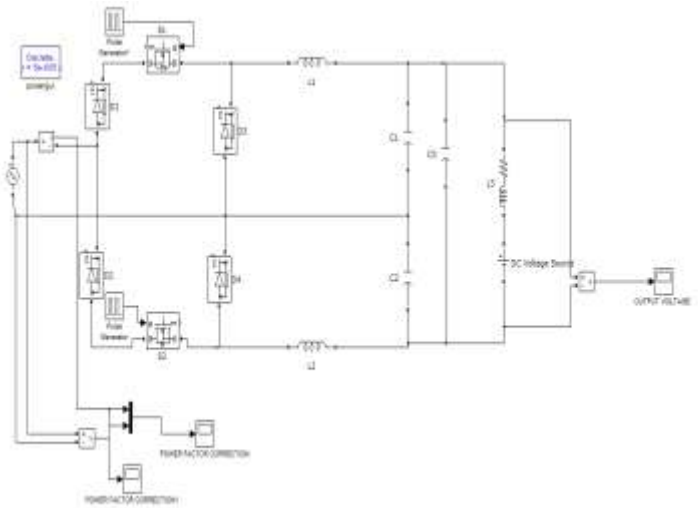


Fig 12.conventional circuit



The conventional circuit is shown in fig 12. By comparing with the proportional circuit the phase difference is decreased which also reduces the THD value. Also the power factor is increased to high value.

V. Conclusion

This proposed circuit will introduces a new concept of bridgeless PFC rectifier with boost converter that substantially improves the efficiency at low line. Firstly the proposed circuit doubles the rectifier output voltage, which extends useable energy after a dropout of the line voltage. Also it reduces the losses through the reduction of input diodes. Moreover by eliminating input bridge diodes, efficiency is further improved. Secondly the boost converter is combined with this circuit to maximize the output voltage with improved PF. Finally, the proposed circuit improves the power factor and efficiencies, also maximizes the output with reduced losses.

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