A Review of techniques used in Lateral Insulated Gate Bipolar Transistor (LIGBT)

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ABSTRACT: *The huge demand for high voltage, high current power devices on Silicon on Chip (SoC) has led to the development of Lateral Insulated Gate Bipolar Transistor (Lateral IGBT/ LIGBT), touted as the best candidate to serve these two purposes. This paper is the first to review the research works on techniques used in LIGBTs published till now. The LIGBTs are categorized into four types based on different technologies applied, mainly junction isolation (JI), silicon on insulator (SOI), partial SOI (PSOI) and membrane, and ten varieties based on their device mechanisms, such as reverse conducting, trench gate and super junction.*

Keywords- *A SoC, LIGBT, JI, SOI, PSOI, Membrane*

I. Introduction

The power semiconductor industry has grown steadily in the past two decades, from $2.7 billion in 1992 to an expected $16.3-billion annual sales volume in 2015, due to the rapid proliferation of power electronics in many fields such as telecommunications, automotive engineering, new renewable energy systems and energy conversion applications. A five-year forecast by IC Insights predicts that sales of LIGBTs are expected to increase by a CAGR (compound annual growth rate) of 7 percent to $3.2 billion between the years of 2011 and 2015.

Since 1985, research efforts have been directed towards developing the IGBT in integration mode. The LIGBT is a promising device for power ICs due to its combination of high input impedance of the MOS gate and the conductivity modulation effect of the drift region. Similar to the discrete IGBT, the conductivity modulation effect allows LIGBT to have a low voltage drop (V_{ON}) but high switching loss due to the removal of electron-hole plasma retained in the undepleted drift region. However, irradiation techniques used in discrete IGBTs to reduce carrier lifetime are not suitable as they adversely affect the CMOS devices in power integrated circuit (PIC) [1], [2]. Various approaches in designing the best device layout for optimal trade-off between VON and turn-off losses are readily available in literature. This paper reviews the various approaches and identifies their strengths and weaknesses, thereby providing possible directions for future research.

II. Device concept of LIGBT

The LIGBT is essentially a combination of a BJT, which provides a high current handling capability, and a MOSFET, which gives a high-impedance voltage control over the bipolar base current. LIGBTs are being assessed against each other on their V_{ON} versus turn off losses (or turn off times, or switching losses). Other electrical parameters such as breakdown voltage (BV), saturation current density, static and dynamic latch up, forward biased, reverse biased and short-circuit safe operating areas (FBSOA, RBSOA and SCSOA) as well as temperature coefficient are also important in determining the application range of a particular LIGBT. Fig. 1 shows a schematic cross section of a conventional LIGBT that is fabricated on a p- substrate with its equivalent circuit. The thick n- drift region can be formed by implantation or epitaxial growth process. The source and body pick up are butted together. The source is also known as the cathode or the emitter while the anode is also termed as the collector in some other literary works. Solid lines refer to junctions while dotted lines refer to different layers but the same type of doping.
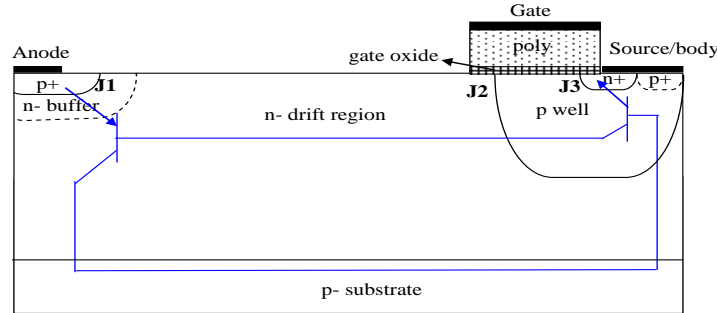
Fig. 1. Schematic cross section of LIGBT and its equivalent circuit.

2.1. On-state and V_{ON}

The current cannot flow if a voltage applied to the anode with respect to the source is less than the voltage required to turn on junction J1 (normally around 0.7V, varies slightly depending on the p+ anode and n- buffer volume concentration) even if the gate is higher than the threshold voltage (V_T). When a positive gate voltage equal or larger than V_T is applied with respect to the source, an inversion channel is formed that connects the body to the n- drift region. This creates the base current of the lateral pnp transistor in the LIGBT structure. If a positive voltage is applied between the anode and source, most of the voltage drops across junction J1, until the junction becomes forward biased. After junction J1 turns on, there is an injection of holes (minority carriers in the case of n- type LIGBT) from both the anode and substrate into the n- drift region leading to conductivity modulation. Part of the holes will flow to the inversion channel, collected and recombined with the electrons in the source while another part of the holes will flow to the p- substrate and collected by the body pick up terminal. This contributes to the "superlinear" region in the IV characteristic of LIGBT as shown in Fig. 2. The current increases much faster than the normal MOSFET due to this modulated drift region. However, if the hole current flowing towards the body is high enough to cause a voltage drop larger than the turn on voltage of junction J3, then latch up may occur in the LIGBT.
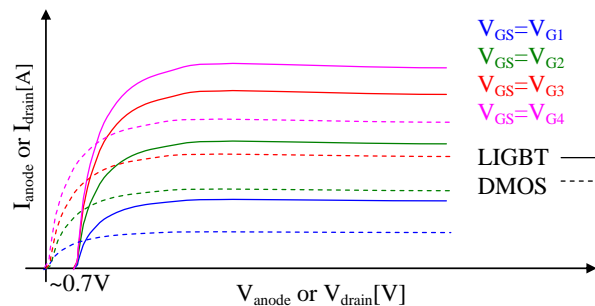

Fig. 2. Typical IV characteristic of LIGBT and MOSFET.

Similar to the MOSFET, the current starts to saturate after channel pinch-off. The total current would thus be equal to the sum of the electron current flowing through the MOSFET part and the hole current flowing through the p well to the source/body terminal. The IGBT V_{ON} can be calculated as per equation 1 [3], whereby V_{J1} refers to the turn on voltage of junction J1, A being the device area, J_{AK} the operating current density and α_{PNP} the inherent pnp transistor gain. R_{ch} and R_{acc} represent the channel resistance and the accumulation region (determined by the overlap distance between the gate and n- drift region) resistance respectively while R_{drift} refers to the non-linear resistance of the n- drift region which in turn depends on the plasma level.

$$V_{ON} = V_{J1} + A \times (1 - \alpha_{pnp}) \times J_{AK} \times (R_{ch} + R_{acc}) + A \times J_{AK} \times R_{drift} \quad (1)$$

During the on-state condition, the n- buffer region aims to control the injection efficiency of holes from the anode. The higher the concentration of the n- buffer region, the fewer the holes that can be injected into the n- drift region as most of them will be recombined in the n- buffer region, thus yielding a lower switching loss but higher V_{ON}.

2.2. Off-state and BV

During the off-state condition, the anode is biased with high reversed voltage and the BV is mainly supported by the junction between n- drift and p well, J2. Similar to the MOSFET, a greater uniformity of the electric field distribution will give a higher BV. To achieve a high BV, the n- drift region must be doped low enough to allow depletion which increases the specific on resistance (R_{dson}) of the device. A higher R_{dson} means

a higher V_{ON}. RESURF [4] is the main technology used in both the MOSFET and LIGBT for the purpose of obtaining a high BV without sacrificing too much R_{dson}. In the LIGBT, the n- buffer region which controls injection efficiency during the on-state condition also helps to terminate the depletion region within the n- buffer region during the off-state condition to avoid punch-through BV.

2.3. Turn off and Switching Loss

To characterize the switching loss of the LIGBT, an example of an inductive switching circuit as shown in Fig. 3 is used to measure the turn off time of the LIGBT. Fig. 4 shows a typical switching waveform of the LIGBT.

Once the gate voltage of the LIGBT becomes lower than V_T, the channel ceases. The anode voltage starts to increase as depicted in (a), Fig. 4. The current remains constant initially due to the nature of the inductor which tends to maintain the current. However, as the voltage reaches the rail voltage, the diode starts to be forward biased and takes over the current from the inductor. The current now drops quickly as shown in (b) due to removal of the electron current at the source terminal. This is followed by a further gradual decrease of the current (c), governed by the charge stored in the n- drift region. The faster the depletion forms, the faster the current drops. A long current tail is normally found (d) due to the charge stored in the undepleted region. The charge stored in this undepleted region can only be removed through a recombination process determined by its carrier lifetime. The implementation of the n- buffer region in the LIGBT helps to reduce the undepleted region thus shortening the recombination tail.
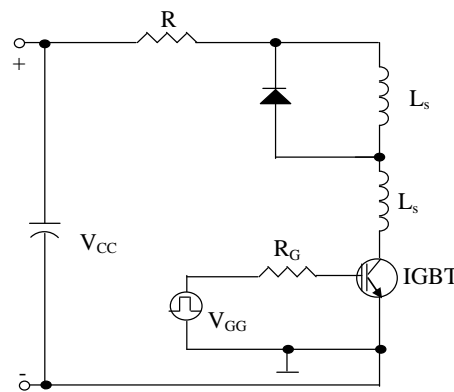
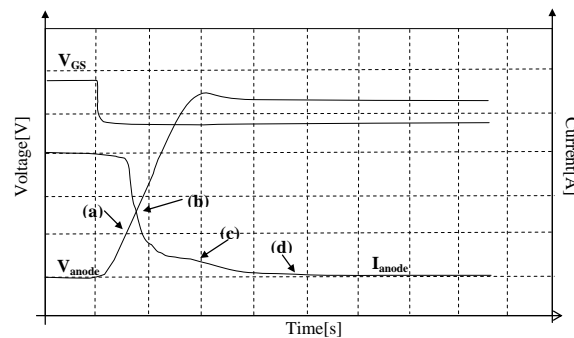

Fig. 3. Example of Inductive Switching Circuit.

Fig. 4. Switching characteristic of LIGBT.

2.4. Temperature Coefficient

One of the favored characteristics of the IGBT as compared to the MOSFET and the BJT is its lower temperature coefficient. The MOSFET normally has a positive temperature coefficient which increases losses as the R_{dson} increases when paralleling the devices in the circuit for high temperature operation while the BJT normally has a negative temperature coefficient which is not suitable for paralleling arrangements as the R_{dson} decreases and may heat up the chip very fast and lead to current imbalance. The positive feedback will lead to further thermal runaway and damage the chip in the end. The temperature characteristic of the LIGBT is much more complex as it is a combined structure of the MOSFET and the BJT. Generally, at low current densities, it is the bipolar portion which dictates the temperature behavior; and at high current densities, it is the channel that determines the electrical performance. With the rise of temperature, the effective intrinsic concentration also increases, leading to a reduction in the energy barrier across junction J1. Thus, the voltage required to turn on junction J1 is also lower. At the same time, the channel resistance is increased due to mobility degradation while

the pnp gain is increased due to reduced barrier across junction J1, which further modulates the drift region. These two effects counter each other, so at a low current density, the voltage drop across junction J1 and reduction of drift resistance due to a higher pnp gain will dominate and result in a negative temperature coefficient while at a higher current density, the channel mobility degradation will dominate and result in a positive temperature coefficient. So far, there are no benchmark values for LIGBT temperature coefficients yet. An LIGBT with a mild positive temperature coefficient seems to be more favored in most applications as it allows paralleling. Fig. 5 shows an example of the temperature behavior of the LIGBT versus Lateral DMOS (LDMOS) in the low voltage region.
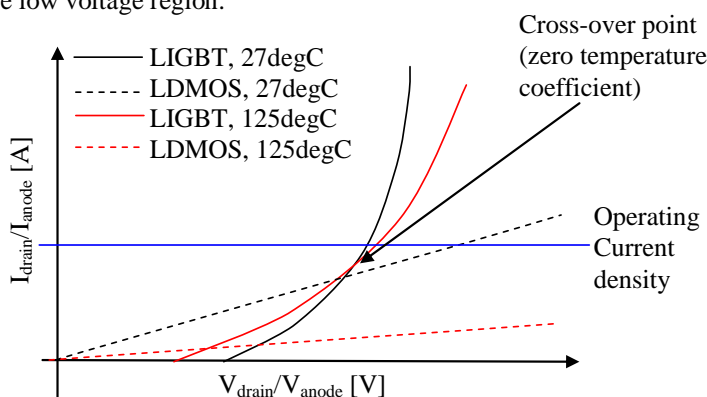

Fig. 5. Temperature behavior of LIGBT vs LDMOS in low voltage region.

2.5. Static and Dynamic Latch up
Due to the inherent parasitic npn composed of n+ source, p well and n- drift, in addition to pnp bipolar discussed above, the parasitic thyristor is formed. Therefore, the LIGBT has always suffered from latch up, either static or dynamic. Latch up occurs if junction J3 is being forward biased when the hole current that flows beneath the source towards the body pick up develops a voltage drop of around 0.6V across the p well lateral resistor thereby turning on the parasitic npn transistor. This is later followed by the injection of electrons straight from the source to the n- drift region. The npn together with pnp will thus form a thyristor feedback, causing a latch up of the LIGBT. The phenomenon is more severe at higher temperatures as the resistance across junction J3 is reduced. A dynamic latch up can also occur during switching, especially under inductive condition. When the gate voltage is below V_T, the electron current is cut off and the hole current can momentarily spike due to the tendency of inductors in series to maintain the current. In other words, at this moment, the voltage drop across junction J3 can increase significantly compared to its on-state level. The common methods used to suppress earlier latch up are by keeping the p well resistance as low as possible or by diverting the holes away from beneath the source. A lower p well resistance allows for a lower voltage drop generated across the p well barrier, assuming the same amount of hole current flowing through, thus increasing the latch-up voltage. Diverting the hole current away from beneath the source also reduces the voltage drop generated, thereby leading to a higher latch-up voltage.

2.6. Safe Operating Area, SOA
The SOA of LIGBT can be divided into three categories, forward-biased SOA (FBSOA), reverse-biased SOA (RBSOA) and short-circuit SOA (SCSOA). FBSOA indicates the maximum voltage that the device can sustain without failing when the anode current is saturated. The FBSOA can be limited by avalanche breakdown, static latch up or thermal breakdown. RBSOA shows the safe operating area during turn off when the gate bias switches from a positive value to zero or a negative value, resulting in high voltage and hole current transport. RBSOA is limited by avalanche breakdown and dynamic latch up. SCSOA refers to the safe operating area for the device under fault condition during load shorts that cause excessive current and high voltage which simultaneously stress the device.

III.   Literature review of techniques used in LIGBT
The history of IGBT was very well reviewed by Udrea in the year 2009 [3]. The first IGBT was patented as early as 1968 [5]. In 1979 and 1980, there were some more publications [6]-[13] related to the invention of IGBT with different design concepts. Generally, there are few main categories of discrete IGBTs [14], some examples of which are DMOS IGBT [15][16], trench IGBT [17]-[20], soft punch through IGBT [21], injection enhanced insulated gate bipolar transistor [22],[23], carrier stored gate bipolar transistor [24], high-conductivity IGBT [25] and super junction bipolar transistor [26][27]. In contrast to discrete IGBTs, the integrated IGBT has complementary metal-oxide-semiconductor (CMOS) compatibility and hence is the

favourite for PICs or smart power. In the 90s, research and development focused in improving the LIGBT performance. Although the use of irradiation to significantly reduce carrier lifetime is possible for PICs, this adds extra costs due to the additional procedure and may affect the CMOS process, too. Consequently, significant efforts have been put into the optimization of LIGBT structures. Generally, there are four main technologies employed for LIGBTs; (A) junction isolation (JI) which is based on a RESURF effect and formed on a silicon substrate; (B) silicon on insulator (SOI) with dielectric isolation (DI) which is more effective than JI; (C) partial SOI (PSOI) which is further improved from SOI; and (D) membrane that may use silicon or SOI wafer. Table 1 shows the LIGBTs surveyed in this paper, categorized by design and technology used.

Type	Technology			
	JI	SOI	PSOI	membrane
conventional	yes	yes	yes	yes
buried layer, sinker, double buried layer	yes			
hole diverter or bypass structure	yes	yes		
reverse conducting, shorted anode design	yes	yes		
reverse conducting, double gate design	yes	yes		
reverse conducting, hybrid design		yes		
multi Channel	yes	yes		
trench Gate	yes	yes		
super Junction			yes	yes
PIGBT	yes			

Table 1. Categories of LIGBT

3.1 JI LIGBT
3.1.1 Conventional LIGBT with buried layer, sinker and hole diverter

The earliest paper that could be found discussing the conventional LIGBT was published in the year 1985 [28]. It demonstrated three techniques; incorporation of p-epi layer, incorporation of p sinker and lastly, incorporation of combination of p sinker together with p buried layer to improve the latching current of JI LIGBT. Fig. 6 shows examples of the different LIGBTs that incorporated (a) p type buried layer and (b) p sinker and hole diverter design.
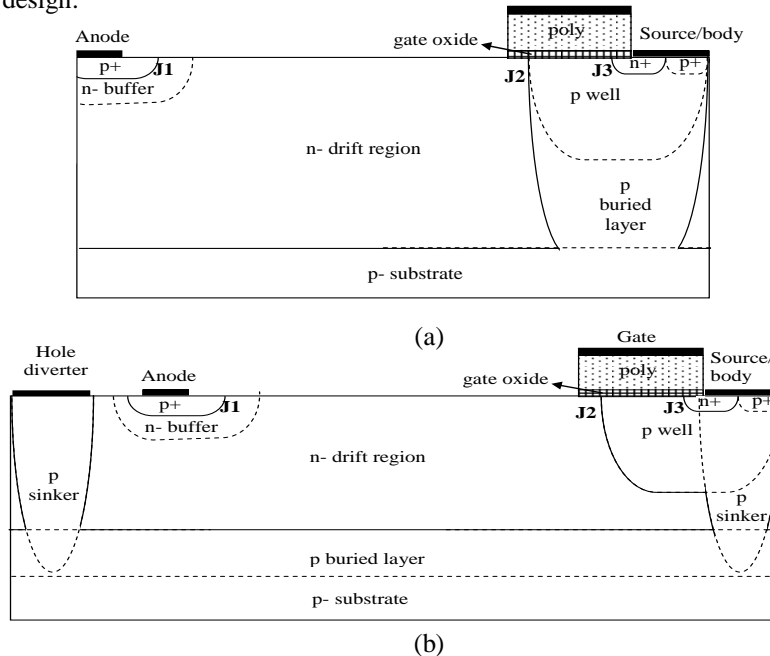

(a)

(b)

Fig. 6. Schematic cross section of LIGBT with (a) p type buried layer and (b) p sinker and hole diverter design.

Among them, the most effective method was by using a p buried layer located under the p well to divert lateral holes, which caused the device to current-limit instead of latching. However, a substantial penalty in V_{ON} was paid. Later in 1986, the steady-state characteristic of the LIGBT was well studied and analyzed [29]. These techniques were further evaluated for 75V to 80V LIGBTs mostly used as power switches, either by combination of p sinker or isolation with p buried layer [30]-[32]. The incorporation of p buried layer and p

sinker not only helped to reduce shunt resistance beneath the source but also helped to divert the holes to a low resistive path (p buried layer), drawing hole current away from beneath the source.

A more advanced structure implemented in 80V smart power technology as illustrated in Fig. 7 incorporating double buried layers and sinkers was published in 2006 [33]-[35]. The new structure incorporated an n- tub that comprised n buried layer sandwiched between the p- substrate and p buried layer, and n sinker which surrounded the active device to further suppress the substrate current. The floating n-tub would follow the potential of the source during the off-state condition. To avoid premature BV, the n buried layer towards p-substrate BV must be higher than internal device BV. During the on-state condition, the potential of n-tub would follow the potential of the anode as both the n- drift region and p buried layer were fully flooded with electrons and holes due to conductivity modulation. The n-tub successfully isolated the internal device from the p-substrate and prohibited the injection of holes from it, resulting in a negligible substrate current, wider SOA and faster switching. The n-tub also enabled the device to be used as a high side switch since the p- substrate can now be biased at high potential. Unlike the previous approach shown in Fig. 6, the hole diverter design applied in Fig. 7 did not add any extra area to the device. Although the application of buried layers, sinkers and hole diverter could help to improve the latch-up, the process became more complex and expensive as it involved epitaxial growth process and complicated sinker formation.
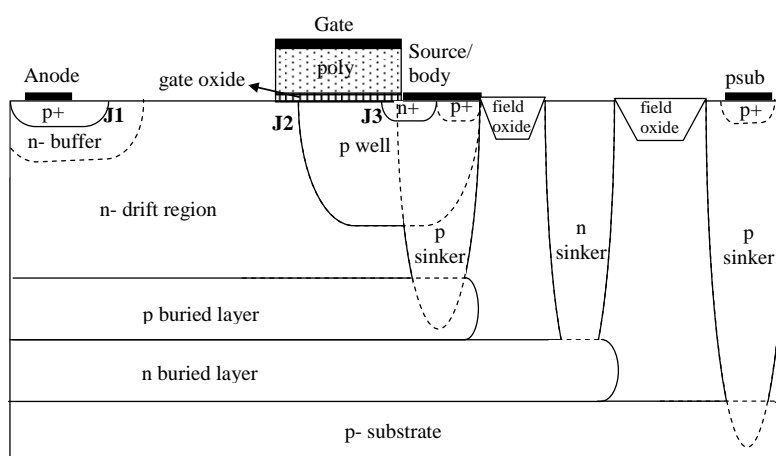
Fig. 7. Schematic cross section of LIGBT with double buried layers and sinkers design.

3.1.2. Reverse conducting (RC) LIGBT

A conventional LIGBT always suffers from high switching loss as the charge tend to store deeply in the un-depleted p- substrate which can only be removed through recombination process. To overcome this, many research efforts had been focused on anode layout variations aiming to provide extra extraction path for the minority carriers during turn off. However, they ended up with negative differential resistance (NDR) regime in output characteristic very similar to that of the non-optimized discrete RC IGBT. The initial purpose of the discrete RC IGBT was actually to provide an anti-parallel diode when reverse biased. However, a 'snapback like' behavior happened in its output characteristic [36] [37] and it led to lots of efforts trying to get rid of this undesired phenomenon. Due to this similar characteristic, LIGBTs with current conducts before anode junction turn on are grouped as RC IGBTs in this review.

3.1.2.1. Shorted-anode LIGBT (SA-LIGBT)

SA-LIGBT was proposed in 1985 [38] and further developed [39]-[41]. Fig. 8 shows a schematic cross section of a basic SA-LIGBT which had an extra n+ region placed next to the p+ region in the anode and shorted by a metal contact. The p+ region was responsible for conductivity modulation of the drift region while the n+ region provided an electron extraction path during device turned off which later helped in reducing the switching loss. However, all SA-LIGBTs exhibited NDR regime as shown in Fig. 9 which could cause undesirable oscillation and instability in switching. The NDR regime basically arose from two different conduction mechanisms that were responsible for current flow in the device. These conduction mechanisms referred to minority carrier injection coupled with majority carrier flow.
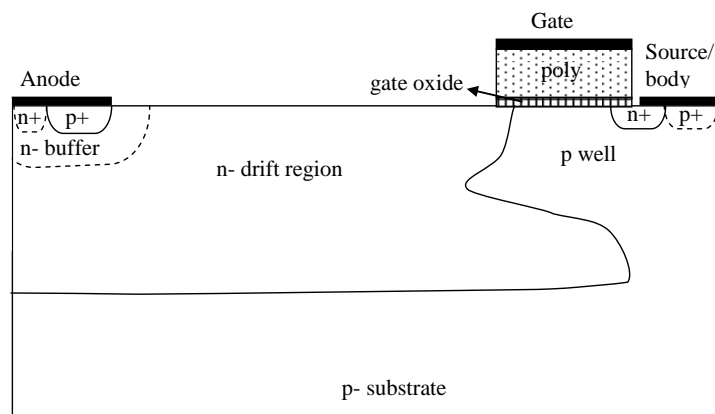
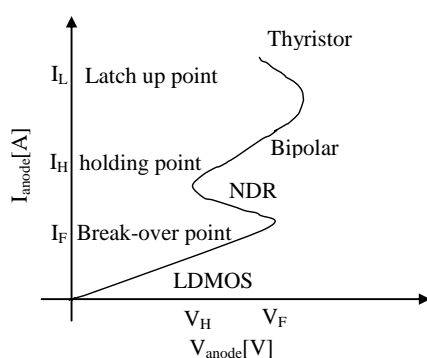Fig.8.   Schematic cross section of SA-LIGBT.

Fig. 9. Typical IV characteristic of SA-LIGBT.

As shown in Fig. 9, in Lateral DMOS (LDMOS) region, since the injection of holes from p+ anode was negligible as compared to background doping, no conductivity modulation took place. In this regime, the conduction was only contributed by the LDMOS part where the electrons were emitted from the source and collected by the n+ region in the anode area. As the anode forward voltage increased, the amount of injected holes also increased beyond the background doping level, indicating the onset of conductivity modulation. At the break-over point, the injected hole concentration exceeded the local background doping level but only within two small, localized regions. Before termination of NDR region, the p+ anode actually kept injecting a significant number of holes into the n- drift region. Existence of these excess holes modulated the n- drift region which thus reduced the voltage across the n- drift region. This was a regenerative process since the smaller voltage drop across the drift region would again resulted in stronger forward bias of the anode junction. Thus, the current increased as more holes were injected whereas the total voltage decreased as n- drift region resistance was reduced further. The end of the NDR region occurred when voltage drop due to intrinsic drift region resistance could not be reduced further. The gradient of SA-LIGBT IV curve would thus approach the conventional LIGBT due to a voltage drop across the parallel resistance and lower modulation of the drift region. To suppress NDR, the anode needed to be made very long to allow reasonable V_{ON} at the expense of switching speed and device area. However, NDR could not be fully eliminated because of the high conductivity buffer region which was needed to avoid punch through breakdown.

3.1.2.2 Improved SA-LIGBT techniques

Many designs had been tried out based on the SA-LIGBT to overcome NDR phenomenon, such as segmented anode LIGBT[42], npn controlled LIGBT [43] and SA-NPN LIGBT [44] [45]. The segmented anode structure had the p+ region split along the width to include segments of n+ regions which allowed a smaller anode area and faster turn off as compared to the shorted anode structure. However, similar to the SA-LIGBT, it still suffered from NDR and the switching speed was influenced by the location of the n+ region as well as the shallow p+ region. Another variant of the SA-LIGBT was the npn controlled LIGBT which utilized an npn type of anode to achieve faster turn off. This structure finally eliminated the NDR regime but the switching speed was significantly influenced by the location of n+ region in the anode as well as the concentration in the shallow p- type region.

The SA-NPN [44] which was developed initially had not only fully eliminated the NDR regime but also achieved ultrafast and low energy loss performance. The later SA-NPN LIGBT comprising segments of p+ and n+ (n+ region formed within a p- base) along the device width direction as shown in Fig. 10 was proposed in 2005.
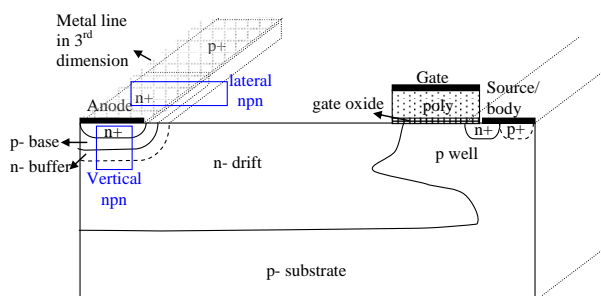

Fig. 10. Schematic cross section of SA-NPN LIGBT.

Different from other segmented structures, the SA-NPN LIGBT offered the additional flexibility of having different characteristics of the LIGBT with varied ratios of segments that determined the V_{ON} vs switching loss trade-off. During the on-state condition, the p- base connected to the p+ acted as a weak injector of holes. Designing the n+ region to be enclosed within the p- base prohibited the electrons from the drift region to reach the n+ region. Consequently, it eliminated the MOSFET-like behavior and also voltage snapback. During switch off, the npn region effectively enabled electrons to be extracted through the p- base anode region. Therefore, increasing the width of the n+/p+ segment with respect to the total width decreased the turn off time but led to an increase of the V_{ON} as a lower injection efficiency meant less modulation of drift. Apart from that, this structure also suffered from a lower BV as compared to the SA-LIGBT (350V vs 410V) [43] due to either vertical punch through breakdown or compensation of n-type dopant by the p- base that affected the balance of RESURF.

Also to overcome the NDR regime in the different anode designs of the LIGBT, double gate structures had been introduced since 1998 [46][47]. The GHI-LIGBT was attempted [46] in 1998, which employed a dual gate and a p+ injector to initiate the hole injection gradually from the anode electrode into the n- drift region. The V_{ON} was reduced by 1V at 200A/cm^2 in comparison with a conventional SA-LIGBT without expense of the device area and switching speed. Fig. 11 shows a schematic cross section of a GHI-LIGBT. During the on-state condition, the electron current injected from the n channel would induce a potential difference in both the n-drift region and n- buffer under the lengthened p+ anode. When the induced potential difference became large enough to forward bias the junction of p+ injector/n- drift, the junction began to inject the holes into the n- drift region from the edge of the p+ injector so that conductivity modulation occurred in the n- drift region. The anode voltage when the hole injection was initiated was much lower than that of the conventional SA-LIGBT as the potential difference in the high resistive n- drift region in the GHI LIGBT was much larger than that of the low resistive n-buffer region in the conventional SA-LIGBT. As the anode voltage further increased, the potential difference in the n- drift region and n- buffer also increased, and the effectively prolonged p+ anode/n-drift junction was gradually forward biased from the corner of the p+ injector to the p+ anode. The NDR regime which was caused by an abrupt conductivity change in the n- drift region of the SA-LIGBT was thus completely eliminated and the V_{ON} was also reduced due to the higher injection efficiency in the GHI-LIGBT.
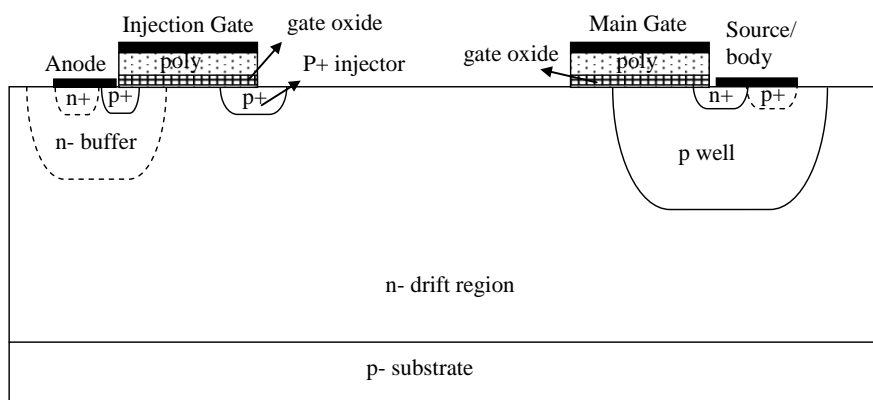

Fig. 11. Schematic cross section of GHI-LIGBT.

Another famous dual gate structure was the DGILET which was based on the concept of inversion layer injection (ILI) [47]. The DGILET had a structure resembling an SA-LIGBT at the anode and source ends except for the presence of a second gate at the anode as shown in Fig. 12. The main difference between the DGILET and the GHI-LIGBT was only the existence of a p+ injector in the latter. Compared to the GHI-LIGBT, the DGILET eliminated the NDR regime with a simpler design. Although both of these structures benefited from a low V_{ON} and low switching loss, the requirements to turn on the anode gate (or injection gate) with different timings and control sequences made the gate driving circuit very complicated.
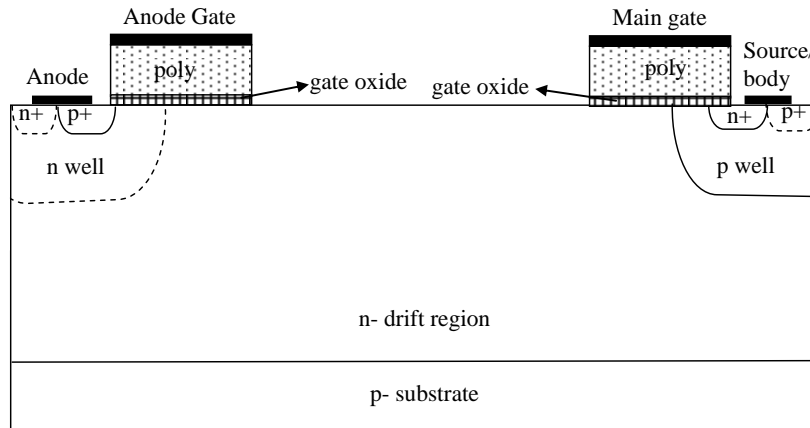
Fig. 12. Schematic cross section of DGILET.

3.1.3. Inversion layer bipolar transistor (ILBT)
The ILBT [48] also applied the concept of inversion layer injection (ILI) [49]. Although it was labeled as a bipolar transistor, it was actually operated as an LIGBT. Fig. 13 shows a schematic cross section of the ILBT. Different from the conventional LIGBT, the p-epi/n- drift junction became forward biased as the hole drift current flowed through the lightly doped p-epi. This phenomenon was equivalent to the base push-out scenario which later led to the spread of electrons into the p-epi. Since the potential difference of the upper part of n- drift/p- epi was similar to the inversion layer/p-epi, the inversion layer/p-epi junction was turned on at the same time leading to a heavily modulated p-epi region. Simulation results showed a BV of 150V could be supported by the p-epi/n-well junction. The kink appeared in the measured output characteristic. Although this structure was favorable for a lower V_{ON} as compared to the conventional LIGBT, the p-epi thickness must be thick enough to avoid vertical punch-through in its vertical thyristor part (p+/n- drift/p- epi/n- substrate) yet thin enough to prevent deep storage of plasma which was hard to be removed during switch off. Besides, the structure proposed here used the n- substrate and involved thick epitaxial growth process which was less flexible and also less economic.
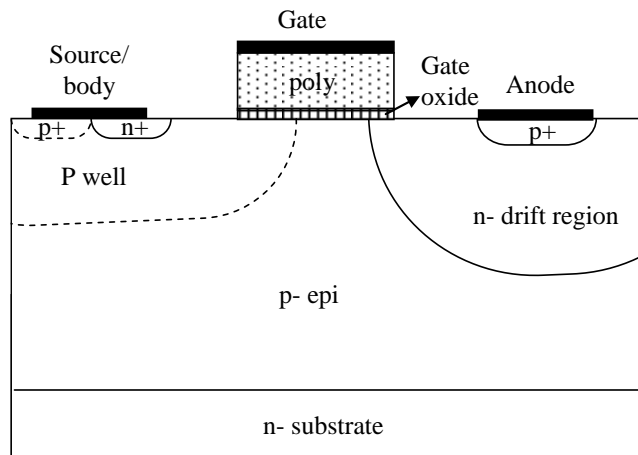
Fig. 13. Schematic cross section of ILBT.

3.1.4. Lateral trench-gate bipolar transistor (LTGBT)

An innovative idea, the LTGBT was proposed in 1999 to improve the latch-up current density [50] by reducing the hole current flowing beneath the source. This structure incorporated a trench-gate in which the locations of the channel and source in a conventional LIGBT were interchanged. This arrangement successfully increased the static and dynamic latch-up current densities by 2.3 and 4.2 times respectively. Fig.14 illustrates a schematic cross section of the LTGBT. The existence of the p well facilitated the collection of holes by the p+ in contact with the source so that the holes had less tendency to flow beneath the n+ source. Simulation also showed that the vertical channel depletion region could help to divert the holes away from beneath the n+ source during the on-state condition. To achieve optimal latch up characteristics, the n effective length should be made as short as possible and the p+ junction depth should be made deeper than the n+ for better pick up of holes. To obtain minimum n effective length which was limited by lithography, the n+ and p+ were designed to overlap in the source region. Experimental results showed no latch up if an n effective length of 2µm was being used at the expense of 0.8V increase in the V_T. In addition to the increase in V_T, the process was also more complex as compared to the conventional LIGBT since deep trench process was involved.
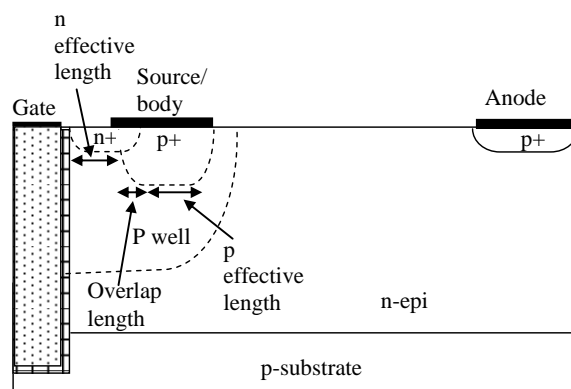

Fig. 14. Schematic cross section of LIGBT.

3.2 SOI LIGBT

There are a number of weaknesses presented in almost all JI LIGBTs, such as substrate current surges during switching transient, static and dynamic interaction between devices [51] [52] as well as higher switching loss as the plasma tends to store in deep substrate which is hard to remove. Compared to JI, SOI provides superior isolation with low leakage current. However, SOI devices may suffer from severe self-heating and worse, latch-up. A paper comparing the JI and SOI LIGBTs had been published in early 1992 [53], showing similar BVs in both JI and SOI LIGBTs using the Reduced Surface Field (RESURF) principle and a higher V_{ON} but one order of magnitude faster in switching speed in the SOI LIGBT as compared to the JI LIGBT. The higher V_{ON} in the SOI LIGBT was because there was only lateral pnp contribution during the on-state condition. In the JI LIGBT, the drift region (normally the epi layer) was always thin leading to the existence of a narrow base vertical pnp which had a considerable gain and also contributed during the on-state condition. Therefore, for the same silicon thickness, SOI LIGBTs always had a lower current density than JI LIGBTs. With the increase of SOI thickness, the SOI LIGBT would have V_{ON} approaching that of the JI LIGBT as the transistor area for the lateral bipolar transistor was also larger. The turn-off time was faster in the SOI LIGBT as the plasma had the tendency to store deeply in the substrate due to a parasitic vertical bipolar which in the SOI LIGBT, was absent.

Since JI LIGBTs were well developed before the emergence of the SOI LIGBT, many concepts used previously in the JI LIGBT, such as dual anode design [54], lateral trench with interchanged channel and source design [55] [56], and p sinker and buried p layer [57]-[60] for hole divergence, were also similarly evaluated on SOI. Apart from that, there are some more new concepts being developed on the SOI LIGBT as discussed in the following subsections.

3.2.1   Multi-channel LIGBT

A new device known as the multi channel LIGBT was published in 1997 [61] to tackle the common problem of low current turn off capability suffered by conventional LIGBTs. This new structure comprised a plural number of parallel polysilicon gates and resultant plural number of channels. As compared to the conventional LIGBT, the Multi-channel LIGBT was able to achieve a larger current density due to enhanced electron injection contributed by a second gate. In addition, FBSOA was also improved as the hole current could be removed through the two p wells during conduction state thus increasing the latch-up current density. To minimize the switching loss, a new anode structure which included a shallow p- layer was implemented to

control the hole injection. However, this reduced the current density due to lower injection efficiency at the anode. Thus, to further increase the current density, the improved structure as shown in Fig. 15 was suggested and proven to increase the current density by having a second gate shared by two neighboring LIGBTs with BVs from 320V to 520V.
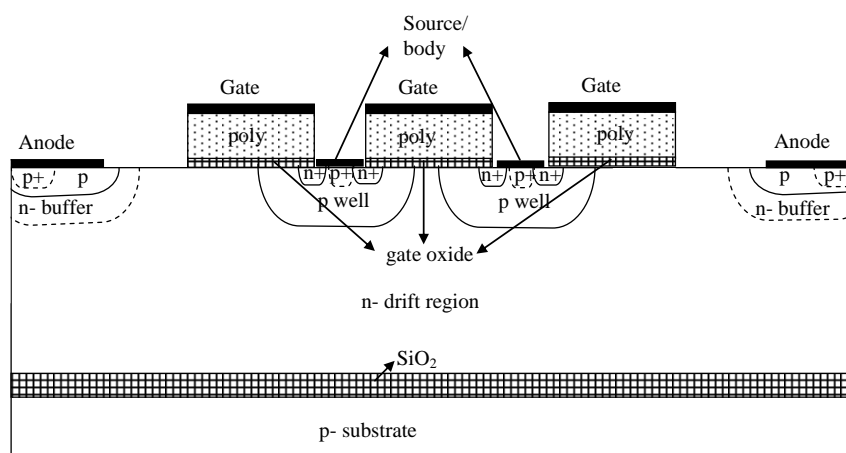

Fig. 15. Schematic cross section of improved multi-channel LIGBT.

3.2.2. LIGBT on ultra thin SOI

Previous studies on SOI power devices [62]-[64] were limited to thick (>10μm) SOI layers leading to complicated trench etching and refilling, which had to be used for lateral isolation. However, device isolation and integration into a low power logic device could be simplified if an ultra-thin (<1μm) SOI layer was used. Evaluation findings of the PiN diodes [65] and the LDMOS [66] which achieved BV of 700V were later reported. This concept had been further extended into the LIGBT [67] with the purpose of getting high BV, fast switching [68]-[70] and low V_{ON}. However, experimental results showed that the SOI layer thickness for the LIGBT became the limiting factor as it controlled the amount of stored carriers in the drift region. A too thin SOI rendered the conductivity modulation ineffective and led to a high V_{ON} while a thick SOI could cause difficulty in the formation of a linearly graded drift region for RESURF, leading to a lower BV.

3.2.3. RC Hybrid LDMOS/LIGBT devices on ultra-thin SOI

Following the development of the LIGBT on ultra-thin SOI, a hybrid LDMOS/LIGBT was later proposed for 500V to 600V power half-bridge source-follower applications [71]. The hybrid construction consisted of parallel segments of bipolar (LIGBT construction) and unipolar conduction (LDMOS construction). During the on-state condition in high-side operation, the LDMOS segment suffered from the pinching effect of depletion from the BOX/substrate MOS capacitor. However, in the LIGBT, the hole current can flow through the inverted drift at the BOX/SOI interface. This extra hole current acted as a screen from the depletion effect and reduced the pinching effect in the LIGBT. By playing with the ratio of LIGBT to LDMOS area, a good trade-off between the saturation current could be achieved. The proposed structure also could be utilized as a high-side power device without any degradation in switching and latch up under high side condition. The enhanced current handling as well as fast internal body diode in LDMOS segments also allowed a reduction in IC area by 25% to 50%, depending on application specifications with respect to peak current and R_{dson}, which were always a trade off. In addition, the hybrid structure under high side operation exhibited a negligible turn off tail as compared to during low side operation since the entire BOX/SOI interface was inverted at high side and provided an extraction path for the holes during turn off. However, since the hybrid structure was fabricated on ultra-thin SOI, it was difficult to optimize device performance owing to the limited conductive area.

3.2.4 Oxide Trench, Hole Bypassed Gate Configuration LIGBT

In 2005, a new LIGBT [72] structure with an oxide trench in the n- drift region and interchanged arrangement of source and body pick up as shown in Fig. 16 was proposed for smart plasma display panel (PDP) scan driver IC application. The reported device successfully reduced the device pitch to about half of the conventional LIGBT with R_{dson} of 330mΩ.mm2, 200V BV and current density of 1000A/cm^2 with 4V on gate. The oxide trench buried with the polysilicon field plate in voltage sustaining region helped to maintain high BV and shortened the device pitch. The hole bypassed gate configuration [73] [74] with the location of source and body pickup interchanged increased its immunity against latch up. To alleviate premature BV between the p well and n- drift region, a source (emitter) side field plate (EFP) was implemented to shield the lateral electric

field from the anode side [75]. The anode (collector) side field plate (CFP) suppressed the surface depletion at the interface between the oxide trench and anode silicon pillar so as to prevent the n- drift region from reaching the p+ anode during reverse blocking. To further suppress the depletion effect from the substrate, at the same time controlling the conductivity modulation and maintaining better gate oxide integrity (GOI), an arsenic implantation was introduced above the interface between BOX and SOI [76]. Despite the superior performance in BV and R_{dson}, this device seemed to have lower leakage only when the gate was biased with negative voltage. Besides, trench structures made the integration more difficult and the whole process more expensive and complicated.
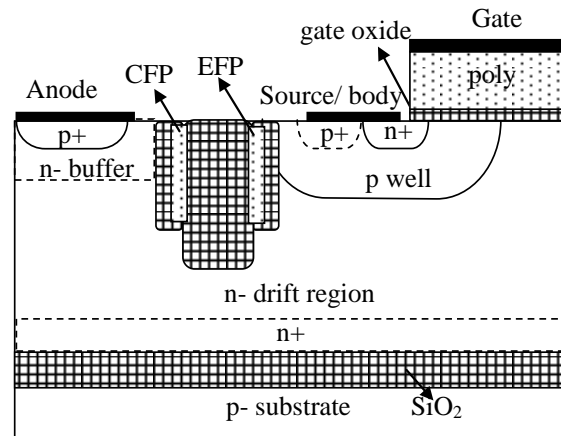

Fig. 16. Schematic cross section of oxide trench, hole bypassed gate configuration LIGBT.

3.2.5. Retrograded channel LIGBT

In 2008, a 200V retrograded channel SOI LIGBT with enhanced SOA [77] as shown in Fig. 17 was published with the same purpose as that of the oxide trench, hole bypassed gate configuration LIGBT. This structure successfully suppressed the latch up without using the expensive and complicated trench process, or buried layer which was formed by either epitaxy or high energy ion implantation, or self-aligned implantation with the n+ source [72] [78]. The main feature of this device was a retrograded doping profile (RDP) under both the channel and source junctions fabricated with an extra one mask, named the RDP mask. In Fig. 17, the LBP was denoted as the space between the RDP mask and the p well mask. The RDP profile not only improved the latch-up immunity by providing a low resistance path under the source and suppressing the parasitic pnp injection efficiency through reducing Gummel number but also helped to scale down the channel length by half of the conventional design as channel punch-through was also being suppressed. Experimental results reported showed dependency of LBP length on the V_T. A maximum LBP length of 0.5μm was needed to ensure the peaks from RDP and p well implantations did not superimpose to allow reasonable V_T values. No latch up was observed in the RDP LIGBT below current density of 1700A/cm^2 in 200ns transmission line pulses (TLP) measurement. However, the mask proximity effect (MPE) during ion implantation [79] needed to be carefully considered when designing the RDP LIGBT. The process margin should also be well controlled to ensure V_T would not be affected.
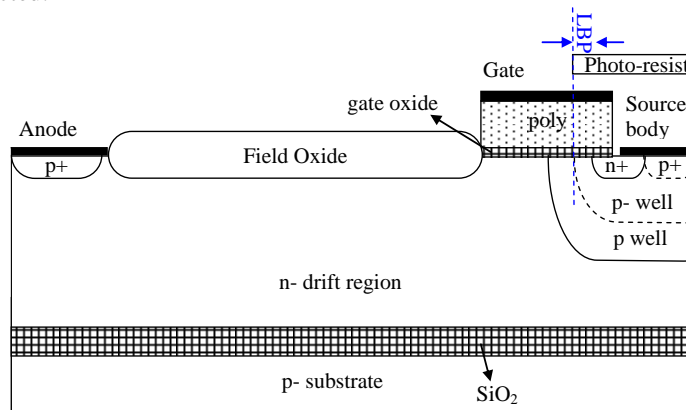

Fig. 17. Schematic cross section of multi-channel RDP LIGBT.

3.2.6. Dummy metal short (DMS) with emitter ballast design in p-type field LIGBT

When compared to n type LIGBTs, there are fewer publications discussing the p type LIGBT. The main reason is that the p type IGBT suffers from latch up more easily as the parasitic bipolar is now npn instead of pnp. The inherent higher mobility of minority carriers as well as the nature of higher gain in npn as compared to pnp structure also leads to more minority carriers in the p type IGBT. However, the p type LIGBT is still important, especially for high-side application when the substrate bias is high. Due to the more active parasitic npn structure embedded in a p type LIGBT, it is theoretically possible to get a pair of equal-sized n type and p type LIGBTs if the device is excellently optimized. In the paper published in 2006 [80], a p type field LIGBT as shown in Fig. 18 was discussed. To suppress the latch up, a DMS structure was used which consisted of n+ and p+ layers shorted via a CoSi2 layer to control the electron injection from the n+ cathode.
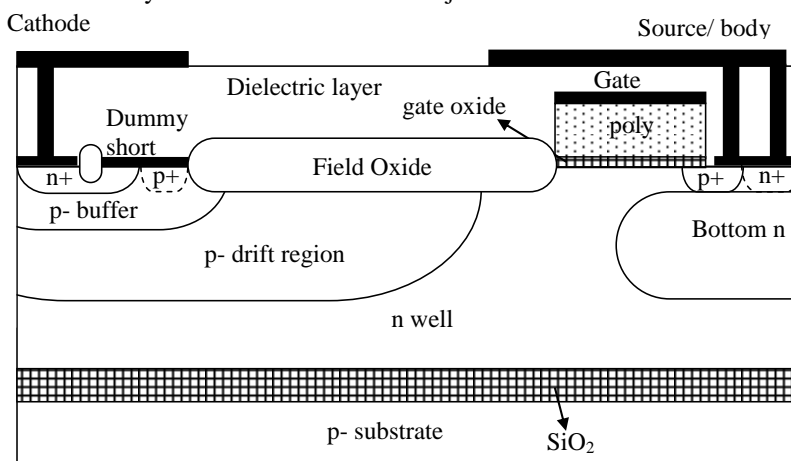

Fig. 18. Schematic cross section of p-type field LIGBT.

3.2.7. Multi-emitter LIGBT with hole barrier layer

Similar to the multi-channel concept, a multi-emitter (multi-source) LIGBT [81] was reported in 2011 for PDP scan driver IC application which applied an extra hole barrier layer to support uniform action of each channel and achieve low V_{ON} of 1.8V at large current density of $760A/cm^2$ and $4000A/cm^2$ saturation current density with 270V BV. Fig. 19 illustrates the schematic cross section of the multi-emitter LIGBT. The function of the n type HBNW layer which enclosed the source region was act as a hole barrier as the holes could recombine more easily in this highly doped n region. In addition, the HBNW layer also helped to reduce the voltage drop difference across the source channels and reduce the JFET effect. This finally brought about greater electron injection from the source and thus increased hole injection from the anode. The weakness of this device was limited BV due to increased impact ionization rate in the multi emitter (multi-source) design, especially at the edge of the multi emitter (multi-source) region if the HBNW dose was more than $4.8e12cm^{-2}$ in order to get a high current density.
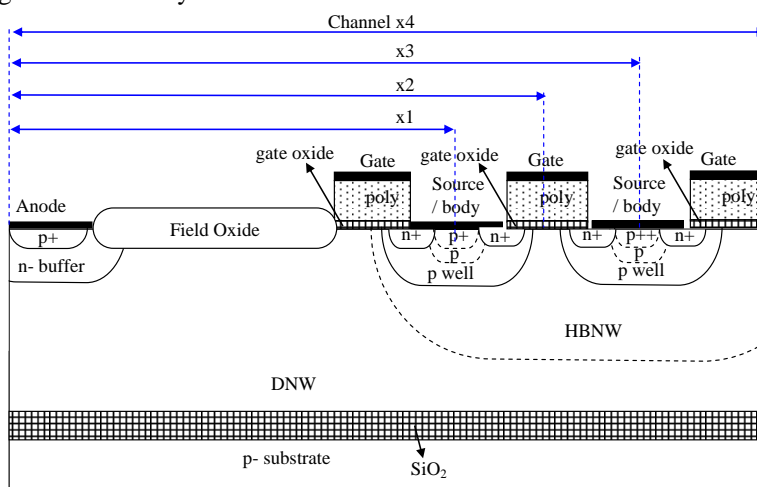

Fig. 19. Example of multi-emitter LIGBT.

3.3. Partial isolation SOI (PSOI) LIGBT

A solution to overcome the weaknesses in SOI devices was later proposed [82] which combined the advantages of SOI and JI technologies, known as PSOI. Unlike the SOI devices, the potential lines were no longer crowded in the n- drift region but extended into the substrate during the off-state condition through the silicon window into the BOX, leading to high BV in PSOI devices. Since the extension of the potential lines into the substrate helped in supporting voltage during the off-state condition, a PSOI device could employ a thinner BOX when compared to an SOI device that always required a thicker oxide to help sustain the voltage. With the silicon window into BOX, heat could be dissipated more efficiently. However, a PSOI structure also had body current generating power and increasing the device temperature. With reduced lattice heat in the PSOI, latch-up immunity could be increased. Compared to JI, the PSOI offered higher switching speed as the current and most of the plasma injection were still confined within the SOI layer.

The first LIGBT investigation based on PSOI technology was reported in 1997 by Udrea [83]. Fig. 20 illustrates the schematic cross section of an LIGBT with PSOI technology, featuring p+ buried layers and deep p well implants to connect the substrate to the source potential. The main principle of this device was to allow potential lines during the off-state condition to be extended from the source side into the p- substrate while preventing plasma injection from the source junction by placing a thin insulating layer underneath the anode. The lowly doped substrate which was electrically connected to the source allowed the depletion region to spread into it and supported part of the voltage, releasing the pressure on the insulating and thin SOI layers.
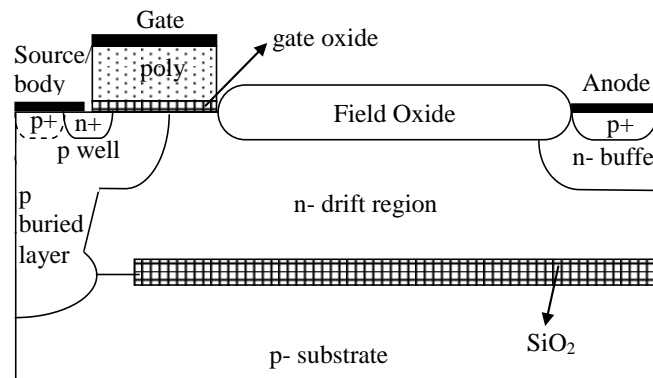

Fig. 20. Schematic cross section of LIGBT based on PSOI technology

Further development of the LIGBT on PSOI was reported later in 2005 [84] which successfully realized the LIGBT structure based on lateral epitaxial growth over oxide (LEGO) process [85]. The resulted device showed a turn-off time of 400ns, BV more than 300V with reduced heating effect when compared to a standard SOI. However, the LEGO technique involved re-crystallization making the process more complex. The location of the hole in the insulating layer had been shifted to below the source side to below the anode side. This change could result in a better distribution of minority carriers (injection of holes also occured from the p- substrate into the n- drift region through the hole in the insulating layer), flowing more to the anode side instead of the source side thus bringing about a faster switching speed.

Developing Lateral Super Junction LIGBTs with BVs ranging from 100V to 400V was proposed later at the end of the year 2010 [86]. The proposed concept was new as compared to prior-art LIGBT, extended from the working LDMOS with lateral super junction built on SOI wafer which employed PSOI concept [87]. First lateral super junction LIGBT showed ideal BV as achieved in vertical super junction LDMOS as well with less than twice the R_{dson}. However, the device is currently limited with its FBSOA and is in the progress of improvement. Fig. 21 shows the schematic cross section of lateral Super Junction LIGBT fabricated on SOI wafer.
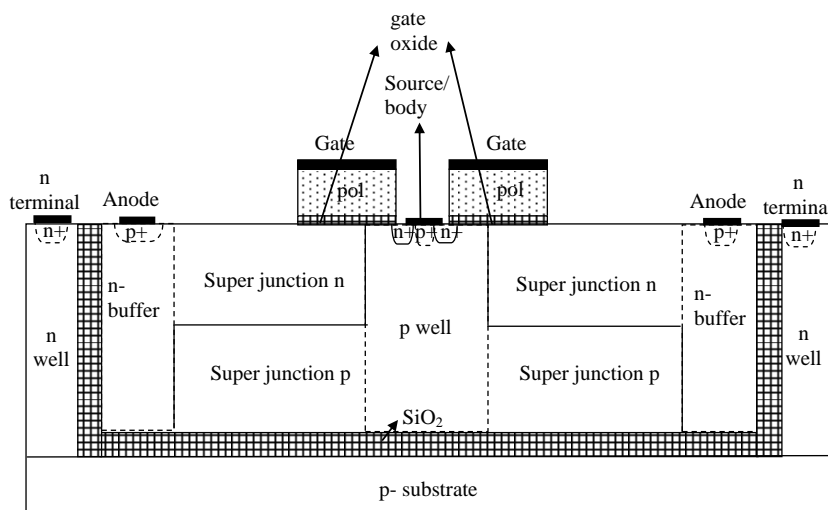
Fig. 21. Schematic cross section of lateral Super Junction LIGBT [86]

3.4. Membrane LIGBTs

Membrane technology with back side etching of the silicon substrate under part of the n- drift region of SOI power devices had been proposed [88] and experimentally reported [89]. As mentioned, most of the time JI LIGBTs were not that successful in ICs due to the poor switching speed and cross-talk with adjacent CMOS blocks via common silicon substrate whereas SOI technology had a number of major drawbacks such as a thicker BOX thickness for effective RESURF. There are more secondary weaknesses in SOI devices such as parasitic back depletion effect in high side configuration, limited speed due to the output capacitance being dominated by anode/substrate capacitance [90] as well as premature breakdown due to hole inversion layer on top of BOX leading to the anode being shorted to the source. The new membrane concept helped in getting high BV as the electrical potential distribution was almost ideal after the removal of silicon under the n- drift region and it also eliminated any possible vertical avalanche breakdown. Virtual absence of anode/substrate capacitance led to increased switching speed as well.

Two LIGBTs (conventional design and super junction design) built on thin membrane were reported in 2005 [91]. The conventional membrane LIGBT built on a thin membrane of 0.25μm achieved a BV more than 700V with higher current density than the super junction membrane LIGBT which exhibited only slightly increased BV due to doping tolerance impact [92][93] as it employed charge compensation techniques that led to virtually ideal square-type electric field distribution in the drift region. The conventional membrane LIGBT reported a record 50ns turn off time, which was much better than prior-art LIGBTs. In membrane technology, the displacement currents were also relatively small as capacitance through the trench underneath the BOX was very small. One drawback in this technology was the reduced thermal conductance of the membrane. To avoid severe self heating, multiple long and narrow membranes were used to allow heat to be dissipated through silicon legs down to the heat sink.

To further improve current capability which was limited by the thickness of silicon membrane, a new LIGBT based on thick membrane was reported [94] that achieved current densities which beat the best of those offered by vertical devices at values greater than 100A/cm^2 and power density of 180W/cm^2 without sacrificing switching speed (lower than 60ns for 1.5μm membranes). A thicker membrane also helped in heat dissipation.

Different from previous membrane LIGBTs built on SOI wafer, the first membrane LIGBT built on bulk wafer was reported in 2009 [95] by the same author after immense and continuing improvements in DRIE tools (old DRIE needed oxide as etch-stop layers). Fig. 22 shows the schematic cross section of the membrane LIGBT on bulk silicon wafer. This structure achieved a higher maximum power density due to better thermal dissipation, more robust operation including unclamped inductive switching, improved SCSOA and no failure after more than 1000 hours of HTRB test. The main challenge in this technology was uniformity in thickness without using BOX as an etch-stop layer.
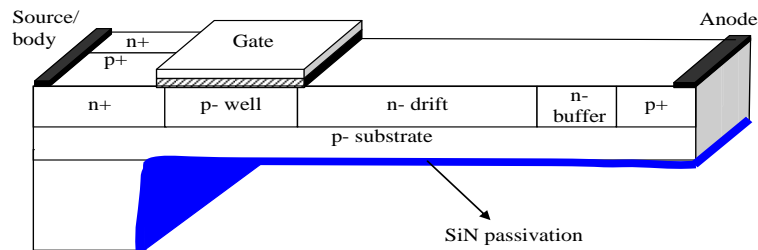
Fig. 22. Membrane LIGBT on bulk CMOS technology.

IV. Conclusion

This paper is the first to cover most of the techniques used in LIGBT devices that were previously published. The concepts of each of the LIGBT devices were reviewed. Their strengths and shortcomings were discussed and summarized so as to provide references for future development studies.

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