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Implementation And Performance Evaluation Of NLC And FCS-MPC Strategies For An MMC-Based Active Power Filter Dedicated To Grid Harmonic Mitigation

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Abstract:
Nonlinear loads introduce harmonic pollution into electrical distribution networks, degrading power quality, increasing losses, and causing equipment malfunction. This paper presents an active power filter based on a Modular Multilevel Converter (MMC) with four submodules per arm (N = 4) and an 800 V DC-link voltage, designed to compensate grid current harmonics caused by nonlinear loads. Two control strategies are studied and compared: Nearest Level Control (NLC) and Finite Control Set Model Predictive Control (FCS-MPC). For FCS-MPC, a voltage-level reduction technique limits the number of admissible switching states to $(N+1)^3$, with the optimal state selected at each sampling instant by minimizing a cost function accounting for the output current tracking error, circulating current deviation, and capacitor voltage imbalance. The MMC model, including arm dynamics and submodule capacitor behavior, is derived and discretized for real-time predictive computation. The proposed scheme is validated in MATLAB/Simulink under identical operating conditions for both strategies. Results show that FCS-MPC clearly outperforms NLC, reducing the THD from 2.32% to 1.04% while also lowering circulating current oscillations and improving capacitor voltage balancing. These findings demonstrate that an MMC-based active filter controlled with FCS-MPC achieves faster dynamics and better steady-state accuracy in harmonic compensation, making it a strong candidate for improving power quality in networks with nonlinear loads.

Keywords: *Modular Multilevel Converter (MMC), Finite Control Set Model Predictive Control (FCS-MPC), submodule capacitor balancing, circulating current suppression, power electronics control, cost function optimization, NearLest Level Control (NLC).*

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I. Introduction

Modular Multilevel Converters (MMCs) have become the reference topology for medium and high-voltage energy conversion. Since their introduction by Lesnicar and Marquardt [5], they have attracted considerable research interest, largely because of their modularity, scalability, fault tolerance, and strong harmonic performance [1]. Their distributed, reconfigurable architecture makes them especially well suited to modern grid infrastructures, which increasingly demand flexible, reliable, and efficient power conversion.

An MMC is built from three-phase legs, each split into upper and lower arms made up of N identical half-bridge submodules (SMs), with each submodule capacitor acting as a distributed energy-storage element. This architecture brings clear advantages, but it also comes at the cost of considerable control complexity: the output AC currents, the inter-phase circulating currents, and the voltage balancing of every submodule capacitor must all be regulated simultaneously [2]. Because these objectives are tightly coupled, and because the number of admissible switching states grows rapidly with the number of submodules, the resulting control problem is far more demanding than for conventional converter topologies [8]. These challenges have motivated nearly two decades of research, which has produced rigorous dynamic models of the MMC along with a range of dedicated control strategies [1], [5], including circulating-current suppression controllers operating at twice the fundamental frequency [6].

Conventional control of Modular Multilevel Converters (MMCs) relies mainly on classical modulation and regulation techniques. One of the most widely adopted is Carrier-Phase-Shifted Pulse Width Modulation (CPS-PWM), which uses several triangular carriers shifted in phase with respect to one another, so that switching losses are evenly distributed across the submodules. This also produces (N+1) output voltage levels per arm and effectively raises the switching frequency, which translates into a noticeable reduction in harmonic distortion. Nearest Level Control (NLC) offers a simpler alternative, and is particularly attractive for converters with a large number of submodules. At each sampling instant, the reference voltage is rounded to the nearest discrete level to determine how many submodules should be inserted, producing a staircase approximation of the sinusoidal waveform.

Finite Control Set Model Predictive Control (FCS-MPC) follows a fundamentally different logic from conventional control schemes. Rather than relying on separate current regulators and modulation stages, it takes advantage of the finite number of switching states available in power converters and directly optimizes a cost function over a short prediction horizon [4], [9]. This predictive, multi-objective formulation allows system constraints and nonlinearities to be handled within a single unified framework, so that current tracking error, circulating current suppression, and submodule capacitor voltage balancing can all be optimized jointly [10], [14].

A practical limitation remains, however: evaluating a large number of admissible switching states in real time imposes a considerable computational burden. Several reduced-complexity formulations have since been proposed to address this issue, notably through voltage-level pre-selection strategies that shrink the search space while preserving solution optimality [13]. More recently, deep learning techniques have been explored to extend the effective prediction horizon of FCS-MPC for MMCs, broadening its applicability and improving its overall control performance [15].

This paper presents the implementation and performance analysis of two control approaches, FCS-MPC and NLC, applied to an MMC-based active power filter. A voltage-level reduction strategy is employed to restrict the search space to $(N+1)^3$ admissible switching states in the FCS-MPC strategy. The performance of the proposed approaches is validated through MATLAB/Simulink simulations under identical operating conditions.

The main contributions of this work can be summarized as follows:

- **Modeling:** A state-space model of the MMC is derived and discretized, accounting for arm inductance dynamics and submodule capacitor behavior.
- **Control design:** An FCS-MPC cost function is designed with weighted penalties on the output current error, the circulating current deviation, and the capacitor voltage imbalance.
- **Complexity reduction:** A voltage-level reduction strategy is used to enumerate the admissible switching states efficiently, keeping the approach computationally feasible for real-time implementation.
- **Validation:** The proposed approach is validated through MATLAB/Simulink simulations and compared with the NLC strategy under equivalent operating conditions.

The remainder of this paper is organized as follows: Section II presents the architecture of the proposed MMC-based shunt active power filter, controlled using either FCS-MPC or NLC, Section III details the simulation setup and results Section IV concludes the paper.

II. Overall Control Architecture Of The Proposed MMC-Based Shunt Active Power Filter, Controlled Using Either FCS-MPC Or NLC.

Fig. 1 shows the general structure of the proposed active filter, built around a Modular Multilevel Converter (MMC). The system is organized around three main blocks: a reference current generator, a control block implemented with either FCS-MPC or NLC and the MMC itself, connected at the Point of Common Coupling (PCC) to compensate for the harmonics produced by the nonlinear load. Working together, these blocks achieve effective harmonic attenuation and a marked improvement in source-current quality.

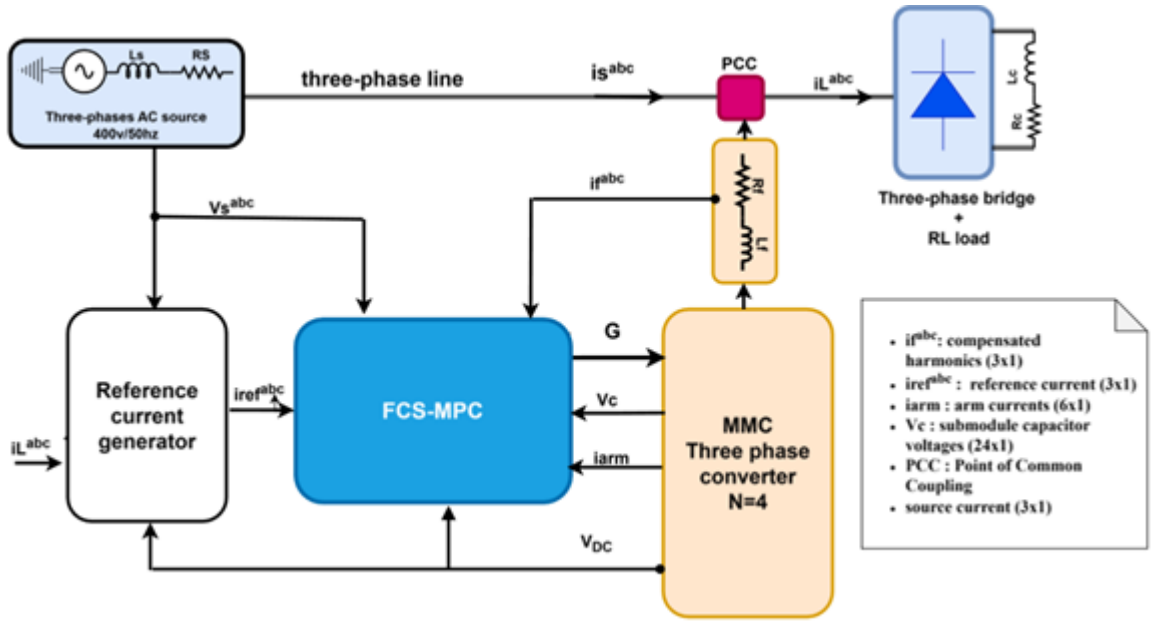

Fig. 1. Block diagram of the FCS-MPC and NLC control strategies applied to an MMC-based shunt active power filter.

A. Converter Topology MMC

1) MMC block architecture (N=4, V_{DC}=800 V)

The three-phase MMC considered in this work is shown schematically in Fig. 3. Each phase leg $j \in \{a,b,c\}$ consists of an upper arm (u) and a lower arm (d), each made up of $N = 4$ half-bridge submodules connected in series with an arm inductance L and an arm resistance R. The DC bus is connected between the positive and negative rails at a voltage $V_{DC} = 800V$. Each submodule k contains a storage capacitor C and two complementary IGBT switches (T_1, T_2): when T_1 is ON and T_2 is OFF $(S_x^{j,k} = 1)$, the submodule is inserted; when T_2 is ON $(S_x^{j,k} = 0)$, it is bypassed. For each half-bridge submodule (SM), the insertion index is denoted $(\mu_x^{j,k}) \in \{0,1\}$, where $x \in \{u, d\}$ identifies the upper or lower arm, j denotes the phase, and $k = 1,2....N$ identifies the submodule number within the arm. This variable $S_x^{j,k}$ corresponds to the switching control signal of the k-th submodule in phase j.

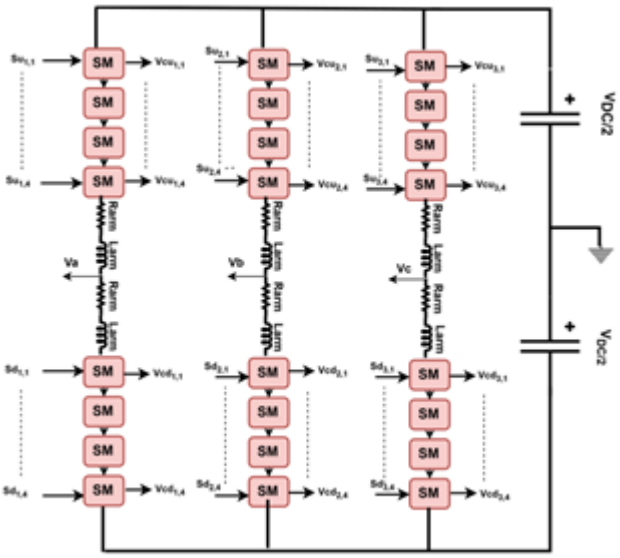

Fig. 3. MMC topology: three-phase, N = 4 submodules per arm, V_{DC} = 800 V.

TABLE 1: Nomenclature of Variables and Parameters

Submodule switching signals	$S_x^{j,k}$ *where* $j \in \{a,b,c\}$, $k \in \{1,2...N\}$ and $x \in \{u,d\}$
Arm currents	$iarm_x^j = i_x^j \quad x \in \{u,d\}$ and $j \in \{a,b,c\}$
Circulating current	$i_{cir}^j \quad j \in \{a,b,c\}$
Submodule Capacitor Voltage	$V_{cx}^{j,k} : x \in \{u,d\}$, $j \in \{a,b,c\}$ and $k \in \{0,1,2,3,4\}$
Arm vloltages	$V_x^j \quad x \in \{u,d\}$
Number of inserted submodules	$n_x^j \quad x \in \{u,d\}$
Insertion index	$\mu_x^{j,k} \quad j \in \{a,b,c\}$, $k \in \{1,2...N\}$ and $x \in \{u,d\}$
Submodule reference voltage	$V_C^{ref} = \frac{V_{DC}}{N}$
Resistor and inductance arm	$Rarm_x^j = R \quad and \quad Larm_x^j = L$
Output Voltage of MMC	$V_j \quad j \in \{a,b,c\}$

2) Arm Voltage and Current Equations

V_u^j and V_d^j denote the total inserted voltages of the upper and lower arms of phase j, respectively. From the circuit diagram in Fig. 3, the following expressions can be derived:

$$V_u^j = \frac{V_{DC}}{2} - L\frac{di_u^j}{dt} - R.i_u^j - V_j \tag{1}$$

$$V_d^j = \frac{V_{DC}}{2} - L\frac{di_d^j}{dt} - R.i_d^j + V_j \tag{2}$$

where V_j denotes the phase output voltage, while i_u^j and i_d^j represent the upper and lower arm currents, respectively.

The circulating current i_{cir}^j consists of a DC component together with an undesirable AC component, occurring mainly at twice the fundamental frequency. This AC component increases converter losses and subjects the arm inductors to additional electrical stress. The current i_f^j flows through the RC filter (R_f, C_f), which acts as the interface between the MMC converter and the three-phase source, helping to attenuate switching harmonics and ensure a smooth current waveform at the point of connection. The output current i_f^j and circulating current i_{cir}^j are defined as:

$$i_f^j = i_u^j - i_d^j \quad \text{and} \quad i_{cir}^j = \frac{i_u^j + i_d^j}{2} \tag{3}$$

3) Submodule capacitor model

The voltage dynamics of the k-th submodule capacitor in arm of phase j are governed by:

$$C\frac{dV_{cx}^{j,k}}{dt} = \mu_x^{j,k} . i_x^j \quad where \quad x \in \{u,d\} \tag{4}$$

Where $\mu_x^{j,k} \in \{0,1\}$ is the insertion index of the k-th submodule in arm j, and i_x^j is the corresponding arm current. The total arm inserted voltage is:

$$V_x^j = \sum_{k=1}^{n_x^j} \mu_x^{j,k} . V_{cx}^{j,k} \quad \text{where} \quad n_x^j \le N \quad \text{and } x \in \{u,d\} \tag{5}$$

n_x^j : Represents the number of submodules inserted in the upper or lower arm of phase j.

4) Discrete-time state-space model

For digital implementation, the continuous-time model is discretized using the forward Euler method, with sampling period Ts . The predicted output current and circulating current at step $(m+1).Ts$ are then given by:

$$i_f^j(m+1)=i_f^j(m)+\frac{T_s}{L_f}\left[V_j(m)-R_f\,.\,i_f^j(m)-V_s^j(m)\right] \quad (6)$$

$$i_{cir}^j(m+1)=i_{cir}^j(m)+\frac{Ts}{L}\left[\frac{V_{DC}}{2}-\frac{V_u^j(m)+V_d^j(m)}{2}-R.\,i_{cir}^j(m)\right] \quad (7)$$

B. FCS-MPC Control Strategy

1) Admissible Switching States

For an MMC with N = 4 submodules per arm, the number of inserted submodules in each arm of a phase can take any value from the set {0, 1, 2, 3, 4}, corresponding to N + 1 = 5 discrete voltage levels per arm. The combined switching-state space of the upper and lower arms of a single phase therefore consists of 5 × 5 = 25 possible combinations. Extending this reasoning to the three-phase system, the total number of switching states becomes $25^3 = 15625$.

Within each arm, a capacitor sorting and selection algorithm subsequently determines precisely which k submodules among the available capacitors should be activated, thereby ensuring voltage balancing without increasing the size of the optimization space. However, the constraint $n_u^j + n_d^j = N$ is generally imposed in order to keep the total number of inserted submodules per phase constant (a necessary condition for maintaining a constant arm voltage). This constraint reduces the number of per-phase combinations to (N+1) =5, since for each value of n_u^j ranging from 0 to N, n_d^j is uniquely determined. Extending this reduction to the three-phase system, the total number of switching states to be evaluated becomes $5^3 = 125$, which corresponds exactly to the reduction of the search space mentioned earlier.

2) Cost Function Design

The FCS-MPC cost function g is evaluated for each admissible switching states at each sampling instant $m.Ts$:

$$g=\lambda_1.[\Delta i_f^j]^2+\lambda_2.[\Delta i_{cir}^j]^2+\lambda_3.(\Delta V_c)^2 \quad (8)$$

Where :

$$(\Delta i_f^j)^2=(i_{ref}^a-i_f^a)^2+(i_{ref}^b-i_f^b)^2+(i_{ref}^c-i_f^c)^2$$

$$(\Delta_{cir}^j)^2=(i_{cir}^a-0)^2+(i_{cir}^b-0)^2+(i_{cir}^c-0)^2$$

$$(\Delta V_c)^2=\sum_{k=1}^{n_x^j}(V_c^{ref}-V_{cx}^{j,k})^2 \text{ with } \quad j\in\{a,b,c\} \text{ and } x\in\{u,d\}$$

where i_f^j denotes the predicted output current obtained from the discrete-time model, and i_{cir}^j represents the predicted circulating current. V_c^{ref} is the nominal capacitor voltage reference, and $\lambda_1,\lambda_2,\lambda_3$ are positive weighting factors. The three terms of the cost function are designed to minimize the output current tracking error, the deviation of the circulating current from its DC reference, and the voltage imbalance among the submodule capacitors. The optimal switching state Sopt is then obtained as: Sopt=argmin_s g(s)

where Sopt denotes the switching state that minimizes the cost function among all admissible switching states.

3) Capacitor Voltage Balancing

To ensure capacitor voltage balancing within each arm, a sorting-based selection strategy is used. The capacitor voltages are first sorted in ascending order, and the submodules to be inserted are then selected according to the direction of the arm current. When $i_x^j>0$ (arm current positive), the *n* submodules with the lowest capacitor voltages are inserted, so that the least charged capacitors are charged first. Conversely, when $i_x^j<0\,j$ (arm current negative), the *n* submodules with the highest capacitor voltages are selected for insertion, allowing the most highly charged capacitors to discharge.

4) Control Algorithm Implementation

1. At each sampling instant *mTs*, the following quantities are predicted i_f^j, i_{cir}^j and $V_{cx}^{j,k}$.

2. Evaluate *g* for each state.
3. Select the state *S* that minimizes *g*: $Sopt = \arg\min g(Si)$
4. Apply *Sopt* to the converter switches.

C. NLC Control Strategy

1) Principle and modeling of the nlc control strategy

Nearest Level Control (NLC) is a widely used control strategy for Modular Multilevel Converters (MMCs). Its principle is simple: at each instant, the number of submodules to be inserted in each arm is selected so that the generated voltage matches the reference voltage V_{ref} as closely as possible. This reference voltage is obtained from the error between the reference compensating current and the injected current, processed through a current controller and then fed to the NLC algorithm, which determines the corresponding number of submodules to insert in each arm. It is worth noting that V_{ref} is computed to track the reference compensating current, rather than to generate a purely sinusoidal voltage waveform. For an MMC with $N = 4$ submodules per arm, the converter can synthesize five discrete voltage levels, which provides a reasonably fine voltage resolution. As a result, NLC directly produces the desired multilevel voltage without relying on PWM modulation, thereby reducing the control complexity and the switching frequency of the power devices. This makes NLC particularly well suited to MMCs with a large number of submodules, although a capacitor voltage balancing mechanism is still required to ensure stable operation.

The reference voltages of the upper and lower arms are calculated according to the following expressions.

$$V_u^{ref} = \frac{V_{DC}}{2} - V_{ref} \quad \text{and} \quad V_d^{ref} = \frac{V_{DC}}{2} + V_{ref} \tag{9}$$

The number of submodules to be inserted in each arm is determined using a rounding operation with saturation, as follows:

$$n_x = sat_{[0,N]}\left(round\left(\frac{V_x^{ref}}{V_{ref}} \right) \right) \tag{10}$$

Where sat(0,N)(.) denotes the saturation function that limits its argument to interval [0,N].

This operation ensures the physical feasibility of the computed result. Subsequently, the complementarity constraint between the upper and lower arms is enforced as follows:

$$n_u^j(m) + n_d^j(m) = N \qquad \forall\, j \in \{a,b,c\} \tag{11}$$

The selection of the submodules (SMs) to be inserted is performed according to the arm current $i_x^j(m)$, where $i_x^j(m)$ denotes the measured arm current. This strategy ensures that:

- **Charging arms** $i_x^j(m) > 0$: SMs with the lowest voltage are inserted first (they charge preferentially).
- **Discharging arms** $i_x^j(m) < 0$: SMs with the highest voltage are inserted first (they discharge preferentially).

2) Evolution of the Voltage Across the SM Capacitor

The upper and lower arm voltage references are derived from the output voltage reference as follow:

$$V_u^j(m) = \frac{V_{DC}}{2} - V_j(m) \quad \text{and} \quad V_d^j(m) = \frac{V_{DC}}{2} + V_j(m) \quad \text{where } x \in \{u,d\} \tag{12}$$

Under the assumption of constant arm current over one sampling period $m.Ts$, the capacitor voltage of SM in arm j evolves as:

$$V_{cx}^{j,k}(m+1) = V_{cx}^{j,k}(m) + \frac{Ts}{C}\left[\mu_x^{j,k}(m).\, i_x^j(m)\right] \tag{13}$$

Where $\mu_x^{j,k}(m)$ is the switching state of SM (1 = inserted, 0 = bypassed) and C is the SM capacitance.

III. Results And Discussion

A. Simulation Parameters

The proposed FCS-MPC and NLC strategy was validated through detailed simulations in MATLAB/Simulink R2023b. The MMC and control parameters are summarized in TABLE 1.

TABLE 1
Simulation Parameters of the MMC System

Parameter	Value	Parameter	Value
DC-link voltage (V_{DC})	800 V	Load resistance (R_l)	20 Ω

Submodules per arm (N)	4	Fundamental frequency (f_1)	50 Hz
Nominal SM capacitor voltage (Vc)	100 V	Sampling period (T_s)	10 µs
SM capacitance (C)	3300 µF	Weighting factor λ_1 (output current)	1.0
Arm inductance (Larm)	5 mH	Weighting factor λ_2 (circulating current)	0.5
Arm resistance (Rarm)	0.1 Ω	Weighting factor λ_3 (capacitor voltage)	0.01
Load inductance (L_l)	10 mH		

B. Comparative Analysis of the FCS-MPC and NLC Harmonic Compensation Strategies

1) Source Current for the Two Control Strategies: NLC and FCS-MPC

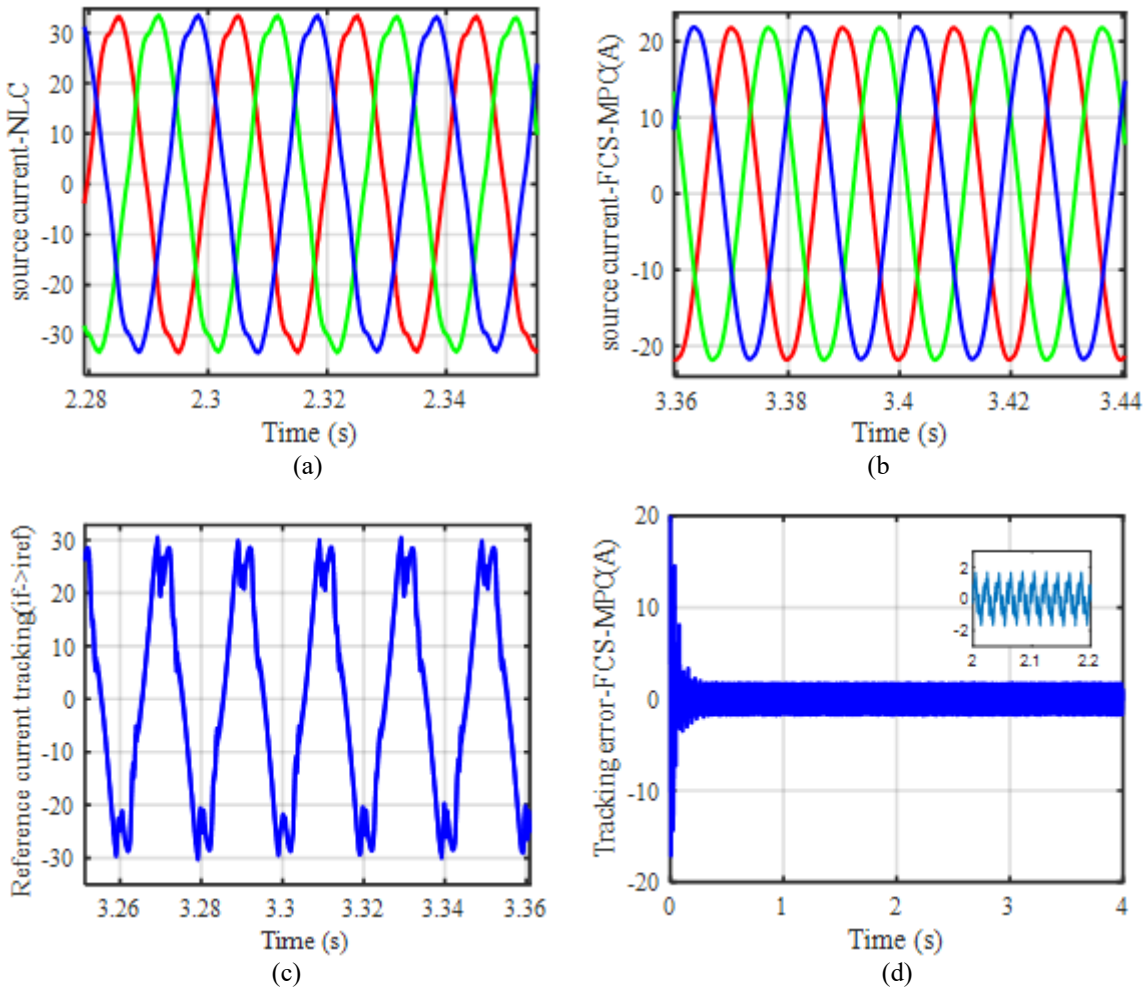

Fig. 4. Performance comparison of the NLC and FCS-MPC control strategies: (a) source currents with NLC control; (b) source currents with FCS-MPC control; (c) Reference current tracking; (d) Current tracking error;

Figs. 4(a) and (b) compares the source currents obtained with the conventional NLC strategy and the proposed FCS-MPC approach. In both cases, the source currents remain balanced and nearly sinusoidal. The FCS-MPC strategy, however, provides a noticeable improvement in current quality, yielding a source-current THD of only 1.04%, compared with 2.32% for the NLC method. This lower harmonic distortion reflects the superior current-tracking capability of the proposed predictive controller and its enhanced ability to compensate for the harmonic components generated by the nonlinear load. As a result, the FCS-MPC approach achieves better power quality and more effective active filtering performance than the conventional NLC strategy.

Fig. (c) shows the filter current i_f^j superimposed on its reference current i_{ref}^j, which appear almost perfectly overlapped throughout the simulation. This close agreement illustrates the ability of the FCS-MPC strategy to ensure accurate and fast reference tracking, confirming the effectiveness of the predictive approach in controlling the active filter. These results demonstrate that the FCS-MPC strategy provides not only a fast transient response but also excellent steady-state tracking accuracy, confirming its suitability for active filtering applications requiring fast dynamics and low residual error.

2) Circulating Current Analysis Under FCS-MPC and NLC Control Strategies

Fig. 5. illustrate the time-domain behavior of the internal circulating current $\pm 4A$ under two control strategies.

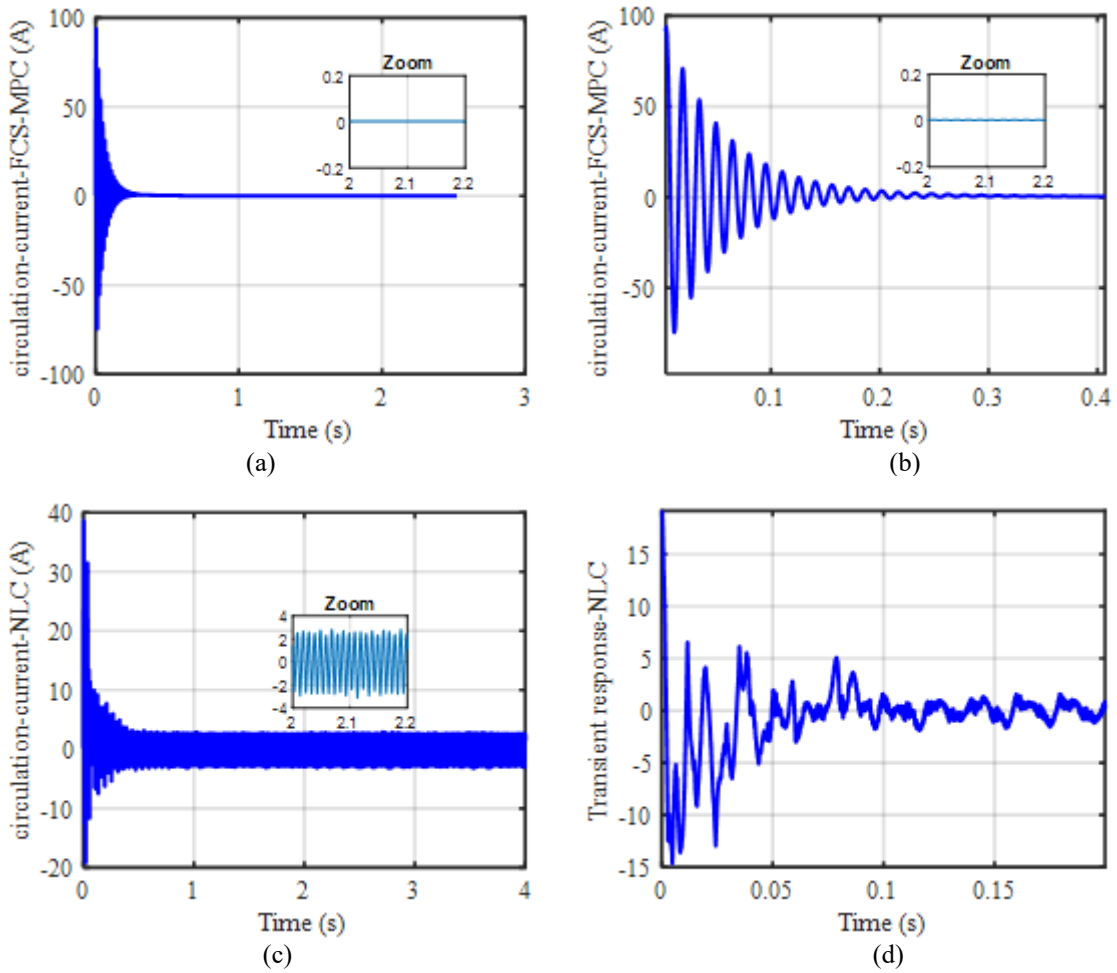

Fig. 5. Time-domain response of the circulating current under different control strategies: (a) FCS-MPC control; (b) transient response of the circulating current under FCS-MPC control; (c) NLC control; (d) transient response of the circulating current under NLC control.

Figs. 5(a) and 5(b) show the evolution of the circulating current i_{cir}^{j} under FCS-MPC control, at a global scale (Fig. 5(a)) and on an enlarged time scale (Fig. 5(b)) that allows the transient response to be examined more closely. At startup, the current shows pronounced damped oscillations reaching about ±90 A. This transient lasts roughly 0.3 s, after which it converges rapidly toward zero. Once steady state is reached, the ripple becomes negligible, as confirmed by the zoomed inset, pointing to effective suppression of the internal circulating current. These results illustrate the ability of FCS-MPC to keep the circulating current under tight control, supporting stable, balanced, and efficient operation of the MMC.

For the NLC strategy, Figs. 5(c) and 5(d) show the corresponding circulating current at a global scale and on an enlarged time scale, respectively. As seen in Fig. 5(d), the transient lasts about 0.4 s, with oscillation amplitudes comparable to those observed under FCS-MPC. In steady state, however (Fig. 5(c)), the circulating current still shows noticeable oscillations, with a peak-to-peak amplitude of about 4 A (−2 A to +2 A), as highlighted in the zoomed inset, evidence of residual internal current harmonics. While the NLC controller keeps the system stable, its ability to suppress circulating-current fluctuations remains limited compared with FCS-MPC.

Overall, these results confirm that FCS-MPC clearly outperforms NLC in attenuating the circulating current and enhancing the internal energy balance of the MMC. NLC, while still ensuring stable operation, leaves residual low-frequency oscillations in steady state.

3) Submodule Capacitor Voltage Regulation Under FCS-MPC and NLC in a Modular Multilevel Converter

Fig. 6. illustrates the capacitor-voltage response of the submodules under FCS-MPC and NLC control strategies.

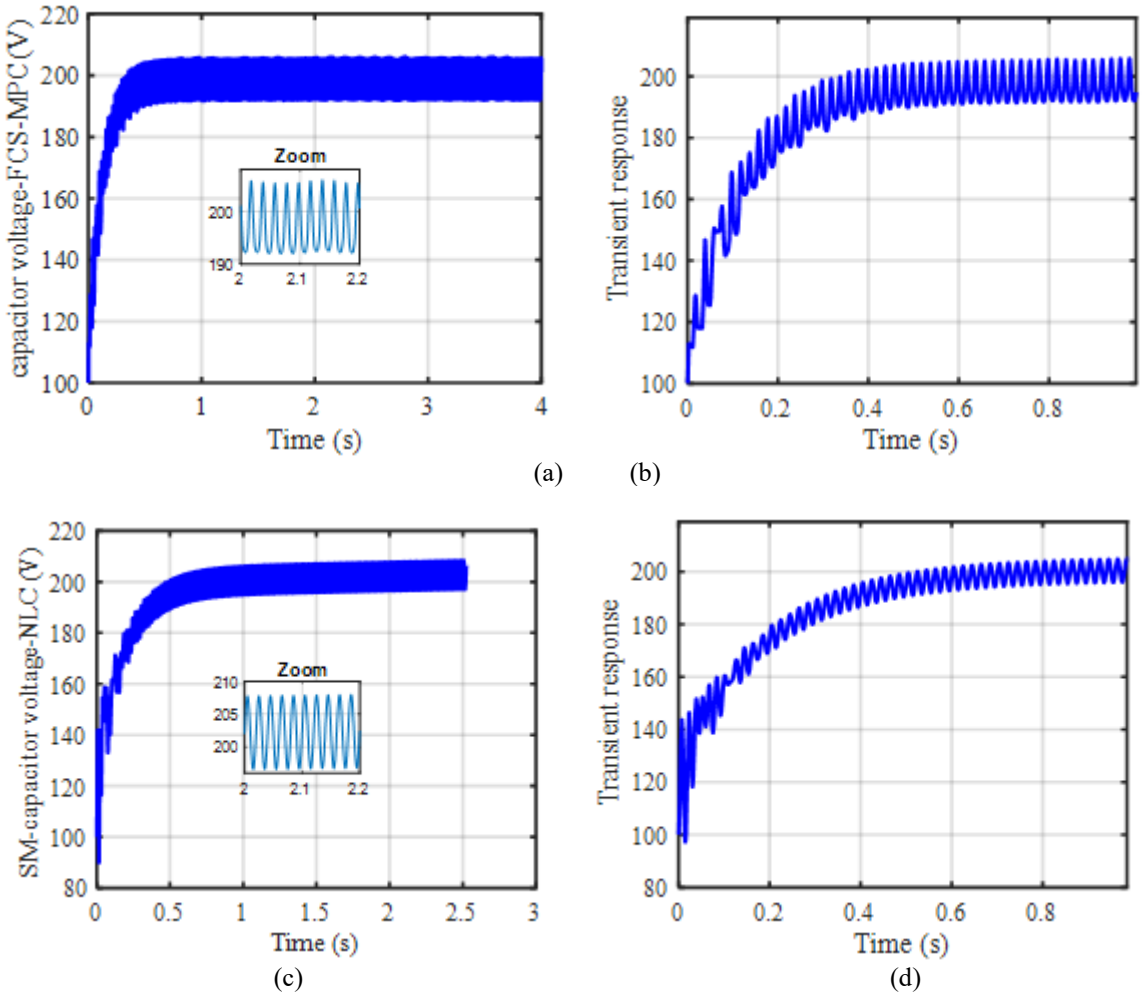

Fig. 6. Capacitor voltages: balancing transient and steady-state ripple ($N = 4$, V_{DC} **= 800 V).**

Starting from their initial conditions, the capacitor voltages rise rapidly and converge toward the reference value $V_c^{ref} = 200V$, corresponding to an equal distribution of the 800 V DC-link voltage among the four submodules. Both control methods achieve stable operation and proper voltage balancing, but FCS-MPC reaches steady state faster, with smaller voltage deviations during the charging process. Once steady state is reached, the capacitor voltages stay centered around their reference value, and the zoomed views show that the voltage ripple under FCS-MPC is lower than under NLC. This points to the superior ability of the predictive controller to regulate the internal energy of the converter and maintain capacitor-voltage balance. Overall, the results confirm that FCS-MPC provides more effective capacitor-voltage regulation, lower steady-state ripple, and better energy-balancing performance than the conventional NLC approach.

As shown in Figs. 6(a) and 6(b), the submodule voltage under FCS-MPC settles to steady state more quickly, in about 0.5 s, whereas under NLC the transient is longer, taking roughly 0.8 s to stabilize, and $V_{cx}^{j,k}$ shows larger oscillations in steady state. This further confirms that FCS-MPC offers better accuracy and stability in balancing the submodule capacitor voltages of the MMC.

E. Voltage Regulation Under FCS-MPC and NLC in a Modular Multilevel Converter

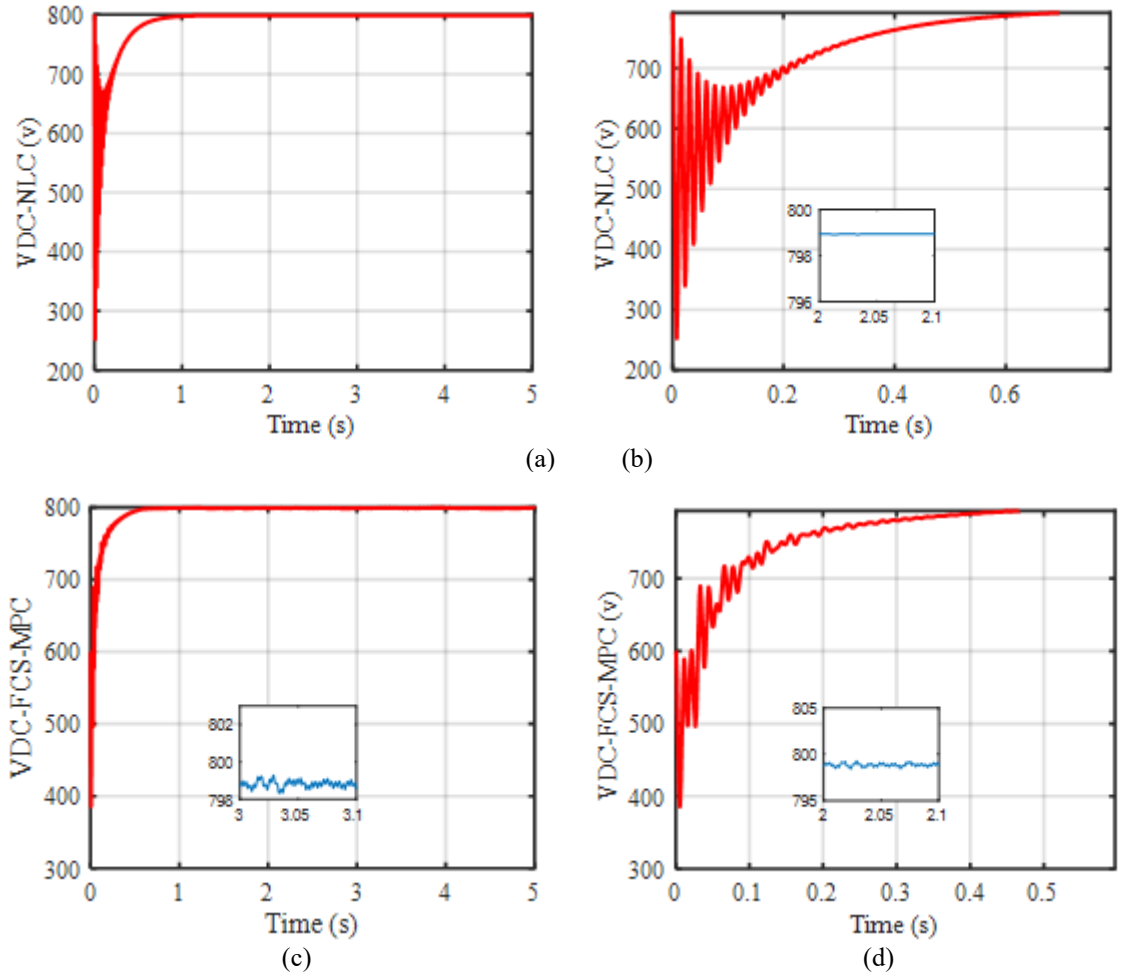

Fig. 7. DC-link voltage V_{DC}: (a) global response under FCS-MPC control; (b) global response under NLC control; (c) transient response under FCS-MPC control; (d) transient response under NLC control.

Under FCS-MPC control, the DC-link voltage shows a smooth, well-controlled transient. Starting from about 400 V, it rises steadily toward the 800 V reference, reaching it in roughly 0.5 s without any overshoot or oscillation. From that point onward, the voltage stays essentially flat for the rest of the simulation (up to $t = 1$ s), with negligible ripple at the macroscopic scale. This reflects the predictive controller's strong ability to regulate the DC-link energy while simultaneously managing the AC-side current injection, confirming its excellent steady-state accuracy and disturbance rejection.

NLC, by contrast, produces a noticeably slower transient. At startup, the DC-link voltage dips sharply, dropping to about 300 V before recovering and climbing back toward the 800 V reference. This pronounced sag points to a temporary energy imbalance, caused by the absence of predictive current control during the initialization stage. The voltage then gradually recovers, settling at its reference value after about 0.8 s. Once steady state is reached, the DC-link voltage remains stable, with no significant ripple visible at this time scale.

IV. Conclusion

This paper presented the implementation and comparative assessment of two control strategies, namely Finite Control Set Model Predictive Control (FCS-MPC) and Nearest Level Control (NLC), applied to a Modular Multilevel Converter (MMC) composed of four submodules per arm and operating with an 800 V DC-link voltage. Both control approaches simultaneously address output current regulation, circulating current suppression, and capacitor-voltage balancing.

Simulation results obtained in MATLAB/Simulink demonstrate the superior performance of the proposed FCS-MPC strategy. Specifically, FCS-MPC achieves a source-current total harmonic distortion (THD) of 1.04%, significantly lower than the 2.32% obtained with the NLC strategy. Moreover, the capacitor-voltage ripple is reduced to approximately ±6.5 V, compared with ±10 V under NLC operation. The proposed

predictive controller also exhibits faster transient response, improved reference current tracking capability, and lower steady-state error than the conventional NLC approach.

These findings confirm the effectiveness and suitability of the proposed FCS-MPC strategy for MMC-based active power filter applications. Future research will focus on extending the proposed control scheme to MMC topologies with a larger number of submodules to further investigate its scalability and robustness. In addition, real-time implementation on hardware platforms such as Digital Signal Processors (DSPs) and Field-Programmable Gate Arrays (FPGAs) will be pursued to validate the practical feasibility of the controller. Further efforts will also be directed toward reducing the computational burden and enhancing the controller's robustness under grid disturbances and parameter uncertainties.

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