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SSPC – Based Secondary Power Distribution System for Typical Aircraft Application

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Abstract: *The increasing adoption of More-Electric Aircraft technology has created demand for efficient and lightweight electrical power distribution systems. This work presents the design and simulation of a Solid-State Power Controller (SSPC)-based system for a typical aircraft application. SSPCs provide several advantages over conventional electromechanical circuit breakers, including improved reliability, reduced maintenance requirements, and enhanced system protection. A ±270 V DC aircraft power distribution architecture is considered, and the SSPC is implemented using Silicon Carbide MOSFETs. The complete secondary power distribution system is modeled and simulated in LTspice to evaluate its performance under normal operating and fault conditions. Wide-bandgap SiC MOSFETs address the limitations of conventional circuit breakers by enabling microsecond-level fault isolation and programmable inverse-time I^2t overcurrent protection. Two topologies were designed and simulated: SSPC-S using a single CAS350M12BM3 SiC MOSFET module (4mΩ, 1200 V) and SSPC-M using five parallel C2M0025120D discrete devices at ±270 V DC with 85°C. LTspice circuit simulations validated turn-off transient behaviour with and without MOV and capacitive snubber protection and verified the protection profile of the I^2t tripping curve. SSPC-S achieves a steady-state junction temperature of 105°C and peaks at 146°C under the worst-case cascaded overcurrent scenario, both within the 175°C device limit. SSPC-S is confirmed as the superior topology, delivering lower conduction loss, higher power density, and simpler gate-drive design for MEA secondary power distribution.*

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I. Introduction

The aviation sector is undergoing a major transformation, driven by stricter environmental regulations, increasing demands for lower fuel consumption, and rapid advancements in power electronic technologies [2], [15]. For many years, aircraft platforms relied on mechanical, hydraulic, and pneumatic systems for secondary power distribution and onboard load management [3]. Such conventional arrangements introduce several disadvantages, including higher structural weight, extensive maintenance requirements, and continuous energy losses throughout operational service life. The More Electric Aircraft (MEA) concept addresses these concerns by replacing numerous non-electrical subsystems with electrically powered alternatives, resulting in improved efficiency, reduced fuel usage, and lower operating costs across aircraft platforms [2], [15].

Electrical power demand in modern aircraft has risen significantly, exceeding one megawatt in large platforms such as the Boeing 787 Dreamliner and Airbus A380. In response, aircraft power distribution systems have gradually progressed beyond conventional 28 V DC and 115 V AC standards toward higher operating voltages, including 270 V DC and 540 V DC in military aircraft, along with 230 V AC in civil platforms [2], [16]. A bipolar ±270 V DC high-voltage DC (HVDC) architecture, investigated by Huang et al. [1], has emerged as a practical option for civil tilt-rotor applications because higher distribution voltage enables equivalent power transfer at lower current levels, resulting in a noticeable reduction in aircraft cable weight while maintaining required power delivery capability [2], [4].

The transition toward higher-voltage DC distribution networks demands a different approach for onboard power switching and protection functions [3]. Conventional electro-mechanical circuit breakers (EMCBs) exhibit several limitations during DC operation, including fault-clearing delays of 20–30ms, arc generation during contact separation due to the absence of a natural current zero-crossing, limited short-circuit interruption capability, increased weight and volume per channel, and reduced operational life under repeated high-current fault events [14], [19]. Solid State Power Controllers (SSPCs) have emerged as a semiconductor-based alternative to EMCBs in aircraft Power Distribution Units (PDUs), integrating fast switching capability and protective functionality within a compact and intelligent structure [3], [15].

As shown in Fig. 1, a typical ±270 V DC electrical power distribution architecture for More Electric Aircraft (MEA) incorporates engine-driven generators, an Auxiliary Power Unit (APU), Primary Electrical Power Distribution Centers (EPDCs), and Secondary Power Distribution Units (SPDUs) responsible for supplying both HVDC and LVDC loads. Protection of power cables linking generator power converters and EPDCs is achieved using high-current, high-voltage protection devices. Conventional electro-mechanical circuit breakers continue to face reliability concerns in DC networks because arc extinction becomes difficult in the absence of a voltage zero-crossing. Consequently, Solid State Power Controllers have attracted significant attention for MEA power distribution applications owing to superior switching and protection characteristics.

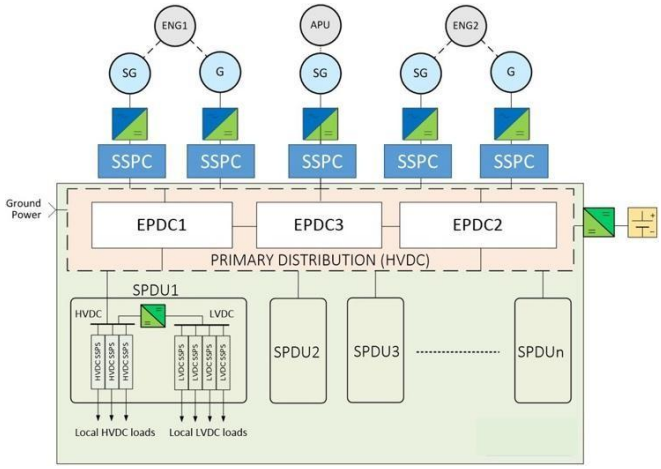

FIGURE 1: Typical Aircraft Electrical Power Distribution Architecture Employing SSPCs.

As illustrated in Fig. 1, SSPCs utilize the fast-switching characteristics of Silicon Carbide (SiC) MOSFETs to detect overcurrent and short-circuit faults within microseconds, interrupt fault currents without arc formation, and transmit fault information directly to the aircraft Load Management System (LMS) [5], [8]. Such features make SSPCs highly suitable for aerospace environments where severe electromagnetic interference and elevated thermal stresses are frequently encountered [10]. For the present work, the Wolfspeed CAS350M12BM3 SiC MOSFET module has been selected as the primary switching device. The module provides a drain-source voltage rating of 1200 V, a continuous current capability of 325 A at a case temperature of 90°C, and a low on-state resistance of 4 mΩ, making it an effective single-device solution for a 100 A SSPC operating from a ±270 V DC distribution bus, as supported by experimental findings reported in published literature [1], [8].

In addition to rapid fault isolation, SSPCs provide programmable overcurrent protection through inverse-time current-squared-time (I^2t) algorithms that closely represent conductor heating behaviour during transient overload conditions [6], [7]. Such protection helps safeguard wiring harnesses against excessive thermal stress while avoiding unnecessary tripping during short-duration inrush current events [9]. Once load current exceeds its rated value, the accumulated I^2t quantity increases progressively, causing trip operation at a duration inversely proportional to the square of the fault-current magnitude, closely matching the thermal endurance characteristics of copper wiring harnesses used in aircraft electrical systems [6], [11]. Combined operation of high-speed semiconductor interruption and software-configurable protection characteristics represents a significant improvement over conventional fuses and mechanical circuit breakers across key performance requirements associated with MEA secondary power distribution networks [3], [7].

II. Methodology

This section presents the fundamental architecture, key design considerations, and protection strategies analysed using the LTspice simulation environment for the Solid-State Power Controller (SSPC).

2.1 Block Diagram and System Configuration

As illustrated in Fig. 2, the proposed architecture is designed to achieve low-latency fault clearing and microsecond-level fault isolation within a high-voltage DC aircraft distribution network. Solid-State Power Controllers are widely adopted for high-voltage DC power management due to reliable overcurrent protection, arc-free switching operation, and advanced software-based diagnostic functions. The primary purpose of the configuration is to monitor and regulate line current within a ±270 V DC secondary aircraft distribution system while protecting wiring harnesses and connected loads from severe short-circuit faults. Operation is achieved

through continuous branch-current measurement using dedicated sensing hardware, followed by processing inside an embedded controller executing a real-time digital protection algorithm. Independent monitoring of conductor thermal behaviour and transient current variations enables accurate protection decisions, reduces unnecessary tripping events, maintains power availability for healthy feeders, and enhances overall distribution-system reliability.

The proposed protection structure incorporates inverse-time I²t processing algorithms, dedicated current-sensing circuitry, Metal Oxide Varistors (MOVs), a parallel capacitive snubber network, and a wide-bandgap Silicon Carbide (SiC) MOSFET power stage. The embedded I²t protection routine continuously evaluates accumulated thermal stress and initiates isolation whenever predefined current limits are exceeded. In addition, the dual-element overvoltage suppression network restricts inductive flyback voltage transients generated during high-current interruption events, thereby protecting the semiconductor device from excessive electrical stress.

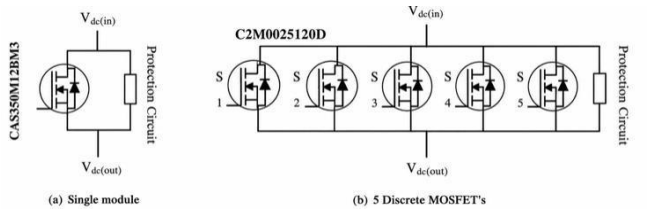

FIGURE 2: Two types of SSPC designs for 100A rating.

2.2 Silicon Carbide MOSFET Power Stage Selection and Topologies

The adoption of wide-bandgap Silicon Carbide (SiC) MOSFET technology represents an important design approach in modern aerospace power electronics for reducing steady-state conduction losses and improving thermal operating capability. The selected configuration is designed to support nominal distribution currents up to 100 A while maintaining low forward voltage drop and reliable operation under voltage stresses reaching 1200 V. Careful optimisation of semiconductor device arrangement contributes to reduced cooling requirements and a compact power-stage structure. Compared with conventional parallel discrete-device configurations, a high-current single-module topology offers improved current distribution characteristics and enhanced thermal performance, making it well suited for demanding high-voltage aerospace applications [4].

A high-current aircraft secondary distribution channel may be realised using two different topological approaches. The single-module configuration (SSPC-S) employs one Wolfspeed CAS350M12BM3 module with an on-state resistance of 4 mΩ, whereas the multi-device configuration (SSPC-M) uses five parallel Wolfspeed C2M0025120D devices to carry the 100 A load current. In the single-module arrangement, the power stage functions as an integrated thermal structure, promoting more uniform heat dissipation through a common case interface.

Such a configuration reduces localised temperature concentrations, lowers conduction-related losses, and maintains semiconductor junction temperatures within safe operating limits. In contrast, discrete-device arrangements require closely matched gate-drive paths to avoid unequal current distribution during switching events. The single-module approach simplifies hardware implementation, reduces current-sharing concerns, and supports higher power density with improved operational reliability across the aircraft distribution system [4].

2.3 Digital I²t Inverse-Time Overcurrent Protection Scheme

Digital inverse-time I²t overcurrent protection, often referred to as programmable thermal modelling, is widely employed in aircraft power protection systems for accurate monitoring of conductor heat accumulation. The fundamental principle involves representing overload currents through equivalent thermal behaviour, where one operating region accommodates short-duration inrush currents while another addresses sustained overcurrent conditions. Implementation is achieved by processing real-time branch current measurements through a discrete numerical integration routine that estimates conductor during motor starting events, and provides improved protection accuracy across a broad range of overload conditions.

Within the digital protection loop, line current is continuously squared and integrated over time to determine the cumulative thermal energy experienced by the feeder. The calculated energy value is repeatedly compared with predefined threshold limits established from aerospace wiring standards. Small current deviations produce slower accumulation rates and longer operating delays, whereas severe short-circuit conditions drive the integration process rapidly toward its tripping threshold. Consequently, fault-clearing action occurs within a very short duration under high-current fault conditions.

By monitoring instantaneous current behaviour and maintaining thermal history through dedicated

software accumulators, the protection algorithm achieves reliable fault identification, stable recovery characteristics, and effective overcurrent interruption performance. Generated trip commands are transferred directly to the gate-drive circuitry through low-latency control channels. Following trip initiation, the SiC MOSFET is turned off to isolate the faulted section and maintain safe system operation [5].

Compared with conventional thermal-magnetic circuit breakers, digital I²t protection provides substantially faster response during short-circuit events, improved tolerance to temporary current surges, elimination of manual reset requirements, and consistent trip performance unaffected by ageing or vibration effects. Owing to such advantages, software-programmable I²t protection characteristics have become a preferred solution in More Electric Aircraft platforms, defence electrical systems, and high-reliability aerospace power distribution networks where dependable and configurable fault isolation is essential [5].

The steady-state power loss calculations are defined by equation (1) and (2) where T_j and T_a the junction temperature and ambient temperature of the MOSFETs, T_c is the device baseplate case temperature, $R_{dson(max)}$ and R_{thja} are the maximum on-state resistance of the MOSFET and thermal resistance from junction to ambient respectively. While the multi-stage transient overcurrent junction tracking bounds are expressed through equations (3),(4),(5) and (6) where n is the number of MOSFETs in parallel, I_{dc} is the nominal current rating of the SSPC, $I_{d(mos)peak}$ is the peak transient current, P_{max} is the peak power dissipation, Z_{thja} is the transient thermal impedance of the device, $C_{l(mos(sspc))}$is the conduction loss of SSPC and $\eta_{mos(sspc)}$ is the efficiency of SSPC.

$$P_{loss} = \frac{T_j - T_a}{R_{thja}} \quad (1)$$

$$I_{d(mos)} = \sqrt{\frac{T_j - T_a}{R_{thja} \cdot R_{dson(max)}}} \quad (2)$$

$$T_{j(act)} = \frac{I_{dc}^2}{n^2} \cdot R_{dson(max)} \cdot R_{thja} + T_a \quad (3)$$

$$P_{max} = \frac{T_j - T_c}{Z_{thja}} \quad (4)$$

$$I_{d(mos)peak} = \sqrt{\frac{T_j - T_c}{Z_{thja} \cdot R_{dson(max)}}} \quad (5)$$

$$T_{j(act)} = \frac{I_p^2}{n^2} \cdot R_{dson(max)} \cdot Z_{thja} + T_c \quad (6)$$

$$C_{l(mos(sspc))} = \frac{I_{dc}^2}{n} \cdot R_{dson(T_{j(act)})} \quad (7)$$

$$\eta_{mos(sspc)} = 1 - \frac{I_{dc}}{n \cdot V_{dc}} \cdot R_{dson(T_{j(act)})} \quad (8)$$

Compared with conventional thermal-magnetic circuit breakers, digital I²t protection provides substantially faster response during short-circuit events, improved tolerance to temporary current surges, elimination of manual reset requirements, and consistent trip performance unaffected by ageing or vibration effects. Owing to such advantages, software-programmable I²t protection characteristics have become a preferred solution in More Electric Aircraft platforms, defence electrical systems, and high-reliability aerospace power distribution networks where dependable and configurable fault isolation is essential [5]. The approximated inverse-time tripping characteristic employed in the present SSPC design is illustrated in Fig. 3, demonstrating the relationship between fault-current magnitude and corresponding trip duration. It shows how long the SSPC allows an overcurrent condition before disconnecting the load.

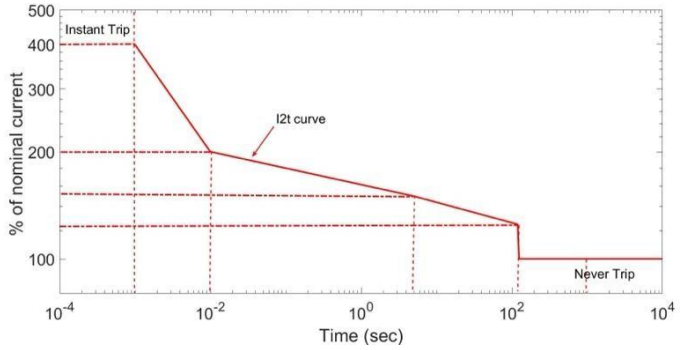

FIGURE 3 : The approximated I^2t curve line of Direct Current SSPC.

2.4 Dual-Element Transient Over-Voltage Suppression

Preservation of dielectric safety margins is achieved by limiting the voltage overshoot developed across the drain and source terminals during rapid release of stored inductive energy following a trip event. The proposed dual-element protection arrangement safeguards the semiconductor device through the combined action of a Metal Oxide Varistor (MOV) and a capacitive snubber network, thereby restricting overvoltage stress and reducing the possibility of device damage. The overall power conversion efficiency and conduction-loss characteristics of the power stage are evaluated using (7) and (8), where Idc denotes the continuous DC line current, Vdc represents the nominal DC bus voltage, n indicates the number of parallel semiconductor branches, and Rdson corresponds to the on-state channel resistance evaluated at the operating junction temperature. Lower conduction-loss values indicate improved electro-thermal performance and a more efficient solid-state power distribution system.

III. Hardware Sizing and Design Methodology

This section presents the detailed design methodology, component sizing procedures, protection-circuit development stages, and comparative topological assessments carried out to enhance the operational reliability of the SSPC power stage.

3.1 Dual-Element Over-Voltage Suppression Network Design

When the line current exceeds the predefined protection threshold, the gate-drive circuit rapidly reduces the channel voltage and isolates the faulted path within microseconds. During interruption of a peak short-circuit current of 400 A, a significant inductive flyback transient is produced as the magnetic energy stored in the 15 µH cable inductance is released over a very short duration. Under unprotected operating conditions, forcing current decay within a 10 µs turn-off interval generates a drain-to-source voltage transient exceeding 1.4 kV. Such a condition results in a peak power stress approaching 450 kW and injects approximately 2.3 J of thermal energy into the semiconductor device, potentially leading to permanent device failure.

To limit the resulting overvoltage transient and evaluate overall power-stage performance, parameters including transient voltage stress, stored inductive energy, source-energy contribution, and power-conversion efficiency are determined using the design equations presented in (9) through (10) where V_{dc} is the voltage across the SSPC, V_{sw} is the transient voltage stress across the semiconductor device, L_{dc} is the inductance of the DC transmission line, I_{p} is the peak current of the SSPC, W_{l} is the inductive energy, V_{CB} is the clamping voltage, W_{source} is the injected energy and W_{total} is the total energy.

$$V_{\mathrm{sw}} = V_{\mathrm{dc}} + L_{\mathrm{dc}} \cdot \frac{\Delta I_{\mathrm{p}}}{t_{\mathrm{fall}}} \tag{9}$$

$$W_{\mathrm{l}} = \frac{1}{2} \cdot L_{\mathrm{dc}} \cdot {I_{\mathrm{p}}}^2 \tag{10}$$

$$W_{\mathrm{source}} = \frac{L_{\mathrm{dc}} \cdot V_{\mathrm{dc}} \cdot {I_{\mathrm{p}}}^2}{2 \cdot (V_{\mathrm{CB}} + V_{\mathrm{dc}})} \tag{11}$$

$$W_{\mathrm{total}} = \frac{1}{2} \cdot L_{\mathrm{dc}} \cdot {I_{\mathrm{p}}}^2 \cdot \left(1 + \frac{V_{\mathrm{dc}}}{V_{\mathrm{CB}} + V_{\mathrm{dc}}}\right) \tag{12}$$

At the maximum fault current of 400 A, the energy stored within the cable inductance is approximately 1.2 J. When the contribution from the DC bus during the interruption interval is considered, the total energy absorption requirement (Wtotal) increases to nearly 2 J. To manage this energy safely, a thermally protected Metal Oxide Varistor (MOV, V275LA20A) is selected as the primary protection element. The MOV limits the peak drain-to-source voltage to a range of 600–850 V, maintaining operation within the safe voltage limits of the 1200 V SiC MOSFET. Application of the MOV significantly reduces transient thermal stress within the CAS350M12BM3 module, lowering the estimated junction temperature rise from approximately 66°C under unprotected conditions to about 31°C during fault interruption.

3.2 Localized Soft-Switching Shunt Capacitor Modeling

To further reduce transient thermal stress during fault interruption, a soft-switching capacitive branch is connected directly across the drain and source terminals of the power switch. Due to its rapid response characteristic, the capacitor provides an alternate current path before the MOV enters its low-impedance operating region, thereby reducing instantaneous power dissipation within the semiconductor device. The complete overvoltage protection arrangement incorporating the MOV and capacitive snubber network is illustrated in Fig. 4.

The required snubber capacitance (Csnub), associated transient thermal response, and turn-on inrush current characteristics are determined using the design equations presented in (13)–(15), where Iinrush represents the inrush current of the SSPC.

$$\Delta T_{j(act)} = \frac{1}{2} \cdot I_p \cdot V_{CB} \cdot Z_{thja}(t) \quad (13)$$

$$C_{snub} = \frac{I_p \cdot \Delta t}{V_{CB}} \quad (14)$$

$$I_{inrush} = \frac{C_{snub} \cdot V_{dc}}{\Delta t} \quad (15)$$

Application of the design equations results in a snubber capacitance value of C_{snub} = 0.7 µF. The combined action of the MOV and capacitive snubber significantly reduces the transient electrical and thermal stress experienced by the power device during fault interruption. As a result, the peak power dissipation across the single-module SSPC decreases to approximately 45 kW, while the corresponding junction temperature rise is limited to about 6°C–7°C during fault-clearing operation. The complete protection circuit incorporating the MOV and snubber capacitor is shown in Fig. 4.

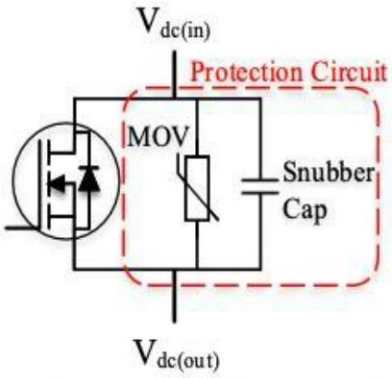

FIGURE 4: Protection circuit of the SSPC with MOV and snubber capacitor

3.3 Topological Comparison and Implementation Benchmarks

The operational characteristics and implementation requirements of the two SSPC topologies were evaluated to determine suitability for aircraft secondary power distribution applications. The single-module configuration (SSPC-S) employs a Wolfspeed CAS350M12BM3 SiC MOSFET module, whereas the parallel-device configuration (SSPC-M) consists of five C2M0025120D SiC MOSFETs mounted on a common heatsink having a thermal resistance of 0.2°C/W. The positive temperature coefficient exhibited by SiC devices supports

stable current distribution among parallel-connected switches and reduces the likelihood of thermal instability during operation.

Branch-current measurements are continuously acquired through the current-sensing circuit to detect overload and short-circuit conditions. The measured signals are processed by a digital protection algorithm operating with a sampling interval of 10 μs and implementing a discrete numerical integration routine. Upon detection of a valid fault condition, the protection logic updates the tripping parameters and commands the gate-drive circuit to disconnect the affected feeder.

Although the parallel-device topology (SSPC-M) provides satisfactory fault interruption capability, it requires closely matched gate-drive paths to maintain balanced current distribution and introduces additional layout complexity. In contrast, the single-module configuration (SSPC-S) avoids current-sharing concerns, simplifies gate-drive implementation, and reduces overall component count. As summarized in Fig. 5, the SSPC-S configuration demonstrates lower conduction losses, higher power density, and improved reliability, making it a suitable choice for aerospace secondary power distribution applications.

IV. Simulation and Results

This chapter presents the simulation results obtained for the proposed Solid-State Power Controller (SSPC) under normal operating conditions, overload conditions, and short-circuit fault scenarios.

4.1 Electro-Thermal Verification of the SSPC-S Module Topology

The single-module SSPC configuration (SSPC-S) was evaluated using a multi-stage Foster RC thermal network derived from the Wolfspeed CAS350M12BM3 manufacturer datasheet. As illustrated in Fig. 5, the thermal model incorporates the equivalent junction-to-case and case-to-ambient thermal paths. The heatsink operating condition was maintained at a thermal resistance of 0.2
°C/W with an ambient temperature of 85°C.

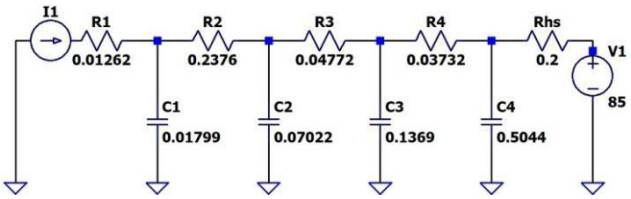

FIGURE 5: Thermal circuit schematic of SSPC-S

Figure 6 presents the simulated junction-temperature and power-loss characteristics of the SSPC-S module. During steady-state operation at the rated current of 100 A, the device exhibits a conduction loss of approximately 70 W. The corresponding thermal equilibrium temperature settles near 105°C. Under the most severe short-circuit condition of 400 A, the junction temperature rises progressively through the internal thermal network and reaches a peak value of 146°C.

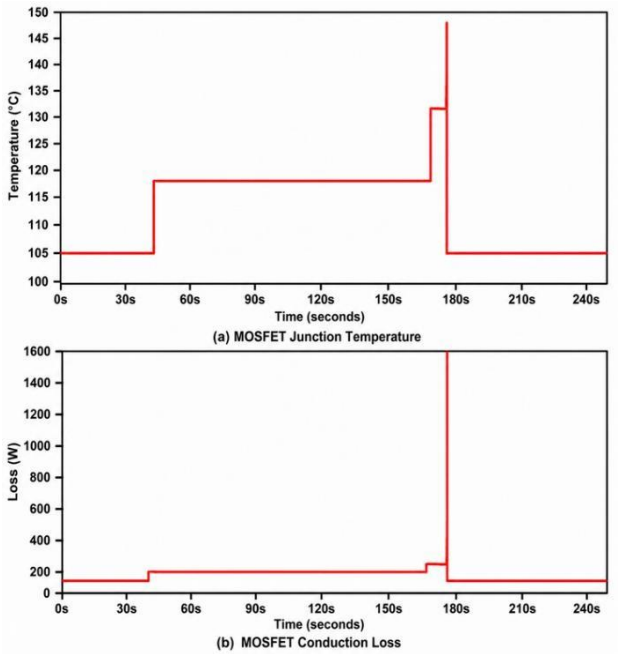

FIGURE 6: Simulation results of the junction temperature and loss of a MOSFET module of the SSPC-S

4.2 Comparative Electro-Thermal Profile of the SSPC-M Discrete Array

The discrete-device SSPC configuration (SSPC-M) employs five parallel-connected C2M0025120D SiC MOSFETs, allowing the 100 A load current to be shared equally among five branches carrying approximately 20 A each. As shown in Fig. 7, each TO-247 package possesses a junction-to-case thermal resistance of 0.27 °C/W, exceeding that of the single-module implementation.

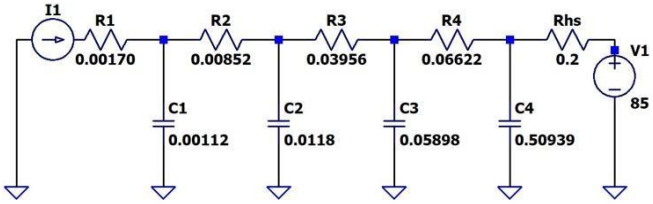

FIGURE 7: Thermal circuit schematic of SSPC-M

At rated operating conditions, temperature rise within the devices increases the effective on-state resistance to approximately 45 mΩ, resulting in an individual power dissipation of 18 W. The combined thermal load transferred to the common heatsink reaches nearly 90 W, exceeding the SSPC-S configuration by approximately 20 W. Consequently, the steady-state junction temperature reaches 107.86°C. Under fault conditions, the peak junction temperature remains below 125°C, maintaining a thermal margin of about 25°C relative to the maximum allowable package temperature of 150°C. The simulated junction-temperature and power-loss characteristics of the SSPC-M configuration are presented in Fig. 8.

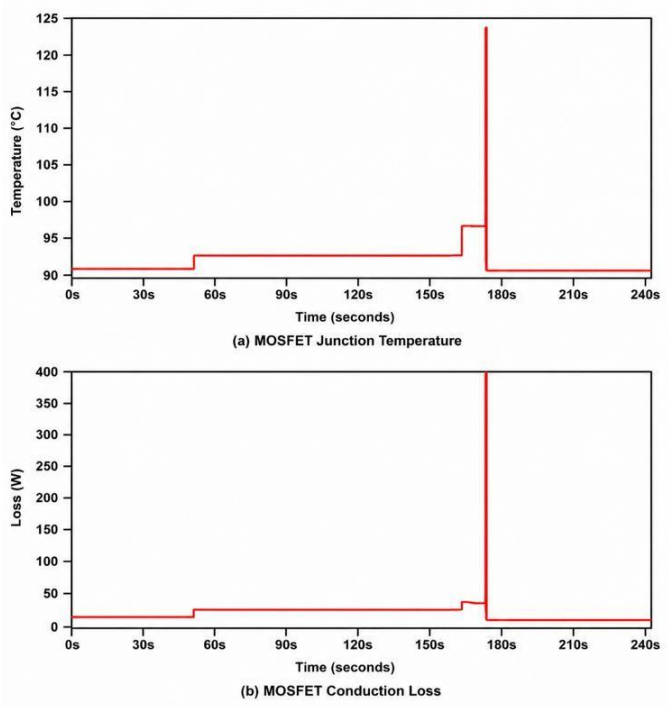

FIGURE 8: Simulation results of the junction temperature and loss of a MOSFET module of the SSPC-S

4.3 Turn-Off Transient and Active Overvoltage Clamping Evaluation

The transient performance of the proposed SSPC was assessed by comparing unprotected fault interruption behaviour with protected operating conditions for both the SSPC-S and SSPC-M configurations.

4.3.1 Unprotected Interruption Vulnerabilities

Interruption of a 400 A fault current within a 10 µs turn-off interval across a 15 µH line inductance produces substantial inductive overvoltage transients

As illustrated in Fig. 9, the SSPC-S topology operating without overvoltage protection is subjected to severe electrical stress during fault interruption. Resonance between the line inductance and device output capacitance causes the drain-to-source voltage to rise beyond 1.4 kV. Such an overvoltage condition coincides with high-current conduction, producing a peak power dissipation approaching 450 kW and depositing approximately 2.3 J of energy within the semiconductor junction. The resulting voltage stress exceeds the 1.2 kV blocking capability of the device and may lead to dielectric breakdown.

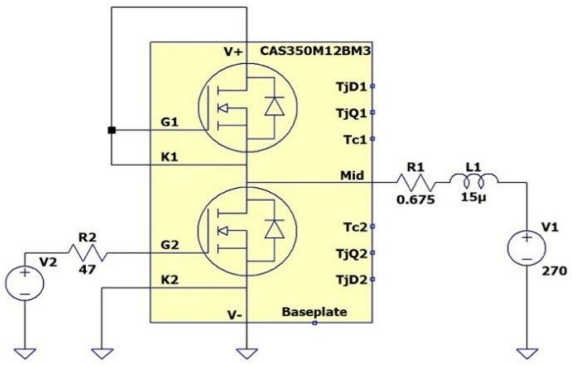

FIGURE 9 : Circuit schematic of SSPC-S without over-voltage protection

The corresponding transient waveforms obtained for the unprotected SSPC-S configuration are presented in Fig. 10. The drian source voltage across the MOSFET,drain current through the MOSFET and power dissipated across the MOSFET are shown in the Fig.10

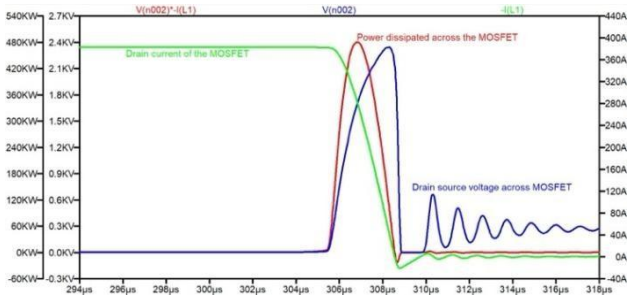

FIGURE 10 : Waveform of unprotected SSPC-S

When the SSPC-M topology experiences the same fault interruption condition, small variations in device parameters and gate-threshold characteristics cause individual MOSFETs to turn off at slightly different rates.

As shown in Fig. 11, the absence of overvoltage protection exposes the parallel-device arrangement to unequal current sharing during the interruption process. The final conducting device temporarily carries a larger portion of the residual current, increasing the local current rate of change (di/dt). Such behaviour initiates high-frequency oscillations that elevate the drain-to-source voltage to nearly 1.6 kV per device, increasing the likelihood of avalanche breakdown and progressive failure within the parallel array.

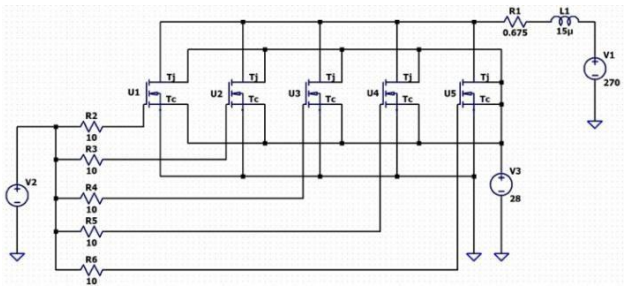

FIGURE 11: Circuit schematic of SSPC-M without over-voltage protection

The simulated transient response of the unprotected SSPC-M configuration is presented in Fig. 12. parallel array. per device, causing cascading avalanche failure across the parallel array.

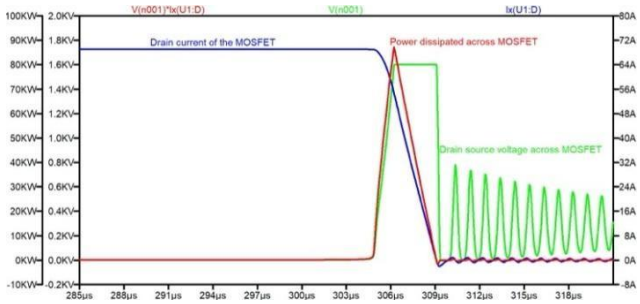

FIGURE 12: Waveform of unprotected SSPC-M

4.3.2 Mitigation via Standalone MOV Clamping

Incorporation of a Metal Oxide Varistor (MOV) across the power switch provides an effective method for suppressing transient overvoltage conditions. As illustrated in Fig. 13, the MOV is connected in parallel with the SSPC-S power stage to limit excessive drain-to-source voltage during fault interruption.

When the drain-to-source voltage exceeds the MOV clamping threshold, the device transitions rapidly into a low-resistance operating region. As a result, a portion of the fault energy is diverted through the MOV, limiting the peak voltage transient to approximately 700–800 V.

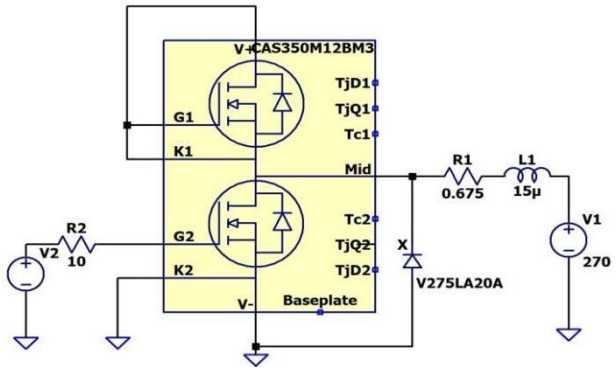

FIGURE 13: Circuit schematic of SSPC-S with MOV protection

The stored inductive energy is dissipated safely within the MOV structure, reducing the transient junction temperature rise to nearly 31°C. The corresponding transient response of the protected SSPC-S configuration is presented in Fig. 14.

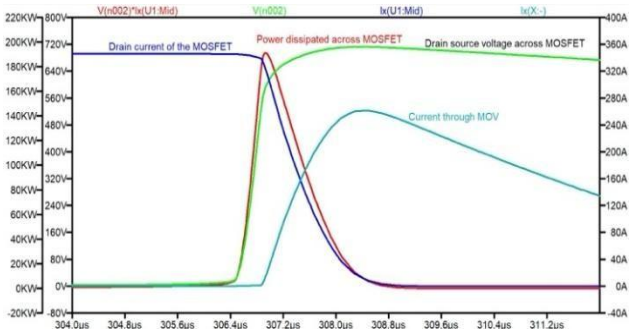

FIGURE 14: Waveform of protected SSPC-S

For the SSPC-M configuration, the protection arrangement shown in Fig. 15 employs a common V275LA20A MOV connected across the output bus. The nonlinear clamping characteristic restricts the overvoltage transient to a similar 700–800 V range, thereby reducing electrical stress on individual devices and limiting transient power dissipation. The resulting protected operating waveform is illustrated in Fig. 16. The waveform shows the drain source voltage across MOSFET, drain current through the MOSFET and power dissipated across the MOSFET.

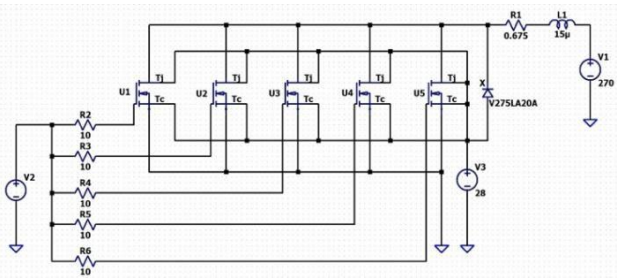

FIGURE 15: Circuit schematic of SSPC-M with MOV protection

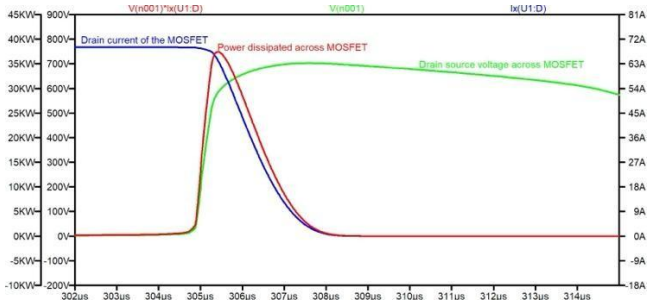

FIGURE 16: Waveform of protected SSPC-M

4.3.3 Soft-Switching Dual-Element Network Optimization

To suppress high-frequency voltage oscillations and further reduce transient thermal stress, a dual-element protection network consisting of a MOV and a capacitive snubber was implemented. For the SSPC-S topology, a 0.7 μF metallized-film snubber capacitor was connected directly across the drain and source terminals of the CAS350M12BM3 module, as shown in Fig. 17.

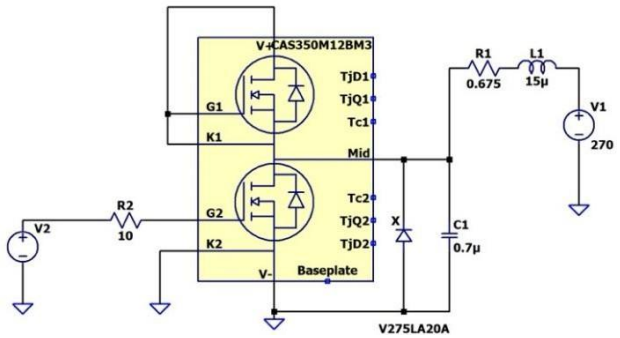

FIGURE 17: Turn-off schematic of SSPC-S with MOV and Capacitive snubber

During interruption of a 400 A fault current, the snubber capacitor provides a temporary low-impedance path that limits the rate of voltage rise across the switch. Such behaviour significantly reduces switching stress and lowers the peak power dissipation from approximately 210 kW to nearly 45 kW. Consequently, the transient junction temperature rise remains limited to about 6°C–7°C. The associated turn-off response is presented in Fig. 18.

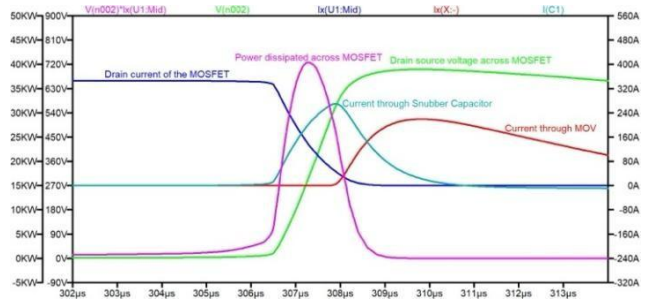

FIGURE 18: Turn-off waveform of SSPC-S with MOV and Capacitive snubber

To investigate turn-on behaviour, the gate-drive circuit was configured with a 20 Ω turn-on resistor, limiting the current rise rate and reducing electromagnetic interference during switching transitions. The turn-on circuit arrangement is illustrated in Fig. 19, while the corresponding turn-on waveform is presented in Fig. 20.

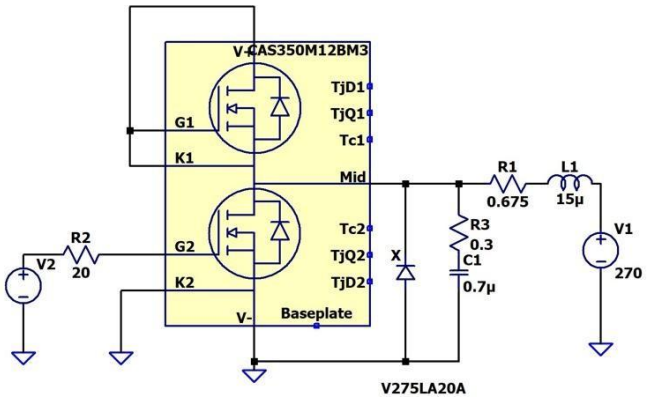

FIGURE 19: Turn-on schematic of SSPC-S with MOV and Capacitive snubber

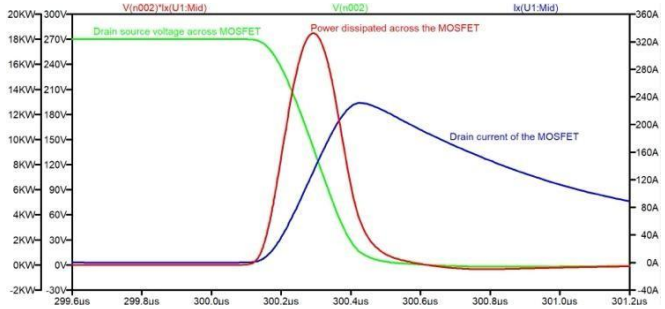

FIGURE 20: Turn-on waveform of SSPC-S with MOV and Capacitive snubber

For the SSPC-M topology, individual 10 Ω gate resistors were incorporated to suppress oscillations produced by parasitic interactions among parallel switching paths. During turn-off operation, additional parasitic inductance within the distributed layout introduces a small voltage overshoot before MOV conduction becomes dominant. To achieve stable turn-on performance, 15 Ω gate resistors were employed within the gate-drive network.

The turn-off circuit and corresponding transient response of the SSPC-M configuration are presented in Fig. 21 and Fig. 22, respectively.

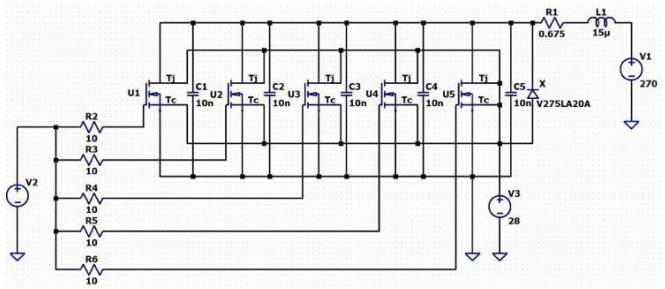

FIGURE 21: Turn-off schematic of SSPC-M with MOV and Capacitive snubber

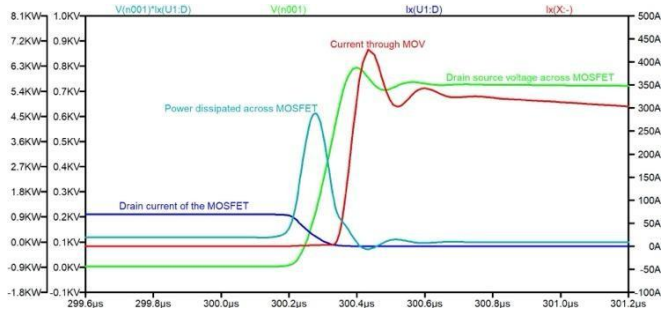

FIGURE 22: Turn-off waveform of SSPC-S with MOV and Capacitive snubber

Similarly, the turn-on circuit arrangement and associated switching waveform are illustrated in Fig. 23 and Fig. 24.

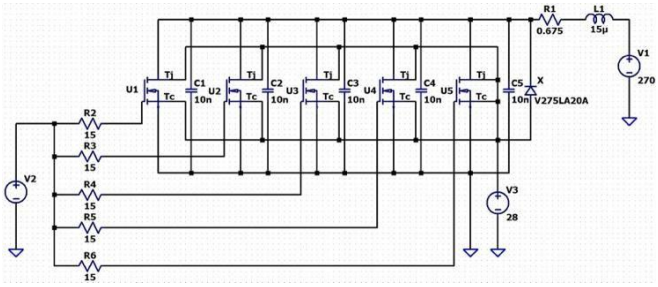

FIGURE 23: Turn-on schematic of SSPC-M with MOV and Capacitive snubber

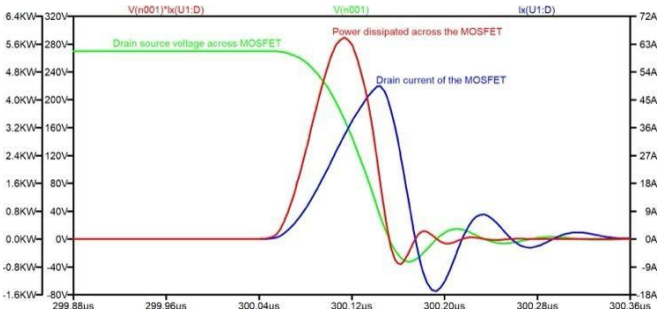

FIGURE 24: Turn-on waveform of SSPC-M with MOV and Capacitive snubber

During turn-on operation, stray inductances present in the PCB layout interact with device capacitances, producing short-duration high-frequency current oscillations. The gate-damping resistors effectively dissipate the associated oscillatory energy, causing the transient disturbance to decay within approximately 1 µs and ensuring stable switching operation.

4.3.4 Soft-Switching Dual-Element Network Optimization

A comparative assessment of the thermal performance characteristics of the SSPC-S and SSPC-M configurations is presented in Table 1. The comparison includes conduction loss, steady-state junction temperature, and peak transient junction temperature under fault conditions.

Results indicate that the SSPC-S topology exhibits lower overall thermal stress and reduced power dissipation while maintaining acceptable junction temperatures during both normal and fault operation.

TABLE 1: Thermal Performance and Conduction Loss Comparison of SSPC

Sl.No	Thermal Parameter	SSPC-S Thermal Model	SSPC-M Thermal Model
1	Static Conduction Power Loss	70W	18 W Per Device
2	Steady-State Junction Temperature	105 °C	107.86 °C
3	Transient Peak Overcurrent Temp	146 °C	125 °C Per Device

TABLE 2: Power and Energy Dissipation in the Junction of the MOSFET

Sl.No	SSPC Configuration & Circuit Topology	Peak Power per MOSFET (kW)	Energy Dissipated across the MOSFET (J)
1	SSPC-S (No Protection)	440	3.52
2	SSPC-S (With MOV Only)	210	0.42
3	SSPC-S during Turn-on (MOV + Capacitor Snubber)	46	0.092
4	SSPC-S during Turn-off (MOV + Capacitor Snubber)	18	0.042
5	SSPC-M (No Protection)	130	0.08
6	SSPC-M (With MOV Only)	21	0.0042
7	SSPC-M during Turn-on (MOV + Capacitive Snubber)	65	0.012
8	SSPC-M during Turn-off (MOV + Capacitive Snubber)	5.8	0.058

The thermal results demonstrate that the SSPC-S configuration achieves a lower steady-state junction temperature rise and reduced conduction losses compared with the parallel-device SSPC-M implementation. Although both topologies operate within safe thermal limits, the single-module approach provides improved thermal utilisation and reduced cooling requirements for aerospace power distribution applications.

A comparison of power dissipation and energy absorption during different fault-interruption scenarios is summarized in Table 2. The analysis considers unprotected operation, MOV-only protection, and dual-element protection employing both MOV and capacitive snubber networks for SSPC-S and SSPC-M configurations.

Results presented in Table 2 show that implementation of MOV protection significantly reduces peak power stress and junction energy dissipation when compared with unprotected operation. Further improvement is achieved through the combined MOV and capacitive snubber network, where both peak power and absorbed energy are reduced substantially. Among the evaluated configurations, the SSPC-S topology with dual-element protection exhibits the lowest energy dissipation and superior transient thermal performance, confirming the effectiveness of the proposed protection strategy.

V. Conclusion

The present work demonstrated the design and simulation of a Silicon Carbide (SiC) MOSFET-based Solid-State Power Controller (SSPC) intended for a ±270 V DC More Electric Aircraft (MEA) secondary power distribution network. A single Wolfspeed CAS350M12BM3 SiC MOSFET module was selected for the SSPC-S topology because of its 4 mΩ on-state resistance and 1200 V blocking capability. Simulation studies performed in LTspice verified reliable operation at a nominal current rating of 100 A under an ambient

temperature of 85°C. The electro-thermal analysis indicated a steady-state conduction loss of 70 W and a junction temperature of 105°C. During a severe 400 A short-circuit condition governed by the inverse-time I^2t protection characteristic, the maximum junction temperature reached 146°C, remaining below the specified device limit of 175°C.

To address inductive overvoltage generated by the 15 μH transmission line, a protection network consisting of a Littelfuse V275LA20A Metal Oxide Varistor (MOV) and a 0.7 μF capacitive snubber was incorporated into the design. Simulation results showed that the protection circuit limited the turn-off voltage transient to approximately 600–650 V and restricted the transient junction temperature rise to nearly 6–7°C during interruption of a 400 A fault current [5]. Comparative analysis between the SSPC-S and SSPC-M topologies demonstrated that the single-module implementation achieved lower conduction losses (70 W compared with 90 W) while avoiding current-sharing challenges and additional parasitic effects associated with parallel device arrangements [4]. Based on the obtained results, the SSPC-S topology represents a suitable solution for aircraft secondary power distribution applications requiring high reliability and efficient fault protection.

Future investigations may focus on bidirectional SSPC structures intended for regenerative aircraft loads, multi-channel power distribution architectures, FPGA-based protection platforms with reduced processing latency, evaluation of Gallium Nitride (GaN) devices for higher-voltage aircraft systems, and integration of ARINC 429 communication interfaces for enhanced compatibility with aircraft load-management systems [9].

Conflict of Interest

The author(s) declare(s) that there is no conflict of interest regarding the publication of this paper.

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