DC-DC Resonant converters with APWM control

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Abstract: *An asymmetrical pulse width modulated (**APWM**) dc-dc converters operating at constant frequency was simulated using Pspice software package. This converter incorporates constant frequency operation in a basic soft switching half bridge topology without any additional component and complexity. In this paper operation of converter configuration with capacitive filter in the output is discussed. A 5V, 50W converter was designed, fabricated using MOSFET and then tested to verify the characteristic of the converter. Due to asymmetrical duty ratio and zero voltage switching (**ZVS**) operation, this converter has low device voltage and current stresses wit no increase in conductively loss. This topology combines the best features of resonant (zero switching loss) and switched mode (low conduction loss) circuits.*

Key words: *Soft switching, Zero voltage switching (ZVS), Asymmetrical pulse width modulated (APWM), Zero current switching (ZCS), Switched mode power supplies (SMPS)*

I. Introduction

Switched mode power supplies (SMPS) are extensively used in most electronic equipment on account of their high efficiency, small size and low cost. The high power density demand and the availability of fast power diodes, push the switching frequency close to Mega Hz region. At this frequency range, lossless switching becomes challenging to maintain high efficiency [1]. Soft switched converters using power MOSFETs have been recognized as candidates for high density dc-dc power converter applications[2],[3].However, they suffer from limitations like increased current level, voltage stresses of devices and minimum load requirement. Another constraint results from the use of the switching frequency as the control variable [4]. Output control through frequency modulation requires that the magnetic components be rated for the entire range of operating frequencies. The variable switching frequency also makes suppression of conducted electromagnetic interference (EMI) difficult to implement. Further more the wider frequency variation for the output voltage regulation needs the larger input and output filters [9]. Some of the above mentioned limitations can be overcome by using half bridge (HB) or full bridge(FB) based circuits with ZVS action during transitions [4],[5]. But FB is not preferred due to unattractive economical factor. HB uses only two power devices, but undesirable for varying frequency. Again difficulty arises to control the converter at constant switching frequency and the ZVS conditions by means of symmetrical drive of both switches [6].Because the OFF interval of both devices is fixed by the resonant circuit parameters, the ON interval of each switch cannot be varied under the condition of constant switching frequency. Moreover, hard switching topologies are rarely used now days in face of drawbacks like high switching stresses, losses and EMI interference.
This paper studies the asymmetrical control of switches in half bridge topology under ZVS conditions.

2.1. Resonant switch dc-dc converters:

A resonant network is added to the conventional hard switching PWM topology. The resonant network consists of passive elements L, C, diodes and semiconductor devices like MOSFET, IGBT etc. sometimes the leakage inductances of the transformer and parasitic capacitance of the semiconductor device are exploited to provide resonance. This resonant network creates the soft switching conditions (ZVS or ZCS) for power device transitions. These converters are subdivided into ZVS converter, ZCS converter and ZVS-clamped converter. The outputs in these converters are controlled by the operating frequency /switching frequency (frequency of gate pulses applied to (power devices/switches).

The work for this paper was performed on ZVS – clamped converter owing to its superior and better performance compared to other topologies. In this topology, the turn off and turn on of the device take place at zero voltage. Also the peak voltages of the devices are clamped at the input voltage level. The capacitor connected across each device ensures the device get turned on only at zero voltage. Otherwise the stored energy in the capacitor get dissipated through the power device or switch. The anti parallel diode across must conduct prior to the gating of the power device. However, this converter has the disadvantage of high device/switch currents.

2.2. Asymmetric duty cycle PWM converter.

Switched mode power supplies seldom operate at variable frequency modulation as the magnetic and filter design create problem at these frequencies. Using constant frequency operation or PWM technique these drawbacks are overcome but at low duty ratio the soft switching conditions is rarely achieved. Hence APWM technique is introduced at constant frequency to ensure the power device/switch transitions occur at zero voltage.
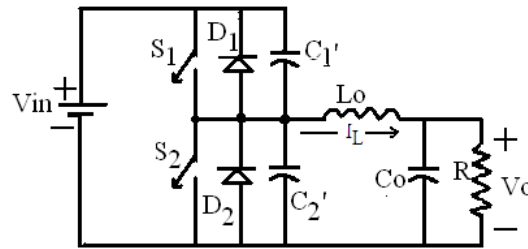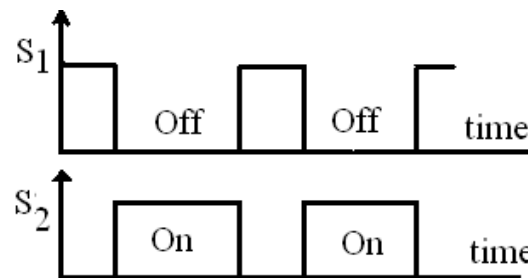

Fig.1 ZVS-Clamped voltage topology

Fig.2 Trigger pulse for APWM control

A basic half bridge topology is shown in fig.1. Using APWM technique one switch/power device of the converter operates for a duty cycle less than 50% while the other switch for duty ratio greater than 50%. Fig.2 shows the trigger pulse required for the half bridge converter under APWM control. Referring to the expanded waveform (fig.3) of the primary voltage and current of the transformer, the switch/power
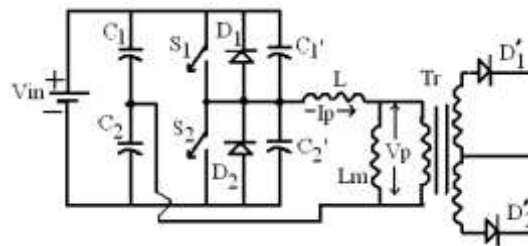

Fig.3 Basic half Bridge topology

device S_1 is turned off at t_o. The current that had been flowing through S_1 tends to flow through the parasitic capacitance C_1' and C_2'. This current charges C_1' and discharges C_2' driving the voltage across transformer primary voltage Vp to zero. But Vp continues to fall below as the inductor 'L' releases its stored energy aiding in the charging and discharging of parasitic capacitance C_1' and C_2' further. Discharge of C_2' below zero is prevented by conduction of D_2. Thus clamping Vp at that point and returning the remaining stored to source.

At t_1, the power device S_2 is turned on, ensuring losses switching as D_2 will conduct prior to S_2. After t_1, current through the inductor Ip reverses its direction. t_2-t_3 interval same as t_0-t_1.

3.1 Design Aspects:

To sustain balanced volt-seconds on the transformer primary (by equal area criteria) as shown in fig.4 we have

$\qquad$ **Vc$_1$ = Vin (1-D)** $\qquad$ **(1)**
$\qquad$ **Vc$_2$ = Vin D** $\qquad$ **(2)**
Therefore, **Vc$_1$ D = Vc$_2$ (1-D)** $\qquad\qquad$ **(3)**
where Vc$_1$, Vc$_2$ are the voltages across C$_1$ and C$_2$ .D and Vin is the duty ratio, input source voltage respectively.
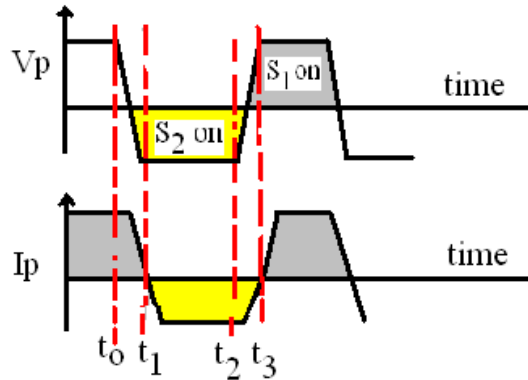
Fig.4 Half bridge APWM waveforms

The output voltage is given by

$$V_o = \frac{[V_{c_1}D + V_{c_2}(1-D)]}{n} \qquad \text{- (4)}$$

Where Vo is the output voltage and n is the number of turns.

The equation for the current through the power devices S_1, S_2 and Io, output current are given by the authors in reference [6].

$$I_1D = I_2(1-D)$$

$$\frac{Io}{n} = \frac{I_1 + I_2}{2}$$

$$I_1 = \frac{2Io(1-D)}{2}$$

$$I_2 = \frac{2IoD}{2} \qquad \text{-(5)}$$

During the start of transition interval circuit has energy stored in its inductance. At the end, the stored energy has been transferred to the parasitic capacitances. If the inductor energy is sufficient enough to completely charge the capacitor voltages to the input source voltage, then circuit switches loss lessly. Otherwise loss free switching is lost. The equation for energy storage in transformer leakage inductance , C_1' and C_2' are given by reference in [6]

$$\mathbf{LI_2^2 = C_e Vc_1^2} \qquad \textbf{(6)}$$

4.1 Design and Fabrication:

Low and medium power level rated APWM dc–dc resonant converter with capacitive filter satisfying ZVS condition while operating at constant frequency is discussed. The operation of above converter lies in the range of 0 – 50% duty cycle or 50 – 100% duty cycle.
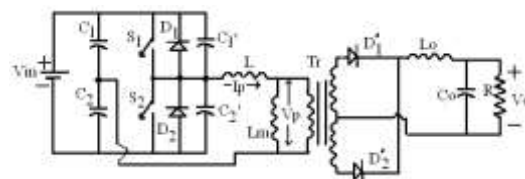

Fig.5 Half bridge capacitive filter circuit

In capacitive filter configuration fig 5, the transformer is current fed due to the presence of L, inductor in the input side and absence of inductor Lo, in the output side. The secondary current is rectified and fed to capacitive filter. The output filter attenuates the high frequency ripple current content in load current Io to provide a constant output voltage Vo across the load R. Lm is the magnetizing inductance, L the inductance at

the primary of the transformer. Input capacitances C_1, C_2 have the same value and divide the supply voltage Vin such that $Vc_1 + Vc_2 = Vin$.

Assumptions made:
1. Transformer secondary side leakage inductance neglected.
2. Forward drop and capacitance of the output diodes neglected.
3. C_1, C_2, C_0 (output filter) are selected large enough to maintain the voltage across them constant.

There should be a minimum dead time before one switch is turned on after the other switch is turned off. This dead time depends on transformer primary current Ip, the inductor L and parasitic capacitances C_1', C_2'. The switch transition cannot be made too fast or too slow. If too slow, it will be comparable to the switching period affecting the steady state performance of the circuit. If too fast, ZVS conditions will not be attained. For better results the power devices may be turned ON as built-in diode/body diode of power device conducts conducting.

4.2 SPECIFICATIONS:
1. Input Voltage Vin = 48V
2. Output Voltage Vo = 5V
3. Load current Io = 10A
4. Switching frequency fs = 20 KHz.

Duty ratio, output voltage and load current are the parameters, which determine the ratings of MOSFET and output diodes. MOSFET, IRF 540, output diodes IN3537 and ferrite core transformer with turns ratio equal to 3. The maximum operating duty ratio is fixed to 0.48. Capacitance value of 0.1µf across each MOSFET and the output filter of 100µf are selected.

The input capacitance C_1 and C_2 must is much larger than output filter capacitance Co. Thus 470µF, 100V capacitor available in the lab was used for experimental purpose. Moreover the leakage inductance of the transformer was found sufficient to achieve soft switching conditions without the aid of any additional inductor.

4.3 Hardware Implementation:
The triggering or gating pulse was generated using ICL8083 Precision waveform generator, IR2110 high speed MOS driver, operational amplifier LM324 and LM311. MOSFET are provided with heat sinks. The input voltage source of 48V is derived from 4*12 V batteries. By varying the control voltage to the comparator LM311 the pulse width of the gate signal can be varied. A dead time of 1usec is introduced between gating pulses for simulation as well as hardware circuit. Fig.6 and fig.7. a & b shows the circuit diagram for experimental and Pspice simulation purpose.
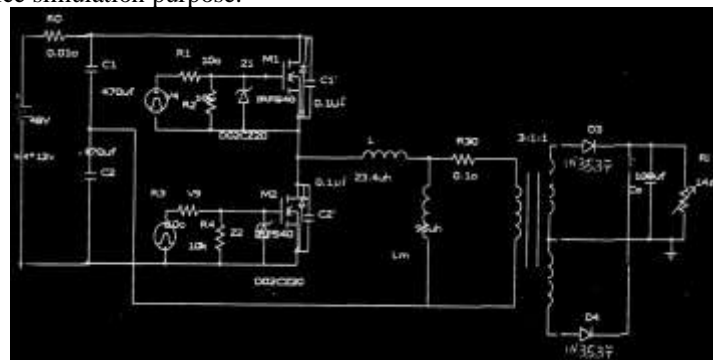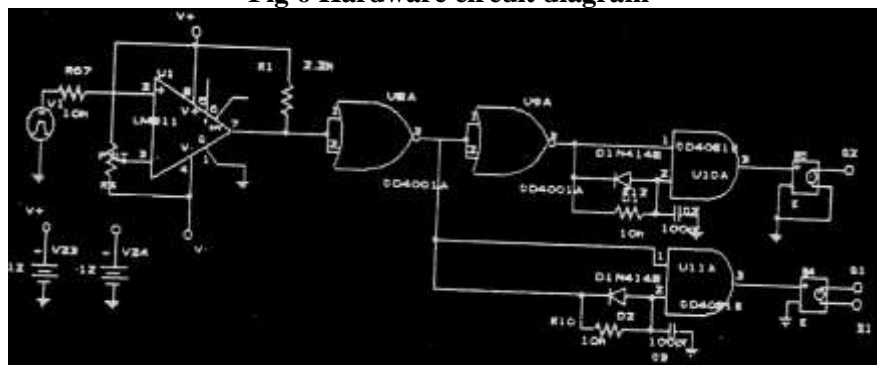

Fig 6 Hardware circuit diagram
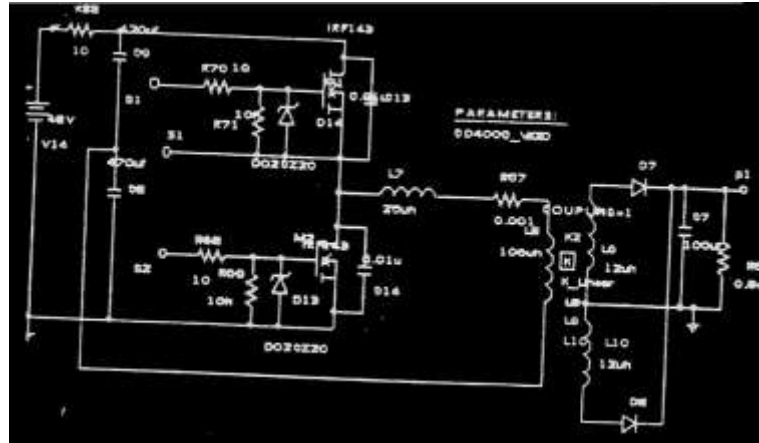

Fig.7.a. Pspice gating circuit

Fig.7.b. Power circuit in Pspice

II. Results:

Fig.8.a&b shows primary voltage and current, output voltage for the experimental circuit. with duty ratio of 0.48. It is observed that drain to source voltage falls to zero before the devices are turned on. Thus, ZVS operation is achieved as the built in diode of the MOSFET conducts before the turn ON of the MOSFET.
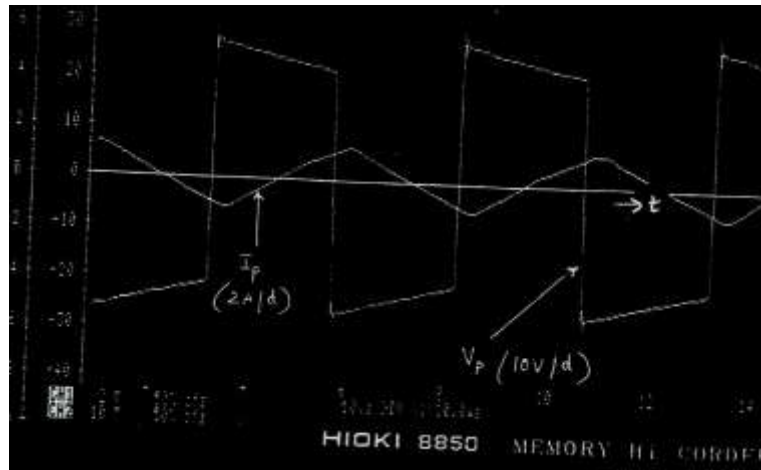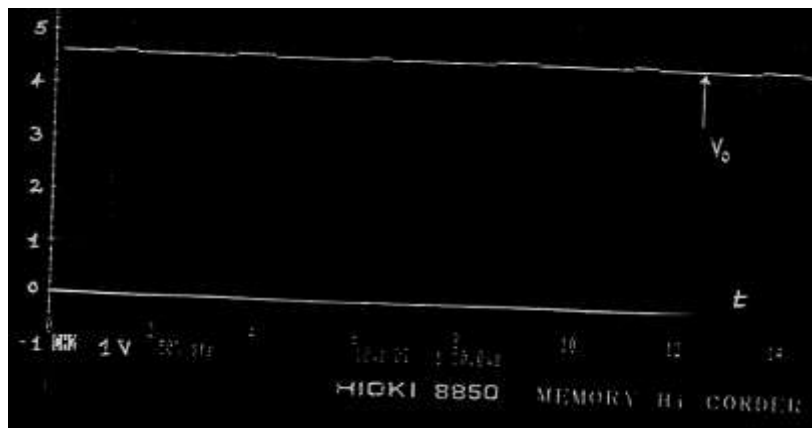

Fig.8.a Vp, Ip for hardware circuit

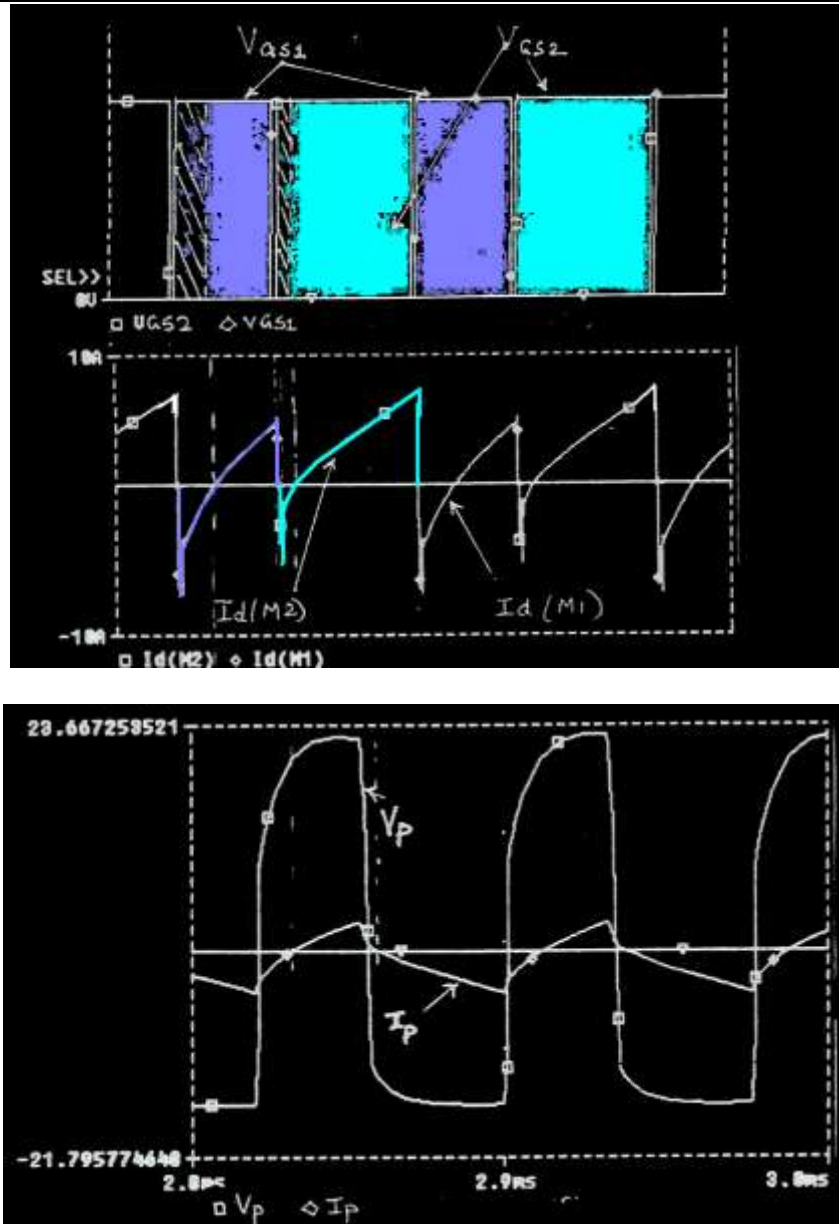**Fig.8.b output voltage Vo for hardware circuit**

Fig 9 Primary voltage and current for capacitive filter in Pspice

Fig.9 depicts the simulated waveform for the converter fabricated above. The simulated primary voltage and current waveforms also show turn ON and turn OFF of the MOSFET occur at zero voltage.

III.   Discussions:

The difference between the parameter values used in simulation and fabrication is in the value of capacitance $C_1^{'}$ and **C2'** i.e. instead of 0.001μF, 0.1μF is used. When the capacitance value of 0.1μF is used for $C_1^{'}$ and **C2'** during fabrication the primary voltage Vp is subjected to high voltage spikes at turn ON transition. Moreover, unexpected heating of switches are recorded for 0.001μF value of $C_1^{'}$ and **C2'**. The waveforms of primary current Ip obtained from simulation and experimental   verifies the equal area criterion. It is observed that the waveforms of Vp and Ip do not possess half wave symmetry although the net area in one cycle is zero. This ensures asymmetrical PWM control.

Fourier analysis of the output waveform using PSpice was performed to study the harmonic contents in this converter. Harmonics of 2nd and 4th order are observed. However their values are not of any significant figure.

Advantages like smaller filer circuits, low component, low device voltage stress, low conduction loss and effective use of parasitic elements are attained with this converter. Likelihood of transformer saturation at higher duty ratios and sluggishness of response due to output filter are the drawbacks to highlight .

IV.   Conclusions:

The Pspice simulation verifies the operation of 5V, 50W converter with capacitive filter exhibiting ZVS at constant frequency. The results of the Pspice simulation are matching with the experimental waveforms. By varying the duty cycle through asymmetrical drive of switches leads to soft switching condition even at light load. The experimental results too confirm the ZVS operation at constant frequency utilizing APWM .

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Biography:

Preeta John graduated in Electrical Engineering from T.K.M College of Engineering, (Kerala University) Kollam, Kerala - India and post-graduated in Power Electronics from National Institute of Technology Calicut, Kerala - India. Her areas of interest are soft switched DC-DC and DC-AC converters and Renewable energy sources. She is currently heading the Electronic department at NTTF at R D Tata Technical Education Centre, Jamshedpur.