IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676, p-ISSN: 2320-3331, Volume 16, Issue 2 Ser. II (Mar. – Apr. 2021), PP 07-11
www.iosrjournals.org

Border trap densities in metal-insulator-semiconductor devices and their correlation in Si and 4H-SiC devices

Dr. Ravi Kumar Chanana
Self-Employed Independent Researcher, Gr. Noida, India
Corresponding author: Dr. Ravi Kumar Chanana.

Abstract: *Border traps or near-interface traps in the amorphous insulator such as thermal silicon dioxide or silicon nitride near the semiconductor conduction band of a metal-insulator-semiconductor device are known to limit the field effect mobility of a field-effect-transistor. Border trap densities in thermal silicon dioxide grown on silicon semiconductor at different high and low temperatures have been calculated at 300K by a new method proposed by the author in an earlier study. The border trap density in the oxide grown on silicon at high temperature with no annealing is found to correlate to the border trap density in oxide on 4H-SiC by a factor of three before nitridation. The new method used for the calculations of the trap densities is based on the concept of displacement current due to a changing electric field across a capacitor. It is put forth in a concise manner in the theory section of the article.*

Keywords: *Border Trap, Displacement Current, Metal-Oxide-Semiconductor, Silicon, Silicon Carbide.*

Date of Submission: 20-03-2021 Date of Acceptance: 04-04-2021

I. Introduction

The border traps or near-interface traps find their origin in specifically the oxygen vacancy defect within 3 nm of the Si/SiO_2 interface in the oxide of a metal-oxide-semiconductor (MOS) device. The border traps lie near the conduction band (CB) of Si or some other semiconductors such as 4H-SiC and GaN, and communicates with the semiconductor by trap to trap tunnelling process upon application of an ac signal across the device. They are inside the oxide and are thus different from the interface traps which are right at the interface of Si and SiO_2. They are important to be studied and their densities determined, as their high densities can limit the achievable high field effect mobility in a MOSFET device. The evidence of 1/f noise in Si MOSFETs to be caused almost entirely by the near-interface traps in the oxide called "Border Traps" led to the recommendation that the border trap density denoted by D_{bt}, be included in the original nomenclature of oxide charges in a MOS device associated with the thermally oxidised silicon, thus revising the original nomenclature [1, 2]. Border traps can exist in other insulators as well such as silicon nitride or aluminium oxide making it a feature of metal-insulator-semiconductor (MIS) system. Referring back to the MOS device, a charge trapping model was developed that correlated the border trap density to the 1/f noise in the linear region of the MOSFET channels [3-5] and is used to estimate the border trap density in Si, Ge, and 4H-SiC MOSFETs before and after irradiation [6-7]. Some other methods of finding the border trap densities also exists such as the hysteresis in the drain current of a field-effect-transistor (FET) [8], and the charge pumping method extended to low frequencies of less than 100 Hz [9]. In this method, a train of pulses at various frequencies is applied at the gate of a MOSFET and the charge pumping current through the source and drain is measured obtaining contributions due to the interface traps and the border traps. A low-frequency C-V technique also exists in which the near-interface traps respond to low frequency of less than a 1000 Hz and create a "hump" in the C-V plot of an MIS device as the near-interface trap capacitance adds to the semiconductor capacitance along with the interface trap capacitance in inversion [10]. Recently, the author has found a new method of finding the border trap density by observing the low-field leakage current in a MOS device in accumulation or inversion in which a low ac conductance is observed at low frequency due to the border traps in the oxide near the silicon, 4H-SiC or GaN conduction band (CB) [11-16]. The method is very simple with a simple calculation based on the concept of displacement current introduced by James Clerk Maxwell around the year 1865 in his fourth equation and used regularly in MOS studies to obtain current-voltage characteristics. It does not require a MOSFET device, but only a MOS device. The border trap density found by this method by the author in 4H-SiC MOS device match with those found by Zhang et al. by the 1/f noise method [11], thus enhancing credibility in this new method.

In this research paper, the border trap density is determined in the Si MOS devices where the thermal oxides have been grown in the temperature range of 750°C to 1200°C. The low-field leakage currents at the onset of FN tunnelling current or below have been observed in these devices from the previous research papers

and the border trap densities are determined by the new method. They are then tabulated in Table I. The border trap densities in Si-MOS devices are then correlated with those in the 4H-SiC MOS device.

II. Theory

The new method of determining the border trap density in Si, 4H-SiC or GaN MOS devices is based on the observation of low ac conductance at low frequency of 0.1 V/s in an oxide with border traps, given that the oxide is not having too many bulk traps so as to be called a 'leaky' oxide. The 0.1 V/s ramp rate represents an ac signal of 0.32 Hz of a peak 50mV small sinusoidal signal. The border traps are dominant at the low frequencies of less than a 100 Hz [9]. The 0.1 V/s ramp rate is chosen because the high frequency (1MHz) C-V plot shows all the minority carriers (electrons) responding to this ramp rate and causing inversion in the p-Si-MOS device [12, 17]. This means that the quasi-static C-V plot for the same device at 0.1 V/s ramp rate will show accumulation capacitance in inversion. The oxide displacement current can therefore be obtained by multiplying the oxide capacitance per unit area by the 0.1 V/s ramp rate. It is also shown that the leakage current in a p-type 4H-SiC-MOS device in accumulation also represents the oxide displacement current at this ramp rate [11]. The observed leakage current in an n-type 4H-SiC-MOS device in accumulation or a p-type Si-MOS device in inversion is having the traps near the semiconductor CB filled with electrons imposing a large resistance to the electron current from the cathode [11-13]. The border traps capacitance is in series with the oxide capacitance. The total observed capacitance is obtained by dividing the observed leakage current by 0.1 V/s ramp rate using the formula for the displacement current. The conductance due to the oxide is subtracted from the total observed conductance to give the conductance due to the border traps from which the trap capacitance is obtained using the formula of the displacement current. The trap capacitance is then converted to the border trap density per eV at 300K or any other temperature by dividing the per unit area capacitance by (q(kT)). This theory is discussed next.

The three simple formulas used in this new method of finding the border trap density in the oxide of a MOS device are the formula for the displacement current density, the per unit area capacitance for the border traps, and the formula for the border trap density per unit area and per unit eV at a given temperature. They are as follows:

$$J = C\frac{dV}{dt} \qquad (1).$$

$$\frac{1}{C_{bt}} = \frac{1}{C_{obs}} - \frac{1}{C_{ox}} \qquad (2).$$

$$D_{bt} = \frac{C_{bt}}{q(kT)} \qquad (3).$$

Here, J is the current density in A/cm^2, C is the capacitance per unit area in F/cm^2, dV/dt is the voltage ramp-rate which is taken as 0.1 V/s, C_{bt} is the per unit area border trap capacitance in F/cm^2, C_{obs} is the per unit area observed capacitance in F/cm^2, C_{ox} is the per unit area oxide capacitance in F/cm^2, D_{bt} is the border trap density in cm^{-2}eV^{-1}, k is the Boltzmann's constant in J/K, q is the electron charge in Coulombs, and T is the temperature in Kelvin. The ramp rate of 0.1 V/s approximates to an equivalent low frequency of 0.32 Hz for a 50 mV peak ac signal. This is shown below. An ac signal is given and processed as:

$$V = V_m Sin(\omega t)$$

$$\frac{dV}{dt} = \omega V_m Cos(\omega t)$$

Since the maximum value for $Cos(\omega t)$ =1, therefore by taking, V_m = 50 mV

0.1=0.05 x 2π x f

f = (1/π) = 0.32 Hz.

Here, V_m is the peak amplitude of a sinusoidal signal, ω is the angular frequency in radians/s and is equal to 2πf , with f as the linear frequency in cycles per sec called Hz. Dividing equation (2) throughout by dV/dt, the equation (2) can be written as follows:

$$\frac{1}{J_{bt}} = \frac{1}{J_{obs}} - \frac{1}{J_{ox}} \qquad (4).$$

Here, J_{bt} is the displacement current density for border traps, J_{obs} is the total observed displacement current density and the J_{ox} is the oxide displacement current density. J_{obs} less than J_{ox} indicates the presence of border traps and J_{obs} greater than J_{ox} indicates the presence of bulk traps that results in a 'leaky' oxide [11]. These current densities are respective measures of the ac conductance per unit area at low frequency for a given voltage as shown next starting with equation (1) and then substituting for dV/dt.

$$J = C\frac{dV}{dt}$$

$$J = C\omega V_m Cos(\omega t)$$

$$\frac{J}{V_m} = \omega C \qquad (5).$$

The equation (5) is obtained for a maximum value of 1 of the Cos (wt) used in approximating the ramp signal. This is the ac conductance per unit area as the inverse of the magnitude of the impedance offered by the capacitance. Thus, the obtained current densities in a MOS device in accumulation or inversion are a measure of the ac conductance per unit area for a given voltage. The obtained current density of J_{bt} from equation (4) when divided by the 0.1 V/s ramp rate gives the C_{bt} per unit area using equation (1) and then the density of border traps D_{bt}, can be calculated using equation (3) at a given temperature T in Kelvin. The oxide displacement current density can be obtained with the knowledge of the oxide thickness using the formula as:

$$J_{ox} = \frac{\varepsilon_0 \varepsilon_r}{d}(0.1) \qquad (6).$$

Here, ε_0 is the free space permittivity as 8.854 x 10^{-14} F/cm, ε_r is the relative permittivity of the dielectric which for the SiO_2 is 3.9, and d is the thickness of the oxide in cm and dV/dt is taken as 0.1 V/s. The above equation (6) has been used to calculate J_{ox} for a given oxide thickness d.

III. Results and Discussions

The border trap densities are calculated for thermal oxides grown on silicon semiconductor at different temperatures from 750°C to 1200°C and presented in Table I below. The equation (4) of the theory section is used to calculate the current density due to border traps given as J_{bt} following which the C_{bt} is calculated for 0.1 V/s ramp rate using equation (1). The border trap density D_{bt} at 300K is finally calculated using equation (3). It can be observed from the Table I below, that high temperature oxidation of Si (1000°C to 1200°C) creates border traps density of 4 x 10^{11}/cm^{2}eV at 300K, with no anneal after metallization. Oxidation at 1000°C followed by e-beam evaporated metal causes radiation damage in terms of creating electron traps in the oxide [18]. 5 min PMA performed at 500°C in dry N_2 not only anneals the radiation damage, but also reduces the border trap density to 2 x 10^{11}/cm^{2}eV. Therefore, if the PMA was not performed, then the border trap density would have been 4 x 10^{11}/cm^{2}eV as in the oxide grown at 1150°C or 1200°C. Low temperature oxidation of Si at 850°C or less creates border trap density in the low 10^{12} order at 300K. It is further observed that a post-oxidation annealing (POA) in dry N_2 at 900°C or 1000°C for 30 min reduces the border trap density. Post-metallization annealing (PMA) at 500°C for 10min also reduces border trap density. POA also affects the bulk oxide by creating traps believed to be oxygen vacancy defects [19, 20].

During the I-V measurements in Osburn and Weitzman's study, the applied field is cycled between low and high fields many times before the I-V curves for the increasing and decreasing fields coincide. It is to be noticed that the low field leakage current or the current at the onset of FN tunnelling does not change by this cycling [21]. This current is used to determine the border trap density which therefore remains unchanged before and after cycling the fields. Lenzlinger and Snow also stressed their device at 10^{-10}A/cm^2 for 2 hrs during which time the current decreased by about one order of magnitude [22]. From the study of Osburn and Weitzman, it is clear that the low-field leakage current or the current at the FN onset would not have changed for the devices in the study by Lenzlinger and Snow also. This is the current that is used to determine the border trap density and so the border trap density remains unaffected due to this stressing. The border traps communicate with the Si CB by capturing and emitting without retaining the charge permanently, unlike other electron traps in the bulk of the oxide. Therefore, the cycling of low and high fields and stressing does not affect the low-field leakage current due to the border traps.

Si-O-O-O is the border trap (E' centre) in Si/SiO_2 MOS and Si-C-O-O could be the border trap (E' centre) in 4H-SiC/SiO_2 MOS before nitridation giving border trap density of 12 x 10^{11}/cm^{2}eV, a three times change from Si-MOS due to presence of a Carbon atom which has 2 less electrons than an Oxygen atom [13]. After nitridation with NO, one N is believed to replace one O forming Si-C-O-N or Si-N-N-N at the interface giving border trap density of 24 x 10^{11}/cm^{2}eV, because N has one less electron than Si-C-O-O doubling the density [13, 23]. Thus, the border trap density in 4H-SiC-MOS correlate with those in Si-MOS by a factor of

three before nitridation. The fixed charges have also been shown to be correlated in Si and 4H-SiC MOS devices before nitridation by a factor of three [15].

Table I. Border trap densities calculated in thermal oxides grown on Silicon at different temperatures.

Reference	Oxidation Conditions for the thermal oxide	Annealing condition	Oxide thickness (nm)	Oxide displacement current density for 0.1 V/s ramp rate, J_{ox} (A/cm^2)	Observed Low-field Leakage current density at the onset of FN tunnelling, J_{obs}, (A/cm^2)	C_{bt} for 0.1 V/s ramp rate from J_{bt} (F/cm^2)	D_{bt} at 300K ($x\ 10^{11}$) ($cm^{-2}eV^{-1}$)
Lenzlinger and Snow J. Appl. Phys., 40(1)278, 1969.Fig.5 (Si)	1200°C dry O_2 on n-type Si-wafer, probably <100>, e-beam evaporated metal	No PMA after metallization that could reduce BT density also.	100	34.53×10^{-10}	1.5×10^{-10}	1.6×10^{-9}	4 (No anneal)
B.P. Rai, K. Singh and R.S. Srivastava, Phys. Stats Solidi (a), 36, 591, 1976, Fig.1 and 2.	1150°C dry O_2 on n<111>Si surface, vacuum evaporated metal.	No PMA after metallization.	150	230×10^{-11}	1.5×10^{-10} (No anneal) 7×10^{-11} (10min 500°C N_2 PMA) 5×10^{-11} (30min 1000 ^{0}C dry N_2 POA)	1.6×10^{-9} (No anneal) 7.2×10^{-10} (10min 500°C N_2 PMA) 5.11×10^{-10} (30min 1000°C dry N_2 POA)	4 (No anneal) 1.8 (10min 500°C N_2 PMA) 1.25 (30min 1000°C dry N_2 POA)
Osburn and Weitzman J. Electrochem. Soc., Solid-State Sci. Tech., 119(5)603, 1972.Fig.8(b)	1000°C dry O_2 on n-type <100> Si-wafer with Al(+), e-beam evaporated metal	5 min PMA at 500°C in dry N_2 after metallization to remove radiation damage. PMA also reduces BT density	140	250×10^{-11}	8×10^{-11} (No further anneal) 3×10^{-11} (Further 10min 500°C N_2 PMA)	8×10^{-10} (No further anneal) 3×10^{-10} (Further 10min 500°C N_2 PMA)	2.0 (No further anneal) 0.8 (Further 10min 500°C N_2 PMA)
Krieger and Swanson J. Appl. Phys. 52(9)5710, 1981.Fig.6	850°C 99.5%O_2-0.5%HCl on n-type <100> Si-surface, e-beam evaporated Al	Ar anneal as POA at 850°C for 30 min. Forming gas PMA for 10min at 400°C.	7 C-V dot area of $2.27x10^{-4}$ cm^2	493×10^{-10}	10^{-13} A/(2.27 x 10^{-4} cm^2) = 4.4 x 10^{-10} A/cm^2	4.4×10^{-9}	11
Scarpa et al., IEEE Trans. On NS-44(6)1818, 1997, Fig.1	750°C wet oxidation, p-Si with positive gate voltage, N+ poly-Si gate.	900°C N_2 anneal as POA	4.4 C-V dot area 10^{-3} cm^2	78×10^{-9}	10^{-9}	10^{-8}	25
	Since BTs are in the oxide, the Si surface orientation does not matter.						

The low ac conductance due to border traps in n-4H-SiC MOS device near the CB gives a low current that can be converted to a voltage with the help of a trans-resistance amplifier (OPAMP based) and the higher leakage current in the p-4H-SiC MOS device not having border traps near the VB can be converted to higher voltage similarly. The low and the high voltages can act as '0' and '1' needed for a memory device. Since the observed current is at low voltage less than the field causing electron heating in the SiO_2 of 2 MV/cm, the memory can be reliable. The speed of such a memory device may be limited by the slew rate of the OPAMP based trans-resistance voltage amplifier that converts the observed current to voltage. The memory may work at high temperatures as well.

IV. Conclusions

Three main conclusions are drawn based on the above study on border traps in oxides grown on Si at different high and low temperatures. First, SiO_2 grown on Si at high temperatures of 1000°C to 1200°C followed by no annealing have a border trap density of 4 x 10^{11}/cm^2eV. The low temperature oxides grown at 850°C and 750°C give a border trap density in low 10^{12}/cm^2eV order. Second, post-metallization annealing at 500°C and post-oxidation annealing at about a 1000°C, both in inert atmosphere of N_2 or Ar reduces the border traps density by more than two to three times, with post-oxidation annealing also affecting the bulk oxide. Third, the border trap and fixed oxide charge densities in Si and 4H-SiC MOS systems are correlated by a factor of three before nitridation because of the presence of at least one Carbon atom in the oxide traps in 4H-SiC-MOS which has two less electrons than an Oxygen atom. The low 10^{12} order border trap densities after nitridation limit the field effect mobility in 4H-SiC power MOSFETs having a high oxide breakdown to 35 to 45 cm^2/V-s and the same is expected in GaN power MOSFETs which show similar border trap density. A high temperature memory device is possible on 4H-SiC due to the border traps in the 4H-SiC-MOS device.

References

[1]. B.E. Deal, "Standardized terminology for oxide charges associated with thermally oxidised silicon", IEEE Trans. On Electron Devices, 1980;27(3):606-608.
[2]. D.M. Fleetwood, ""Border Traps" in MOS Devices", IEEE Trans. On Nuclear Science, 1992;39(2):269-271.
[3]. J.H. Scofield, T.P. Doerr, D.M. Fleetwood, "Correlation between preirradiation 1/f noise and postirradiation oxide-trapped charge in MOS transistors", IEEE Trans. On Nuclear Science, 1989;36:1946-1954.
[4]. D.M. Fleetwood, J.H. Scofield, "Evidence that similar point defects cause 1/f noise and radiation-induced hole trapping in metal-oxide-semiconductor transistors", Physical Review Letters, 1990;64(5):579-582.
[5]. D.M. Fleetwood, P.S. Winokur, R.A. Reber Jr., T.L. Meisenheimer, J.R. Schwank, M.R. Shaneyfelt, L.C. Riewe, "Effects of oxide traps, interface traps, and "border traps" on metal-oxide-semiconductor devices", J. Appl. Phys. 1993;73(10):5058-5074.
[6]. C.X. Zhang, S.A. Francis, E.X. Zhang, D.M. Fleetwood, R.D. Schrimpf, K.F. Galloway, E. Simoen, J. Mitard, C. Claeys, "Effect of ionizing radiation on defects and 1/f noise in Ge pMOSFETs", IEEE Trans. On Nuclear Science, 2011;58(3):764-769.
[7]. C.X. Zhang, X. Shen, E.X. Zhang, D.M. Fleetwood, R.D. Schrimpf, S.A. Francis, T. Roy, S. Dhar, Sei-Hyung Ryu, S.T. Pantelides, "Temperature dependence and postirradiation annealing response of the 1/f noise of 4H-SiC MOSFETs", IEEE Trans. On Electron Devices, 2013;60(7):2361-2367.
[8]. K.N. ManjulaRani, V. Ramgopal Rao, J. Vasi, "A new method to characterize border traps in submicron transistors using hysteresis in the drain current", IEEE Trans. On Electron Devices, 2003;50(4):973-979.
[9]. R.E. Paulsen, M.H. White, "Theory and application of charge pumping for the characterization of Si-SiO_2 interface and near-interface oxide traps", IEEE trans. On Electron Devices, 1994;41(7):1213-1216.
[10]. N.L. Cohen, R.E. Paulsen, M.H. White, "Observation and characterization of near-interface oxide traps with C-V techniques", IEEE Trans. on ED, 1995; 42(11): 2004-2009.
[11]. R.K. Chanana, "An interrelated current-voltage/capacitance-voltage traces based characterisation on 4H-SiC metal-oxide-semiconductor devices in accumulation and Si device in inversion along with derivation of the average oxide fields for carrier tunnelling from the cathode and the anode", IOSR-JEEE, 2019;14(3):49-63.
[12]. R.K. Chanana, "Issues in current-voltage/capacitance-voltage traces-based MIS characterisation that improves understanding for a better design of n-channel MOSFETs on Si and SiC", IOSR-JEEE, 2019:14(3): 1-9.
[13]. R.K. Chanana, "High density of deep acceptor traps near the 4H-SiC conduction band limits surface mobility and dielectric breakdown field in an n-channel 4H-SiC MOSFET", IOSR-JEEE, 2019;14(4):1-8
[14]. R.K. Chanana, "Correlated positive charges and deep donor and acceptor "Border" traps in Si and 4H-SiC MOS devices", IOSR-J. Electrical and Electronics Engineering, 2019; 14(4):49-55.
[15]. R.K. Chanana, "The intertwined features of trap charges and surface mobility in the MOS and MOSFET devices fabricated on elemental silicon and compound semiconductors such as silicon carbide and gallium nitride", IOSR-JEEE, 2019;14(5):52-64.
[16]. R.K. Chanana, "Electron diffusion current after ionisation of thermal silicon dioxide in a MOS device forms the Fowler-Nordheim electron tunnelling current showing wave-particle duality of electrons", IOSR-Journal of Appl. Phys., 2021;13(1):5-9.
[17]. P.S. Winokur, J.R. Schwank,, P.J. McWhorter, P.V. Dressendorfer, D.C. Turpin, "Correlating the radiation response of MOS capacitors and transistors", IEEE Trans. On Nuclear Science, 1984;31(6):1453-1460.
[18]. Tak H. Ning, "Electron trapping in SiO_2 due to electron-beam deposition of aluminium", J. Appl. Phys., 1978;49(7):4077-4082.
[19]. B.P. Rai, K. Singh, R.S. Srivastava, "Current transport phenomena in SiO_2 films", Phys. Stat. Sol.(a),1976;36:591-595.
[20]. P. Balk, M. Aslam, D.R. Young, "High temperature annealing behavior of electron traps in thermal SiO_2", Solid-State Electronics, 1984;27(8-9):709-719.
[21]. C.M. Osburn, E.J. Weitzman, "Electrical conduction and dielectric breakdown in silicon dioxide films on silicon", J. Electrochem. Soc.,Solid-State Science and Technology, 1972;119(5):603-609.
[22]. M. Lenzlinger, E.H. Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2", J. Appl. Phys.,1969;40(1):278-283.
[23]. R.K. Chanana, "Notes on interface traps in 4H-Silicon Carbide metal-oxide-semiconductor devices", IOSR-J. Electrical and Electronics Engg.,2020;15(5):36-39.

Dr. Ravi Kumar Chanana. "Border trap densities in metal-insulator-semiconductor devices and their correlation in Si and 4H-SiC devices." *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)*, 16(2), (2021): pp. 07-11.