IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 13, Issue 4 Ver. II (Jul. – Aug. 2018), PP 01-04
www.iosrjournals.org

Design and Implementation of 32-Bit Magnitude Comparator Using Full Adder

Raman Shrivastav[1], Shweta Agrawal[2],
[1]*M.Tech Scholar, SRCEM Gwalior, India,*
[2]*Assistant Professor, SRCEM Gwalior,India,ershwetaagrawal*
Corresponding Author: Raman Shrivastav

***Abstract**: In today's life VLSI plays vital role for low power consumption, small area and fast response of the electronic devices. Here 32-bit magnitude comparator is designed taken into account of low power, small area and less delay. For this novel magnitude comparator designing full adder is used .Full adder gives two outputs sum and carry which is equivalent to the output of comparator 's equal and smaller respectively.*
Keywords— area, comparator, full adder, low power, Verilog, Xilinx

---

Date of Submission: 09-07-2018 Date of acceptance: 23-07-2018

I. Introduction

The Magnitude comparator is the main part of any procesor,hence the speed of comparator affects the speed of procesor.To maintain the speed and other design paramters here proposed the magnitude comparator which uses full adder to genrate their outputs smaller and equal,this design reduces the relative complexity of conventional comparator design. Following subsection first introduces the proposed comaprator architecture followed by complexity analysis.

II. Proposed Comparator Architecture

The architecture of the proposed comparator is shown in Figure 4.1. The proposed comparator is implemented using full adder which genrates outputs sum and carry that is equal to equal and smaller signal respectively.
The outputs equal and smaller is used further used to generate greater signal.

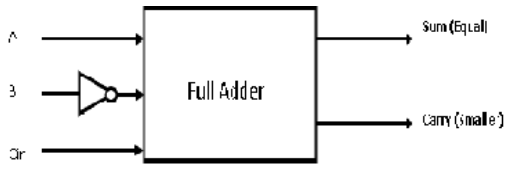

Figure 2.1 Architecture of the proposed comparator.

It is observed in the literature that complexity in terms of area, power and delay are more for greater and smaller over the equal. Therefore, we introduces comparator as shown in Figure 4.1 which computes equal and smaller inplace of greater and equal. The equal and smaller signal are further used to generate the greater signal. Here fulladder is used to obtain the desired results .For full adder there are three inputs A,B and Cin which is pervious carry . A input is taken as its original value and B input is taken as the complement of B and C perivous carry which will be always high.

A. 4-bit Magnitude comparator

To explain how it will work lets take the example in which A and B are 4-bit numbers to be compared. There will be three casaes of comparision :
(i)A >B
(ii) A=B
(iii) A<B
Case (i) A=9 and B=6
A=9 and B=6 convet this decimal number into its binary equvalient numbers A will be "1001" and B will be "0110". Input Cin will be always high ie. '1'.
Now take 1's complement of B ie.1001 know add A,B'and C we get
1001

10011
10011
Here Cout is '1' and sum is non zero.
Case (ii) A=9 and B=9
A=9 and B=9 convet this decimal number into its binary equvalient numbers A will be "1001" and B will be "1001". Input Cin will be always high ie. '1'.
Now take 1's complement of B ie.0110 know add A,B'and C we get
1001
01101
1000
Here Cout is '1' but sum is '0'.

Case (iii) A<B
A=6 and B=9 convet this decimal number into its binary equvalient numbers A will be "0110" and B will be "1001". Input Cin will be always high ie. '1'.
Now take 1's complement of B ie. 0110 know add A,B'and C we get
0110
0110
1
1001
Here cout is zero .
From the above calculations it is observed that if :
(i)Cout is '1' then it concludes that A>B.
(ii) Cout is '1' and sum is '0' it concludes that A=B.
(iii) Cout is '0' it concludes that A<B.
According to the conclusions comparator is designed ,that computes equal and smaller signal.
In order to figure out the performance of the proposed architecture over the existing and proposed designs are implemented in Verilog. Further, 4-bit comparator are designed using different techniques and these four bit comparators are utilized to design 32-bit comparators which are simulated and compared over the proposed comparator architecture.

III. Simulation Results and analysis

The proposed 32-bit magnitude comparator using full adder is designed and implemented on Xilinx 12.1 tool and the design is simulated using ISim simulator.The design is coded in Verilog HDL and the functional verification is done with help of test bench .The following figure shows schematic of 32-bit magnitude compartor using full adder.

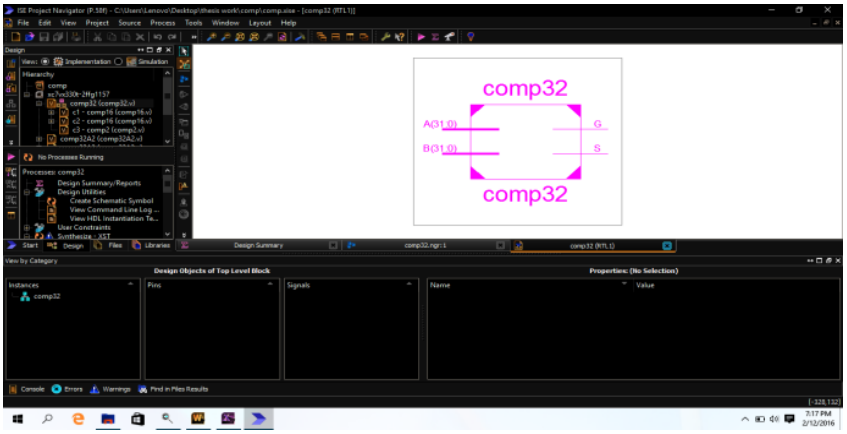

Figure 3.1 Top module of 32-bit magnitude comparator

The above figure shows the top module of the design. Detailed architecture of 32 –bit magnitude comparator is shown below:

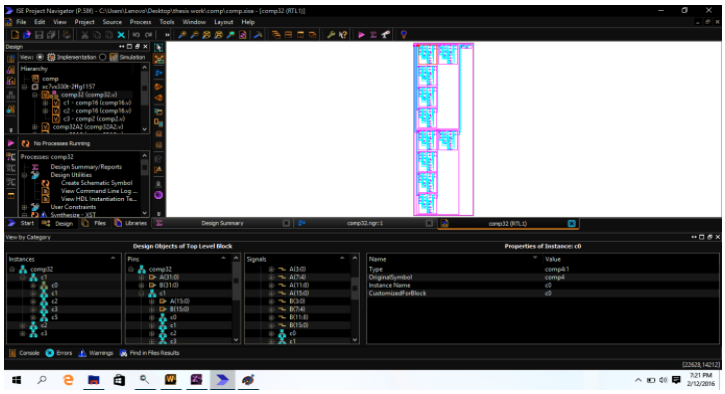

Figure 3.2 Detailed view of 32-bit magnitude comparator

The simulated waveforms are represented as follows

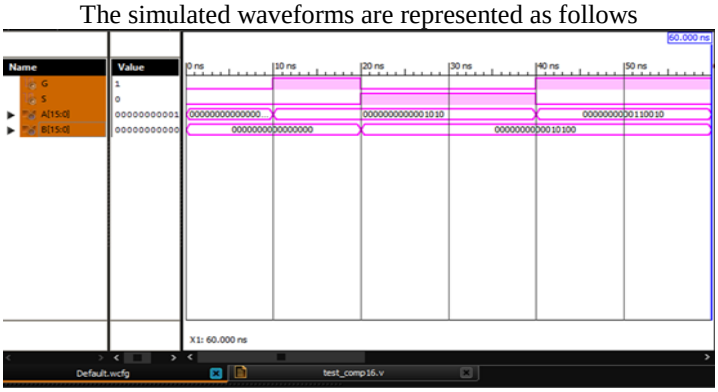

Figure 3.2 Output Waveforms of 32-bit magnitude comparator

Table 3.1 comparison of types of comparator

Technique Comparator	Area (#LUTs)	Delay (nS)	Power (mW)
Priority Based	32	4.94	163
Look-ahead	31	5.84	168
Proposed	32	5.23	151

From the table the following graph is obtained, which shows the area, delay and power of different comparators.

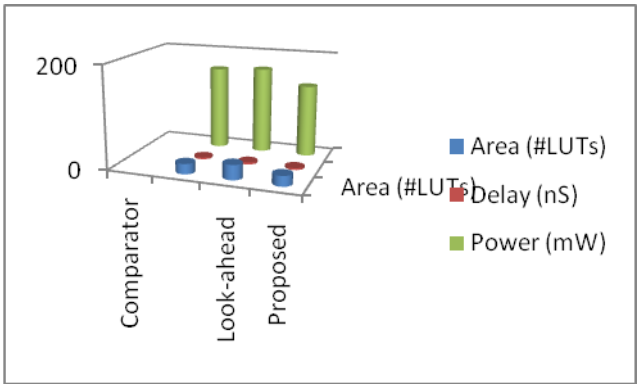

Figure 3.3 Design parameters of different comparators.

IV. Conclusion

From the result obtained it clear that the proposed 32- bit magnitude comparator is best among all the mentioned comparators. The power consumption is lowest. The proposed comparator requires 7.2% and 11.2 %, reduced power consumption over Priority based and Look-ahead comparator architectures respectively.The area is measured in terms of number of (Look Up Tables) LUTs which reflects the required combination logic to implement the desired logic.

References

[1]. M. Morris Mano, Digital Logic and Computer Design.
[2]. T.Suryakalas, B. Swaroopa, Bhaskara Rao Doddi,"Circuit Design of Low area 8-bit magnitude Comparator With Low Power by Static CMOS", International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Vol. 4, Issue 10, pp 3982-86, October 2015.
[3]. Anjuli and Satyajit Anand, "2-Bit Magnitude Comparator Design Using Different Logic Styles", International Journal of Engineering Science Invention, Vol.2 ,Issue 1 , pp.13-24,January 2013.
[4]. Geetanjali Sharma, Uma Nirmal, and Yogesh Misra, "A Low Power 8-bit Magnitude Comparator with Small Transistor Count using Hybrid PTL/CMOS Logic" ,IJCEM International Journal of Computational Engineering & Management, Vol. 12, pp 110-115,April 2011.
[5]. Oguz Ergin, Kanad Ghose, Gurhan Kucuk, and Dmitry Ponomarev, "A Circuit–Level Implementation of Fast, Energy–Efficient CMOS Comparators for High–Performance Microprocessors",in IEEE International Conference on Computer Design: VLSI in Computers and Processors (ICCD'02), pp. 115-118,2002.

IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) is UGC approved Journal with Sl. No. 4198, Journal no. 45125.

Raman Shrivastav "Design and Implementation of 32-Bit Magnitude Comparator Using Full Adder." IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) 13.4 (2018): 01-04.