# Dynamic Reconfiguration of Analog VLSI System: A Review

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***Abstract:*** *Dynamic reconfigurable system came in to limelight in the current generation of VLSI design. Till now area, performance, cost and power are the priorities of design engineers overlooking the Multifunctionality of a single system design. Many researchers are focused on digital VLSI system as compared to the analog VLSI system, it is because of digital system is highly atomized and number of testing hardware and software platforms are available Also very few parameter are sensitive to input as compare to the analog system design. In this paper general concept of dynamic reconfiguration for various analog system design and application is illustrate*

***Keywords-Analog***, *Digital, Reconfigurable FPGA, FPAA, VLSI.*

## I. Introduction

As VLSI system solutions dominate the area of research in digital circuits but analog integrated circuits are also important in modern electronic systems. Analog circuits and systems also plays a very crucial role in interfacing digital system in many real world application such as analog signal processing and conditioning, industrial process and motion control, monitoring and control, wireless communications, biomedical measurements etc. The application where compactness and low power consumption is required, analog circuitry is a solution. The process of design, fabrication, and testing of analog module and circuit chip needs an experts, good practice, costly, and is time consuming.

Now a day's Dynamic reconfigurable digital and analog systems are a key component in the dedicated, embedded computing and communication systems. The dynamic reconfiguration method provides the adaptability to a computation required at any given instant of time. This higher adaptability is useful in the systems of high processing requirements, and system should be adaptable, centrally controlled and reconfigured, such as smart TV set-top boxes.

But as it is observed when analog and Digital circuit are combined at one platform and reconfigure according to the system requirement there are many problems arises due the flow of analog and digital system is different and analog system is more sensitive to parameter variations as compare to digital systems. Figure no. 1 depicts typical flow of digital and analog system.
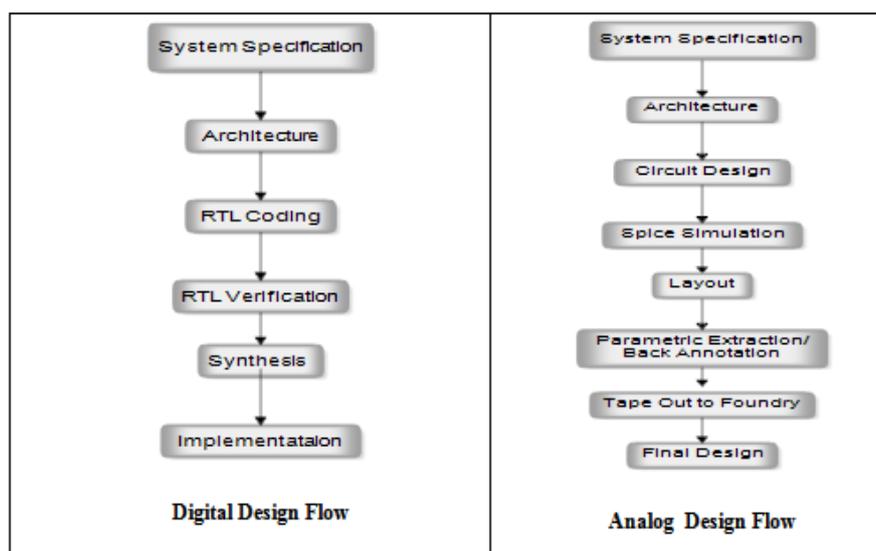
## II. Analog System Reconfiguration Systems & Types

Kush Gulati (2001) described the low-power CMOS reconfigurable analog-to-digital converter that can digitize signals over a wide range of bandwidth and resolution with adaptive power consumption. The converter achieves the wide operating range by reconfiguring its architecture between pipeline and delta–sigma modes, varying its circuit parameters, such as size of capacitors, length of pipeline, and oversampling ratio, among others and varying the bias currents of the opamp in proportion to the converter sampling frequency, accomplished through the use of a phase-locked loop (PLL). An author proposes the idea of a single converter that can morph itself into different topologies to cover the desired continuum of resolution and bandwidth space with minimum power at each performance level. The proposed converter is designed to provide a significantly larger reconfigurability space [1].

Rapid prototyping of analog systems is not completely analogous to its digital counterpart. Developing robust, programmable analog circuits presents a number of challenges not found in the digital world. In particular, the noise sensitivity (and effects of the switch network on the results of the computation) and the design space to which programmable devices are applicable are more critical factors in designing Field Programmable Analog Arrays (FPAAs). Systems implemented on these FPAAs are demonstrated to be programmable over a wide range of frequencies, Q-peaks, bandwidths, and/or time constants. With orders of magnitude power consumption savings over traditional digital approaches, this reconfigurable analog technology offers an attractive alternative for implementing advanced signal processing systems in low-power embedded systems. Currently available commercial and academic FPAAs are typically based on operational amplifiers [4].

Daihong Fu, Kenneth C (1998) describe the digital background calibration is of potential interest to reduce the effects of mismatch in time interleaved analog to digital converters. Since the calibration is done in the digital domain here, the overhead required in terms of area and power dissipation to implement monolithic background calibration is expected to scale dramatically in scaled technologies [9].

A dynamically reconfigurable mixed-signal circuit using the new technology of Field Programmable Analog Arrays (FPAA) combined with existing well established technology of Field Programmable Gate Arrays (FPGA). A FPAA can be used to build filters for analog signals as well as other kinds of analog applications implemented in switched capacitor technology (S/C-technology). The experiment described in this paper takes advantage of performance and programmability of the FPAA for filtering of an analog signal controlled by a digital system. Investigations of such hardware in application to adaptive signal filtering and process control are in progress. The paper will present results of work on adaptive filtering with dynamic reconfiguration based on 2 parallel FPAA chips cooperating with a digital control system. Theoretical studies and measurements of transition behavior of the switching process between the 2 FPAA chips and analysis of limitations imposed by hardware imperfections will be presented [12].

Ramesh K. Pokharel (2009) employed a switching transistor concept between two inductors for dual-band operation of the oscillator and the switching operation is controlled by a digital signal. Furthermore, operation of the capacitor banks is fully controlled by 10 bits digital signals so that the oscillator becomes fully digitally controlled. As proposed system consume very high power and for future generation multi standard wireless transreceivers, is therefore necessary to implement and integrated with the complete system with digitally assisted approaches [14].

Tuning tank used to realize a frequency range between 3.25 GHz and 4.25 GHz bands is a binary weighted capacitor tank which is controlled by the 10-bit coarse tuning data [18].

## III. Conclusion

Lots Of Analog System Architecture Has Been Proposed By The Authors Which Uses Different Methods Like Pipeline, Delta Sigma, Adjustable Bias Current, R/2r, Ladder, Analog Switch Array, Digitally Tunable Capacitor Array. By These Methods The Single Circuit Is Reconfigured For Different Modes Of Example Filter Of Two Frequencies, ADC With Different Configuration, Multistage Power Amplifier, VCO Etc. But As VLSI World Move Fast So There Is Be Develop A Technology Where Single Analog Chip Which Can Dynamically Reconfigured For Different Circuits Like Digital Chip. The Chip Can Perform A Multifunction With Single Chip With All Analog Parameter Considering By Using Simple Reconfiguring The Switches.

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