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Design of A Low Power Dissipation Bandgap Voltage Reference Without Resistors

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***Abstract**: With the development of portable electronics, low power dissipation have become the main direction of current chip research, because Bandgap Reference (BGR) circuits are widely used in modern LSIs to generate a reference voltage on chips, So this paper presents a low power and low temperature coefficient bandgap voltage reference that employs the proportional to absolute temperature (PTAT) voltage generator circuit based on overdrive voltage differences. The BGR circuit consists of MOSFET and bipolar transistor without resistors. The simulated results are verified by Cadence Spectre.The simulated results based on the Magnachip 0.18μm CMOS process demonstrate that the BGR's temperature coefficient is 22.44ppm/℃at a temperature range from -40℃to 140℃when power voltage is 0.95V. The PSRR is -50.4023dB at 100Hz, -13.2811dB at 10MHz, and the power dissipation at room temperature is only 83nW.*

***Keywords**: overdrive voltage differences; PTAT voltage generator; no resistors; low power; low temperature coefficient*

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I. Introduction

TheBandgapReference circuit is an important part of the power management chip. The BGR can provide a reference voltage for voltage sampling or power voltage regulation circuit which is irrelevant to the power supply and process and has a stable temperature characteristic. As the rapid development of portable electronic devices, the power management chip with low power dissipation has become the hotspot of research. So studying the BGR with low power dissipation becomes more important.

The resistors in traditionalreference circuits [1]-[3] are used to generate current or voltage to control the temperature characteristics of the output reference voltage. Because of the resistors, the power dissipation can hardly be reduced to nW level. Although it can be reduced if we adopt using a large value for resistor, the resistors will occupy a large area of the silicon. A reference voltage source circuit with no resistors and power dissipation of nW level is proposed in documents [4]-[5], and the output reference voltage is based on the threshold of MOSFET. The reference voltage will be affected by the process. A low power dissipation BGR which uses switching capacitors to replace the resistors is proposed in documents [6]. This circuit uses the charge pump to reduce the influence of the power supply. Because the generated PTAT voltage is sensitive to the parasitic capacitance and the output of charge pump, the temperature characteristics of the reference voltage will be affected seriously. In this paper, we employs the PTAT voltage based on MOSFET overdrive voltage differences to compensate the complementary to absolute temperature (CTAT) voltage, and the proposed resistorless BGR has better temperature characteristic and lower power dissipation. The proposed BGR consists of start-up circuit, reference current of nA level circuit, voltage divider and PTAT voltage generators. The simulated results shows the proposed BGR can operate normally as the power supply is less than 1V, and the power dissipation is only 83nW.

II. Design of the bandgap reference circuits

2.1 Characteristic of subthreshold current

When drain-source voltage V_{DS} is lower than threshold voltage V_{TH}, the surface potential is approximately equal to the Fermi potential and there is no conducting channel, these conditions show the MOSFET is in subthreshold region. Because the bias current of MOSFET in subthreshold region is nA level, the BGR can achieve low power dissipation by using MOSFET working in subthreshold region. The subthreshold current *I* is related to the gate-source voltage V_{GS} and drain-source voltage V_{DS}, and can be expressed as:

$$I = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \times \left(1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right) \quad (1)$$

where *K* (=*W*/*L*) is the aspect ratio of a transistor, I_0 (=$\mu C_{OX}(\eta - 1)V_T$) is the process-dependent parameter, μ is

the carrier mobility, C_{OX} (=ε_{OX}/t_{OX}) is the gate-oxide capacitance, ε_{OX} is the oxide permittivity, t_{OX} is oxide thickness, V_T(=k_BT/q) is the thermal voltage,$k_B$is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, and η is the subthreshold slope factor [7]. When V_{DS} is higher than 0.1V, the effect of V_{DS} can be neglected. The equation (1) can be expressed simply as:

$$I = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (2)$$

2.2 The BGR circuit

Figure 1 shows the proposed BGR circuit by four parts: the start-up circuit, the reference current of nA level circuit, the voltage divider and the PTAT voltage generators. The reference current of nA level circuit provides bias current for other parts. Then CTAT voltage V_{CTAT} is divided into $V_{CTAT}/2$ by the voltage divider. Next $V_{CTAT}/2$ is into the PTAT voltage generators. Finally a reference voltage with good temperature characteristic can be obtained, and its value equals the half of bandgap voltage (about 0.6V). The voltage divider can not only operate normally as the power supply is less than 1V, but also reduce the power dissipation and area of this chip.

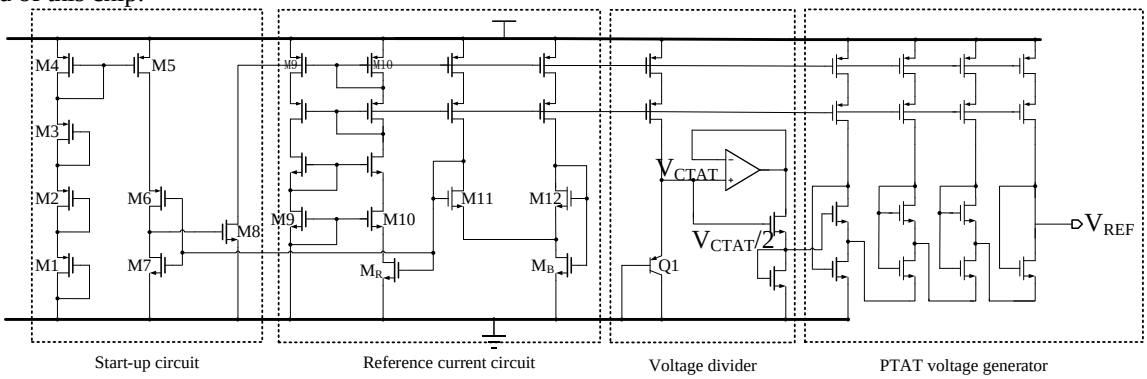


Figure 1. Schematic of proposed BGR circuit

2.3 The reference current circuit

This circuit uses MOSFET $M_R$which operates in deep-triode region to replace resistor, and adopts current mirror of cascade to improve power supply rejection ratio (PSRR). In this circuit, all the MOSFETs are operated in the subthreshold region expect for the nMOS M_R. When M_R operates in deep-triode region ($V_{DS} \ll V_{GS} - V_{TH}$), the drain current of M_R can be expressed as:

$$I_{DS,R} = \beta_{MR}\left(V_{GS,R} - V_{TH}\right)V_{DS,R}, \quad (3)$$

where β_{MR} is the current gain factor of M_R. The voltages $V_{GS,R}$ and $V_{DS,R}$ can be expressed as:

$$V_{GS,R} = V_{GS,B} + \eta V_T \ln\left(\frac{K_{12}}{K_{11}}\right) \quad (4)$$

$$V_{DS,R} = \eta V_T \ln\left(\frac{K_{10}}{K_9}\right) \quad (5)$$

where K_i is the aspect ratio of M_i. In order to reduce the effect of the threshold voltage mismatch due to the different size, channel lengths between transistor pairs (M_R and M_B, M_9 and M_{10}, M_{11} and M_{12}) are designed equally. From (3), (4) and (5), the reference current I_{OUT} can be expressed as:

$$I_{OUT} = \beta_{MR}\eta^2 V_T^2 \ln\left(\frac{K_{12}I_{OUT}}{K_B K_{11} I_0}\right)\ln\left(\frac{K_{10}}{K_9}\right) \quad (6)$$

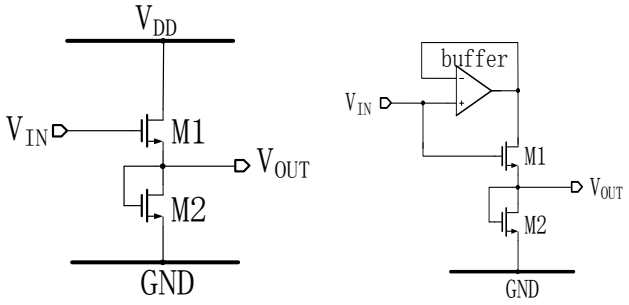
2.4 Voltage divider

Figure 2(a) [9] shows a voltage divider to reduce power supply and power dissipation. And the output voltage is half of the input voltage. The two NMOS M_1 and M_2 have the same aspect ratio, and in order to obtain the same threshold voltage their bulks are connected to the source. Assume the leakage current of gate and substrate are too small to be neglected and the two NMOS both are in subthreshold region, the drain-source current of M_1 and M_2 can be regarded equally, and can be expressed as:

$$I_{DS,M1} = KI_0 \exp\left(\frac{V_{GS1} - V_{TH}}{\eta V_T}\right) \times \left(1 - \exp\left(-\frac{V_{DD} - V_{GS2}}{V_T}\right)\right) \quad (7)$$

$$I_{DS,M2} = KI_0 \exp\left(\frac{V_{GS2} - V_{TH}}{\eta V_T}\right) \times \left(1 - \exp\left(-\frac{V_{GS2}}{V_T}\right)\right) \quad (8)$$

Because V_{GS2} and $(V_{DD} - V_{GS,R})$ are not equal and vary with power supply and temperature, V_{GS1} is not the same as V_{GS2}. Therefore, the V_{OUT} is not exactly equal to the half of V_{IN}.



(a) traditional voltage divider(b) proposed voltage divider

Figure 2. Comparison of voltage divider

In order to improve the stability and decrease the effect of power supply, this article proposes a circuit in Figure 2(b). This circuit inserts a voltage buffer which is a self-bias amplifier between the gate and drain of M_1, and M_1 and buffer form a negative feedback loop to increase the stability and precision of this circuit. In this circuit, the aspect ratio of M_1 and M_2 are both same, and their V_{GS} are equal to their V_{DS}. The simulated results shows V_{GS1} and V_{GS2} are both bigger than 0.1V. Therefore the relation of drain current between M_1 and M_2 can be expressed as:

$$KI_0 \exp\left(\frac{V_{GS1} - V_{TH}}{\eta V_T}\right) = KI_0 \exp\left(\frac{V_{GS2} - V_{TH}}{\eta V_T}\right) \quad (9)$$

So the equation$V_{GS1} = V_{GS2} = V_{CTAT}/2$ is established.

2.5 PTAT voltage generator

The emitter-base voltage V_{EB} of bipolar transistor Q_1 is a CTAT voltage, and can be expressed as:

$$V_{EB} = V_{BGR} - \gamma T \quad (10)$$

where V_{BGR} is the bandgap voltage of the silicon at 0K (about 1.2V) and γ is the temperature coefficient of the V_{EB}.To obtain the reference voltage with better temperature characteristic, the PTAT voltage is needed to compensate the negative temperature dependence of V_{EB}.

The PTAT voltage is generated by a negative feedback loop which contains two bipolar transistors, resistors and a amplifier in the traditional circuits. But this method can increase the area and power of the chip. Figure 3 shows the PTAT voltage generator which consists of two source-coupled pairs [10].

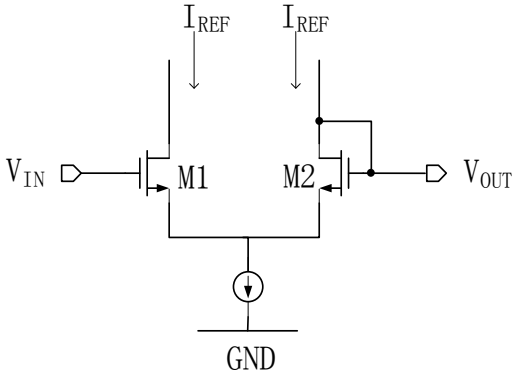


Figure 3. Schematic of source-coupled circuit

In this circuit, when M_1 and M_2 both are in subthreshold region and their souce-drain voltage both are bigger than 0.1V, a gate-to-gate voltage V_{GG} from M_1 to M_2 can be expressed as:

$$V_{GG} = V_{GS,M2} - V_{GS,M1} = \eta V_T \ln\left(\frac{K_2}{K_1}\right) \quad (11)$$

From the equation (11), if K_1/K_2 is smaller than 1, V_{GG} will be a PTAT voltage. Because K_1/K_2 is includes in a logarithmic function, the temperature coefficient of the voltage is too small to compensate the negative temperature dependence of V_{EB}, we need to increase the number of source-coupled pairs. The reference voltage can be obtained by adding $V_{GG,i}$ to V_{EB}. From the equation (10) and (11), the reference voltage can be expressed as

$$V_{REF} = V_{BGR} + \left(-\varepsilon + \sum_{i=1}^{n} \eta \frac{k_B}{q} \ln\left(\frac{K_{2i-1}}{K_{2i}}\right)\right) T \quad (12)$$

Through designing the aspect ratio of the source-coupled pairs and the number of source-coupled pairs, the reference voltage with zero temperature coefficient can be obtained.

2.6 Start-up circuit

The start-up circuit is composed of MOSFETM_1-M_8, in which the M_1-M_8 use a diode connection to provide a bias current for the start-up circuit. The bias current is 2nA. M6 and M7 constitute a inverter. When the circuit is powered up, M6 and M7 are on, the drain voltage of M7 gets high level, and M8 is on. After that, M9 and M10 are on. As the bias current is settled, the gate voltage of M_R gets high level, and M6 and M7 are cut off due the gate voltage of them are high level. Then M8 also are cut off because of the inverter. Finally the BGR finishes starting up, the start-up circuit shuts down.

III. Experimental Results

The proposed BGR fabricated in MagnaChip 0.18μm, 1-poly 6-metal CMOS process, and the verification is finished via Cadence Spectre EDA tool.

Figure 4 plots the simulated voltage of V_{REF} as a function of temperature from -40℃ to 140℃. It can be seen from the Figure 4 that the reference voltage value only changed 2.3mV at the range of -40℃ to 140℃, and the temperature coefficient of the reference voltage was 22.24ppm/℃, which had better temperature characteristics.

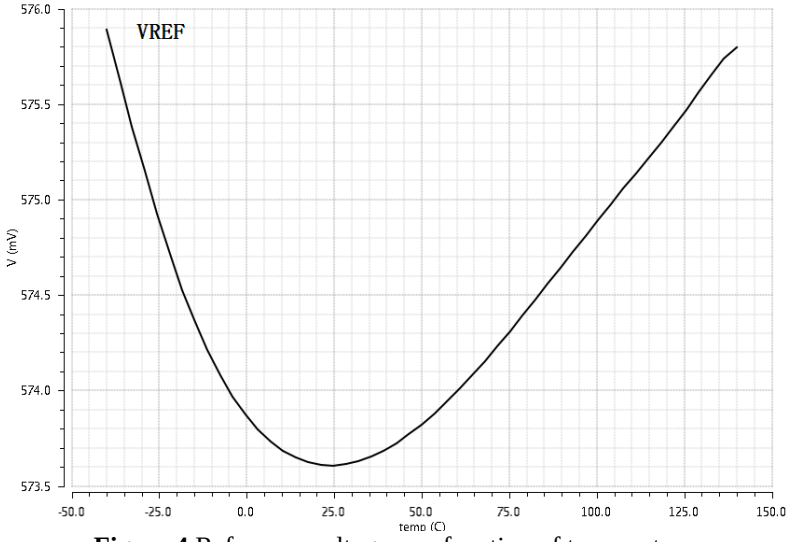
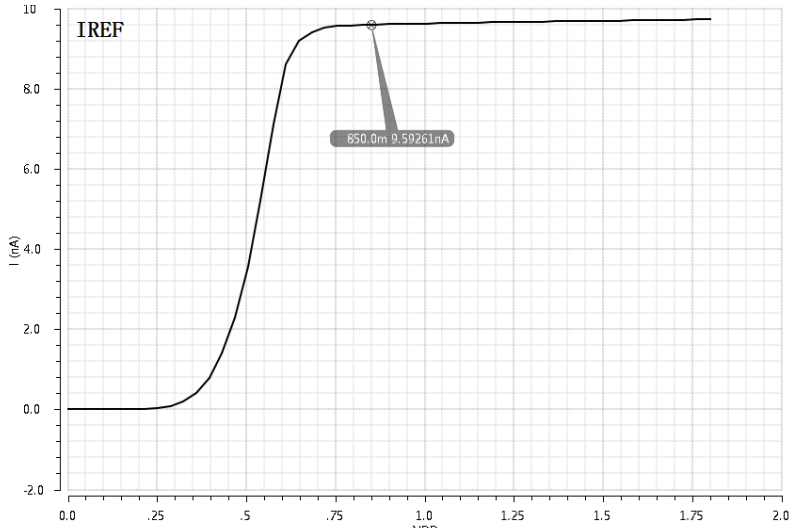
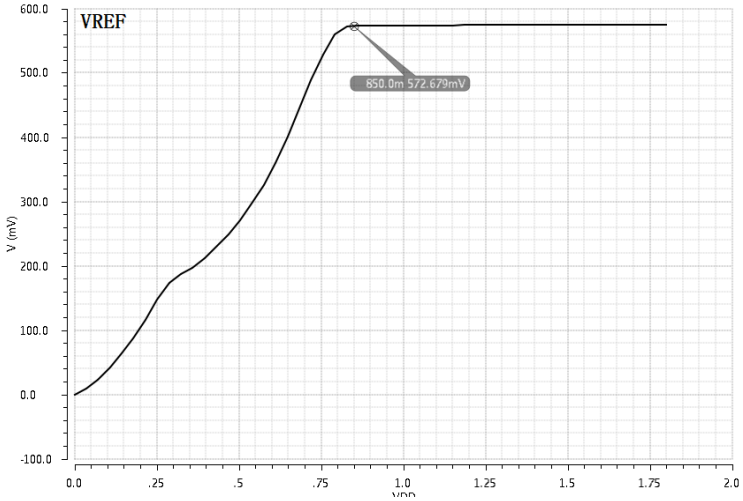


Figure 4 Reference voltage as a function of temperature

Figure 5(a) plots the simulated operating current I_{REF} in the current reference circuit as a function of V_{DD} at room temperature. The circuit operated at more than 0.85V power supply, and the current was about 10nA. The line regulation of the current was 1.42%/V. Figure 5(b) plots the simulated operating V_{REF} in the BGR as a function of V_{DD} at room temperature. The reference voltage obtained at more than 0.85V power supply, and the voltage was about 573mV. The BGR circuit could operate at sub-1-V power supply. It can been seen from Figure 5(b) that the reference voltage only changed 2.13mV at the range of 0.85V to 1.8V. And the line regulation of the reference voltage was 0.22%.



(a)



(b)

Figure 5. Simulated current of I_{REF} and voltage ofV_{REF} as function of V_{DD}

Figure 6 plots the simulated voltage of V_{REF}as a function of temperature from -40℃ to 140℃ in nine samples with different corners and different power supply. The biggest temperature coefficient in Figure 6 is 63.03 ppm/℃.

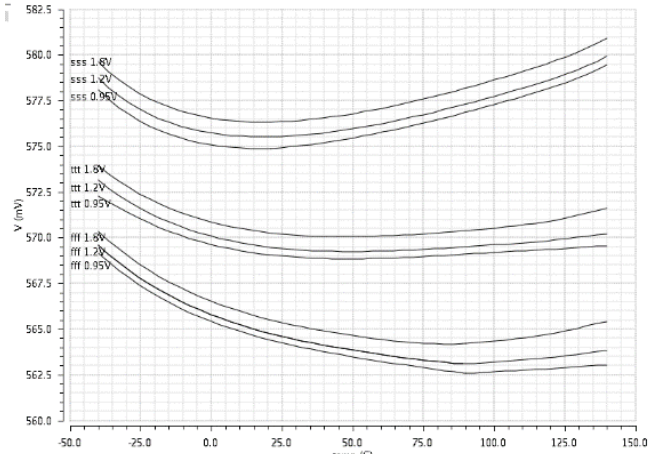


Figure 6. Reference voltage as a function of temperature in nine samples

In order to evaluate robustness to process variations, we performed Monte Carlo simulations. The results for 100 runs are showed in Figure 7. It showed the mean was 574.03mV, the standard deviation was 2.02882mV, and the coefficients of variation was 0.35%.

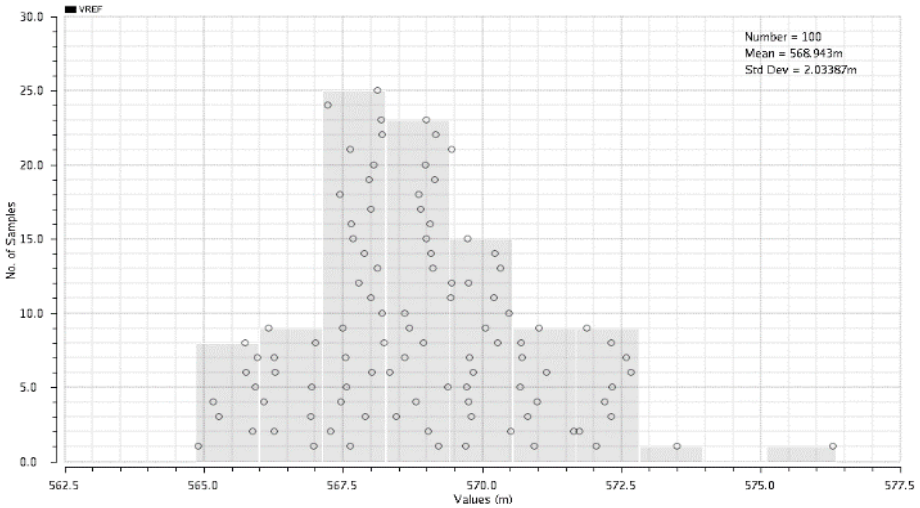


Figure 7. Monte Carlo simulation of 100 runs

Figure 8 plots the simulated PSRR of the BGR circuit. The PSRR of V_{REF} at 100Hz and 10MHz corresponded to -50.036dB and -13.28dB respectively.

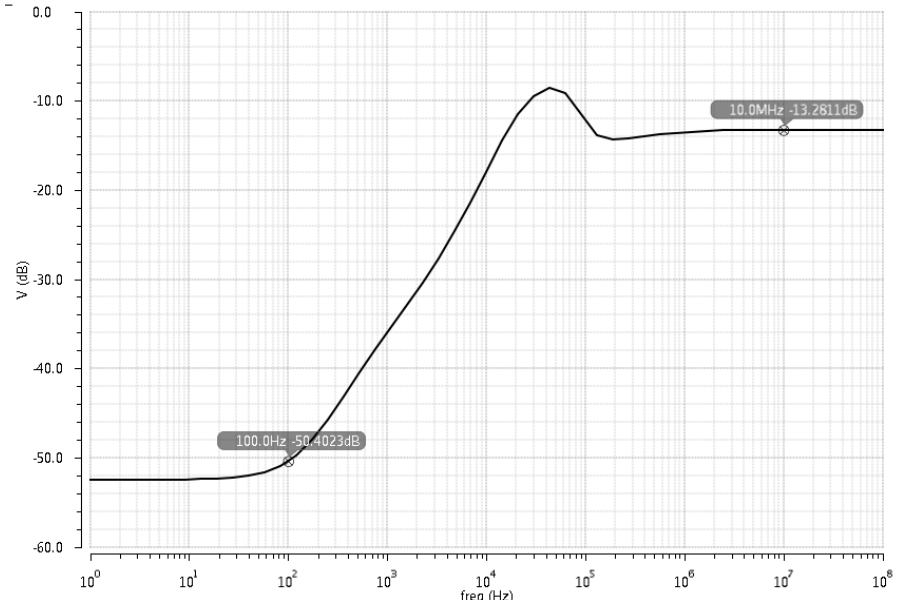


Figure 8. PSRR of reference voltage of V_{REF}

Table 1 summarizes the performance of the proposed BGR circuit and compares it with other BGR circuits [1]-[6]. The proposed circuits operate with lower power dissipation, better temperature characteristic and lower power supply.

Tab.1 Performance summary and comparison

Parameter	Thiswork	[1]	[2]	[3]	[4]	[5]	[6]
Technology（μm）	0.18	0.16	0.35	0.16	0.35	0.13	0.13
Power Supply(V)	0.85~1.8	1.8±10%	2.5	1.1-1.8	1.4~3.0	0.5~3.0	0.5~3.0
TC(ppm/℃)	22.24	5-12	13.7	30	7	231	75
Temperature range（℃）	-40~140	-40~125	-50~150	-40~135	-20~80	-20~80	0~80
Power dissipation（μW）	0.083	55	65.2	1.54	0.3	22×10^{-7}	0.032
Coefficient of variation（%）	0.35	0.75	N/A	0.8	0.87	0.72	0.67
PSRR（dB）@100Hz	-50.036	-74	N/A	N/A	-45	-53	-40

IV. Conclusion

A BGR circuit with lower power dissipation and better temperature characteristic has been presented in this work. The BGR consists of start-up circuit, current reference circuit, voltage divider and PTAT voltage generator. In order to achieve lower power dissipation and operate at lower power supply, this BGR only includes MOSFET and bipolar, without resistors. We design PTAT generator with three source-coupled pairs to compensate the CTAT voltage. We design voltage divider to make the BGR operate at sub-1-V power supply. The simulated results show: The BGR could generate reference voltage of 574mV at 0.95V power supply, and the power dissipation of this circuit was only 83nW. This BGR has simple structure, no resistor and small area. It is suitable for the chip with higher demand of power dissipation and lower power supply.

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