Design of LED Driver Power Based on LNK417EG

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Abstract: *In recent years, people have been committed to the development and the design of new lighting sources. The life of LED lamps depends on the life of the LED driver which has a great relationship with the life of the electrolytic capacitor. In this paper the advantages of the drive power of the electrolytic capacitor are analyzed and the design of the PFC circuit and the transformer is described in details. On the basis of the LNK417 driver chip, a novel single-stage flyback drive circuit without the electrolytic capacitor is designed, which combines the power factor correction technology and constant current control to avoid the use of large electrolytic capacitors. The design and implementation of the control circuit are given and the overall performance is tested and analyzed in the article. The test results show that the driver is of high efficiency, high PF and long life etc. The efficiency is up to 85% and the PF value is not less than 0.9.*
Keywords: *electrolytic capacitor; single-stage flyback; high power factor; LNK417*

I. Introduction

In recent years people have been committed to the development and the design of new lighting sources. The drive power with high efficiency, low cost, high power factor and long life is the key to ensuring LED light quality and overall performance[1]. Due to the ambient temperature, voltage, ripple current, frequency and other factors, the life of the electrolytic capacitor is only a few thousand hours, while the life of LED light source can reach tens of thousands of hours. Their lives do not match, greatly reducing the life of the LED drive power[2]. This article is to study how to solve the problem of the short life of the LED drive power by removing or replacing the capacitors.

This paper designs a new type of LED drive circuit without electrolytic capacitor based on LNK417EG, analyses the main part in details and finally produces a prototype to verify the conclusion.

II. Design Indicators and Overall Framework of the Drive Circuit

2.1 Design Indicators
The input is a wide range of AC voltage 90V ~ 265V and the output is 500mA/30V. In the rated input voltage range, the efficiency reaches 85% and the power factor is not less than 0.9.

2.2 Hardware Design
LED driver hardware design of no electrolytic capacitor includes 9 parts: the preceding-stage protection circuit, EMI filter circuit, rectifier circuit, clamp circuit, power conversion circuit, control circuit, feedback circuit, output circuit, and LED array. The system block is shown as the Fig 1.
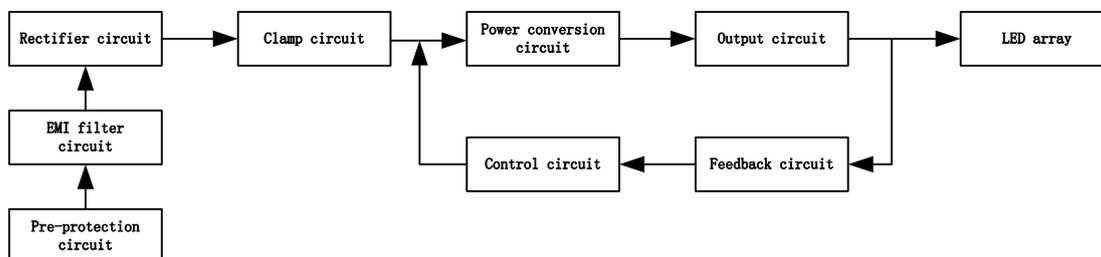
fig.1 block diagram of the circuit

2.3 Analysis of the LNK417EG Working Mechanism
LNK417EG belongs to the Power Internationas company's Linkswitch-H series. The LNK417EG chip itself has very good electrical characteristics and perfect protection and has integrated the PWM control module into the chip, which can effectively prevent the strobe from impacting the LED working efficiency, making the output frequency of the voltage within a very good range. Besides, chips of LinkSwitch-PH series are highly integrated, in small size and more stable.

The internal principle of LNK417 chip is shown in Figure 2.

fig.2 LNK417 chip internal schematic

Pin Function Description:

R pin: reference pin. This pin is used to connect the external precise resistors in the circuit and acts as an intervening pin for non-TRIAC dimming modes.

V pin: voltage detection pin. This pin is connected to the external circuit input main line and detects its peak value.

FB pin: feedback pin. This pin is used for feedback connection of the output voltage.

BP pin: bypass pin. This pin can choose to output different powers as well as different capacitance values according to actual requirements.

S pin: source pin. In the LNK417EG chip is a 725V internal FET and this pin will connect the internal power FET source pin.

D pin: drain pin. This pin is connection point for the drain of the power FET and can provide start and stable internal operating current, making the whole chip work in a stable current state.

III. PFC and Transformer Design

3.1 Single-stage Flyback PFC Circuit Design

After years of development, the two-stage PFC technology has been mature and stable. The two-stage PFC technology has many excellent electrical properties: THD less than 5%, PF up to 0.99, PFC stage constant output voltage, wide input voltage range and so on. However, the realization needs complex circuit structure. The high production costs and the increasing power supply volume lead to the lack of competitiveness in low-power applications[3].

This power supply uses single-stage flyback PFC circuit design and has different flyback converter modes. The current flowing through the inductor depends on the actual conditions, which may be divided into the following three modes: current critical mode (BCM), the current discontinuous mode (DCM), and current continuous mode (CCM). Flyback converter working in CCM mode not only can guarantee that the output current is continuous but also make the output ripple current smaller[4]. So in this case the output part of the circuit and rectifier filter circuit are relatively easy to achieve and can make the overall efficiency of the system much higher[5]. If it works in DCM mode, the output current is discontinuous, the output ripple is larger and the rectifier filter part is relatively complex and thus makes the system less efficient.

Single-stage PFC scheme is shown in Figure 3. Compared with the two-stage PFC circuit, the single-stage circuit combines DC/DC stage and PFC stage and has only one switch and one control circuit. When the switch V conducts, the voltage VC is applied to the primary winding of the transformer. When the rectified voltage is greater than Np, the current will flow through the capacitor C2. When V is cut off, the reverse voltage applied to C2 is the sum of the voltage VN2 on Ns and VC1 minus the input voltage. The addition of two coupling coils N1 and N2 provides a negative feedback voltage that reduces the voltage stress on C1 and improves efficiency.

fig.3 single-stage PFC schematic

3.2 Transformer Design
Flyback high-frequency transformer is actually a power inductor design. It needs the following steps to calculate the primary side inductance value, core size and winding turns.
(1) Maximum duty cycle
According to the volt seconds balance method it can be:

$$V_{in} \Box t_o \overline{\overline{n}} \ V \Box_o \, t$$

(1)

Where ton is T conductance time and toff is the T cutoff time.
The duty cycle D satisfies the following formula:

$$D = \frac{t_{on}}{t_{on} + t_{off}}$$

(2)

Finishing the two formula it is available that:

$$D = \frac{V_{or}}{V_{or} + V_{in}}$$

(3)

According to the design requirements, the minimum input voltage Vin(max)=√2×90V=127V, Dmax=0.44.
(2) Calculate the primary side current
MOS tube during the opening meets the relationship:

$$V_{in} = L_p \cdot \frac{di_p}{dt}$$

(4)

Thus:

$$I_{AVG} = \frac{\int_0^T di_p}{T}$$

(5)

The flyback converter designed in this paper operates in continuous mode

$$I_{pk(ccm)} = \kappa \cdot I_{pk} = \kappa \cdot \frac{2P_0(V_{or} + V_{in(min)})}{V_{in(min)} \cdot \eta \Box V_{or}}$$

(6)

According to practical experience, in this design take κ =0.6 into the parameters $I_{pk(ccm)} = 0.81A$.
(3) Find the primary side inductance value
The primary side inductance value is expressed as

$$L_{p(ccm)} = \frac{V_{in(max)}^{2} \cdot V_{or}^{2} \cdot \eta}{2\kappa \cdot P_0 \cdot f_s \cdot (V_{or} + V_{in(max)})^2} \tag{7}$$

Take the parameters to find Lp=1.6mH.
The actual operation allows the error range to be within 10%.
(4) Core size selection
Using AP method to find the core size:

$$AP = A_w A_e \tag{8}$$

Where AP represents the core area product, Aw means the core windable wire window area [6].
Derived:

$$AP = A_w A_e = \frac{V_p I_{RMS} + V_s I_{SRMS}}{K_f B_w f_s J K_w} \tag{9}$$

The final selected core is RM10.
(5) The calculation of the number of turns of the second and second sides
Find the primary winding formula:

$$N_p = \frac{L_p I_{pk(ccm)}}{A_e \Delta B} \tag{10}$$

Magnetic core RM10's Ae=0.966cm2, take ΔB =0.25T, then Np = 45 turns.
According to the basic principles of the transformer:

$$\frac{V_{or}}{N_P} = \frac{V_s}{N_s} \tag{11}$$

Substituting data, then Ns = 15 turns.
The relationship between the secondary winding Ns and the auxiliary side winding NB is:

$$\frac{N_B}{N_s} = \frac{V_B}{V_0 + V_d} \tag{12}$$

Substituting data, NB = 9 turns.

IV. Design of Circuit and Test Results

4.1 Overall circuit design
According to the choice of the chip before, PFC circuit and the calculation of the transformer, the LED driver is designed with an output voltage of 30V and an output current of 500mA.
The overall circuit design is shown in Figure 4.
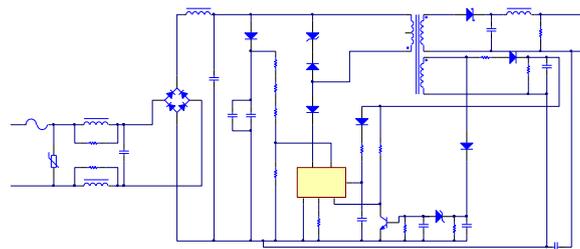
fig.4 schematic diagram

The physical diagram of the circuit is shown in Figure 5.

fig.5 physical diagram

4.2 PFC Test Results and Analysis
Steady-state input voltage and current waveform and input current harmonic test are shown in Figure 6.
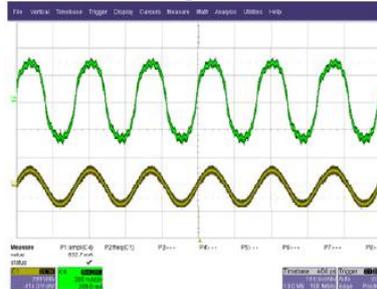
(a) Steady-state voltage and current waveform
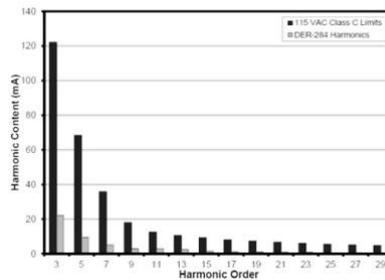
(b) Steady-state current harmonic test chart
fig.6 input voltage and current waveforms and the input current harmonic waveform

In Figure 6 (a), the above waveform is the current waveform; the bottom is the voltage waveform. From the figure it can be seen that the input current and input voltage conduction angle is the same−the standard sine wave. In the single-stage flyback PFC circuit, the correction of the power factor is not as ideal as the two-stage circuit[7], but for low-power products its circuit structure and cost advantages are reflected because of the mathematical relationship between total harmonic distortion and PF[8]. Therefore, the total harmonic diagram has a more intuitive judgment for the power factor. Figure 6 (b) is the total harmonic map.

4.3 Test Results under Wide Range of Input Voltage
When the input voltage changes from 85V to 265V, the efficiency curve is shown in Figure 7.
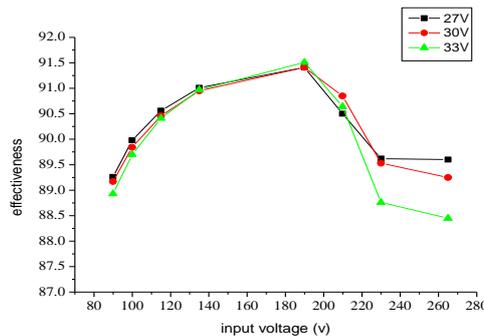
fig.7 efficiency graph

Figure 7 shows that when the output voltage is 27V, 30V, and 33V respectively, with the input voltage changes, the efficiency first increases and then reduces. When the voltage is 210V or so, it reaches the maximum and no matter how the input voltage changes, the efficiency remains above 88% to meet the design requirements.

When the input voltage changes from 85V to 265V, the power factor curve is shown in Figure 8.
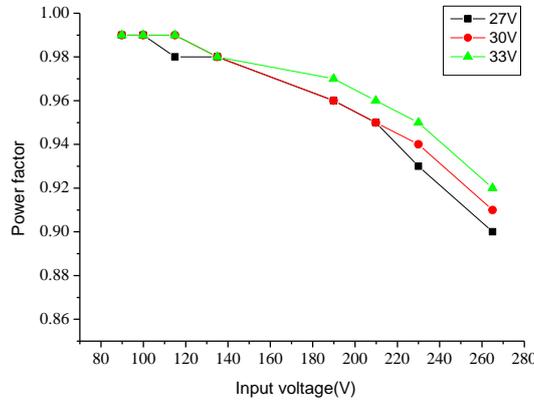
fig.8 power factor graph

It can be seen from Figure 8 that the power factor decreases gradually with the input voltage increasing and decreases to 0.91 when the input voltage is 265 V. When the input voltage is constant, the higher the output voltage, the higher the power factor. Within the wide input voltage range, when the overall power factor is greater than 0.9, it meets the design requirements.

When the input voltage changes from 85V to 265V, the harmonic current curve is shown in Figure 9.
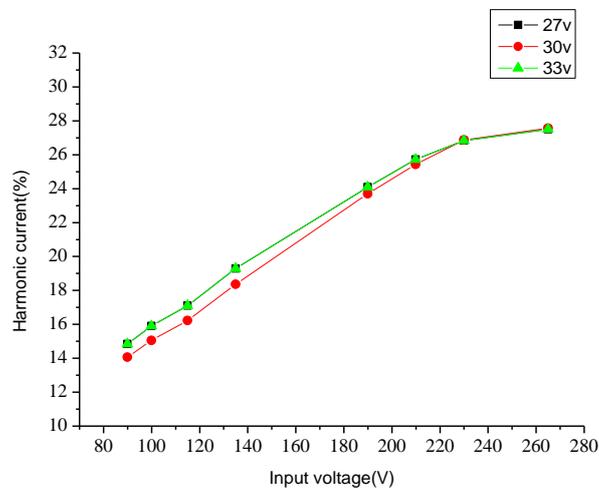
fig.9 harmonic current graph

It can be seen from Figure 9, within the input voltage range, the content of THD has a clear upward trend. When the input voltage is constant, the content of THD decreases as the output voltage increases.

V. Conclusion

According to the design requirements of home lighting condition, this paper designs an LED drive power of no electrolytic capacitor with the characteristics of LNK417EG chip and calculates and designs the PFC circuit and transformer parameters and makes the prototype and performs the performance test. Experimental results show that this power supply's output current is stable, the power efficiency is up to 85%, power factor is higher than 0.90, and the overall performance of the circuit is good and meets the design requirements. Because the design of no electrolytic capacitors greatly optimizes the life of the LED driver, it has an effective use value.

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