IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 11, Issue 4 Ver. II (Jul. – Aug. 2016), PP 63-69
www.iosrjournals.org

A High Gain Broadband Low Noise Amplifier for Wireless Networks

Majid Ghazanfari[1], Alireza Kashani Niya[1], Farhad Razaghian[2]
[1](Department of Electrical Engineering, Central Tehran Branch, Islamic Azad University, Tehran, Iran)
Author Email: eng.majid .ghazanfari@gmail.com
[2](Department of Electrical Engineering, South Tehran Branch, Islamic Azad University, Tehran, Iran)

Abstract: *In this paper, a high gain broadband low noise amplifier with flat power gain is designed for using in the wireless systems in frequency range of 2-5.5 GHz. This LNA is designed employing two pHEMT devices which are in cascode while using current reuse structure. The low noise amplifier which is unconditionally stable in the over frequency range of 2-5.5 GHz, is achieved to have maximum power gain of 28.28 dB at 2.25 GHz. Minimum noise figure of the LNA is 0.939 dB. Maximum of input return loss, output return loss and reverse isolation are less than – 10.15 dB, less than – 10.53 dB and below – 39.18, respectively. The LNA consumes DC power of 54.92 mw. The figure of merit (FOM) of proposed broadband LNA was calculated that shows good improvement compared with other works.*

Keywords: *Cascode, Current Reuse Technique, Inter-stage Matching Network, Low Noise Amplifier, Negative Feedback*

I. Introduction

The noise figure (NF) is a significant parameter for a high frequency amplifier design, the 1st stage of any receiver system has significant influence on the noise operation of total module, so, have a preamplifier with low NF is required, because, simultaneously achievement to minimum NF and maximum power gain is not accomplishable for a high gain LNA, then several trade-off have to be made [1]. A broadband LNA should have flat power gain and excellent input impedance match in the band of interest, achievement to maximum power gain in a narrow frequency range, is possible, although a LNA that is designed with less than maximum power gain, has better bandwidth, but input and output terms of the broadband LNA may be weekly matched [1]. High electron mobility devices have lower noise figures than some other transistors, so they are very excellent for using in LNA design [1]. So in this research, a GaAs pHEMT [2] is used for designing the LNA. In [3], a typical LNA by passive biasing is designed, The LNA schematic is shown in fig. 1.

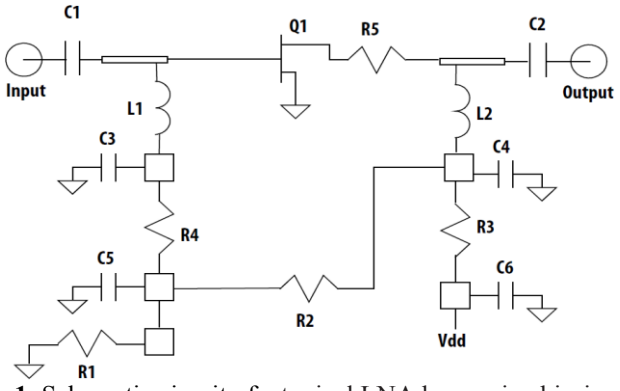

Fig. 1. Schematic circuit of a typical LNA by passive biasing [3]

In the design of proposed LNA, cascode structure is employed. The most important benefits of cascode topology are low NF, flat and high forward power gain, but this topology has a trouble, its DC power consumption is very high, for solving this trouble, current reuse technique can be used [4]. In the some past researches, cascode topology with an inter-stage matching network, is used. E.g. in [5], in the design of a LNA, the conventional cascode architecture is assumed such as two-stage amplifier and result in an inter-stage impedance matching network is employed [5]. In [6], design of cascode amplifier in the frequency of 60 GHz by CMOS process is reported, the amplifier is implemented using an inter-stage impedance matching network, this network, improve the power gain and make an excellent impedance matching between the CS and the CG devices [6].In the second section of this paper, matching networks structure is discussed. In the third part, circuit techniques, such as current reuse topology and negative feedback is described. In the next section of this paper,

schematic design of the proposed high gain broadband LNA, is explained. In 5th part, simulation results is presented and these results is compared with past designs. In the final, conclusion is described.

II. Matching Structure

The broadband impedance matching networks design is possible by analytical methods, but, often computer-aided design tools is needed, since analytical forms calculations are very complicated, naturally, a suitable analytical method can be yield a starting point for a better design that must be tuned and optimized by CAD techniques [7]. In the design of proposed LNA, inter-stage matching network is used, the design of this network is done by helping inductive T network topology [8]. The T network topology is illustrated in fig. 2.

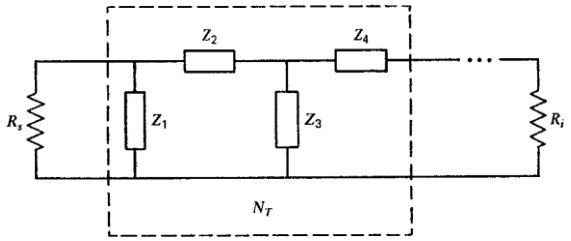

Fig. 2. T Network [8]

Necessary formulas for calculating T network elements are depicted as below [8]:

$$Z_1(s) = \left(\frac{T^2}{sM_{pi}} \right) \tag{1}$$

$$Z_2(s) = \left[sN_{pi}\left(T^2 - T\right) \right] \tag{2}$$

$$Z_3(s) = \left(sN_{pi}T \right) \tag{3}$$

$$Z_4(s) = \left[sN_{sj} + s(1-T)N_{pi} \right] \tag{4}$$

In these relations, M=C, N=L and T=t is used for inductive T network [8].

The L network [7] [9], in the input & output of proposed LNA, is used. The L network topology is shown in fig.3.

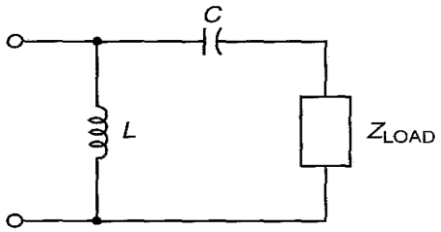

Fig. 3. L network [7]

III. Circuit Techniques

A. Current Reuse Topology

The current reuse structure is illustrated in fig. 4.

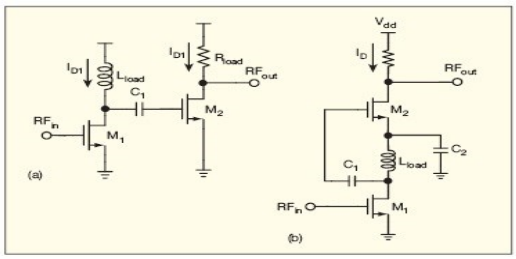

Fig. 4. (a) Cascade structure in comparison with **(b)** current reuse topology [10]

In the current reuse topology, just a DC flow is available, however, the radio frequency signal is amplified by both stages, for this reason, the current reuse structure has both few DC power consumption and high power gain [11]. The operation of this topology is described follow; C1 is a coupling capacitor, C_2 is a bypass capacitor, L_{load} is a RFC, the high inductance of L_{load} , have to radio frequency signal pass by C1 and feed to the gate [11].

B. Negative Feedback

Negative feedback technique will be better the stability factors such as; stabfact1, delta and other stability specifications … , it can be flatten the power gain, and may be enhance the input and output impedance matching (S11 and S22), also, by this technique, at the sacrifice of the power gain and NF, increasing the bandwidth of the LNA is achievable [1].In the design of proposed LNA, resistive parallel feedback [7] and series inductive feedback [8] is used.

IV. Schematic design

After using mentioned topologies, and then tuning and optimization for several times, schematic circuit of the proposed high gain broadband LNA is achieved, that is shown in fig. 5. In the circuit, a type of voltage

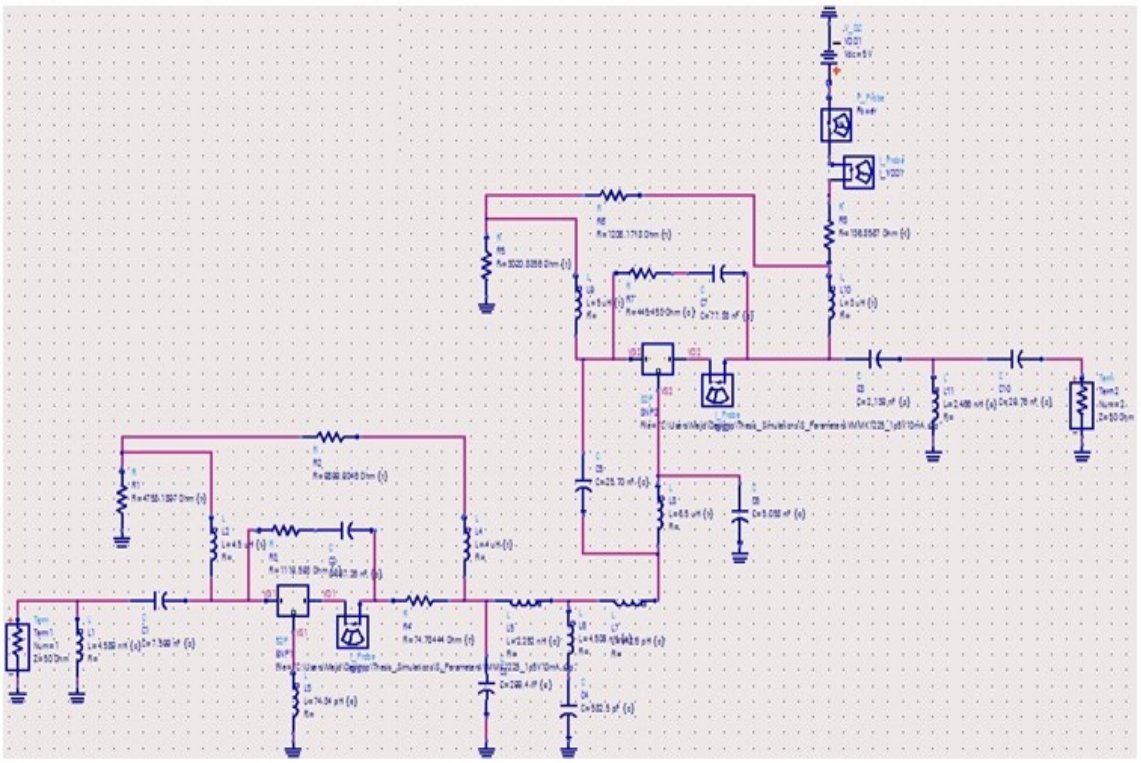

Fig. 5. Schematic circuit of the proposed high gain broadband low noise amplifier

divider include of resistors R5 and R6, makes the voltage required in the gate, the voltage is deduced from the drain, it makes a voltage feedback by employing R8, to maintain drain flow fix [3]. Capacitor C1, and inductor L1, form input L network. L3, consist of a series inductive feedback. Resistor R3 is a parallel feedback. Capacitor C9, and inductor L11, form output L network. Inductors L5, L6, L7 and capacitors C3, C4, consist of modified inductive T inter-stage matching network [6]. Capacitors C5, C6 and inductor L8, form current reuse topology. Capacitor C8, is a coupling capacitor. Notice, the radio frequency specifications of the LNA is achieved using S2P file that is provided by avago technologies company [12]. It should be noted that, with the help of the recommendations issued by the avago technologies company, DC bias characteristics of the proposed amplifier, is reached [3] [13] [14] [15] [16].

V. Simulation results

In this paper, design and simulation are done by advanced design system (ADS) software.Performance of the LNA is described by figures shown below. Situation of the input and output stability circles is illustrated in fig. 6, as seen in this figure, none of stability circles have not any cover into smith chart.

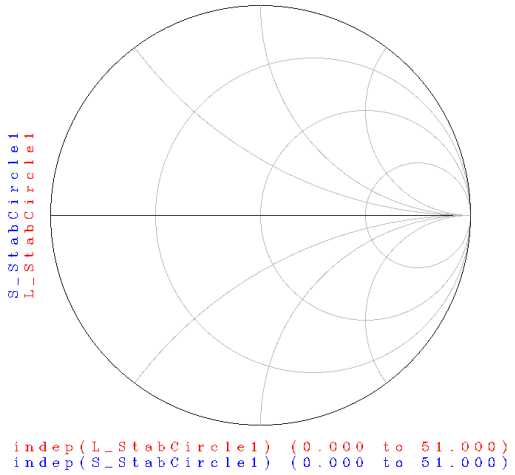

Fig. 6. Stability circles situation in smith chart

Rollet stability factor is illustrated in fig. 7. , as shown in this figure, the StabFact is greater than 1 and by other calculations, also, delta coefficient $|\Delta|$ is smaller than 1, that is mean the LNA is unconditionally stable.

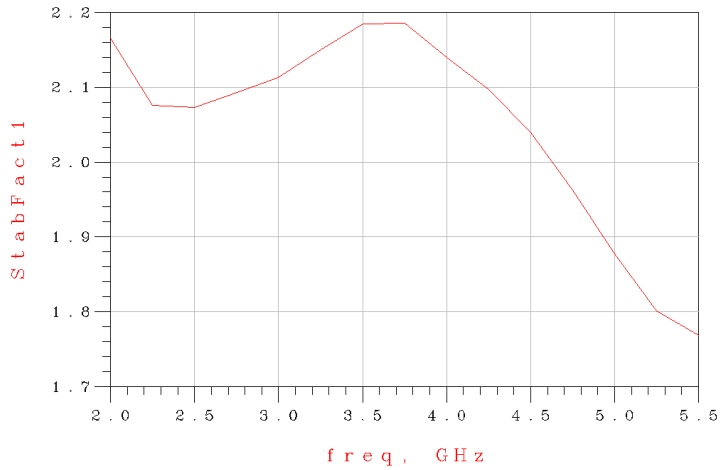

Fig. 7. Rollet stability factor of the proposed LNA

Noise figure curve of the proposed high gain broadband low noise amplifier is demonstrated in fig. 8 and in fig. 9, power gain (S21) of the LNA is presented.

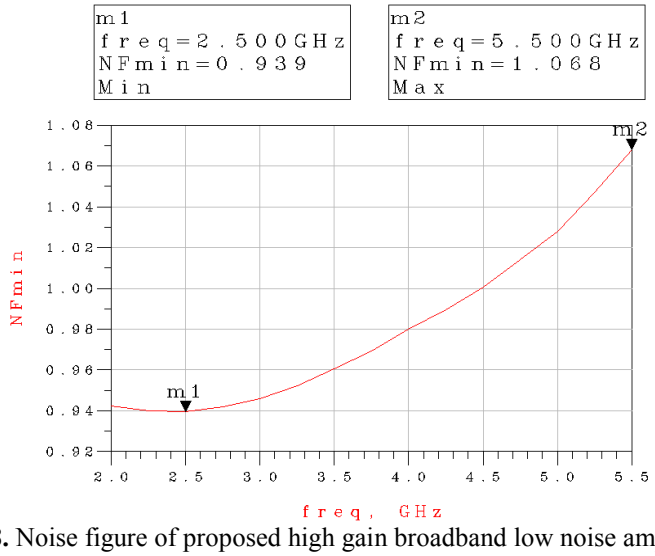

Fig. 8. Noise figure of proposed high gain broadband low noise amplifier

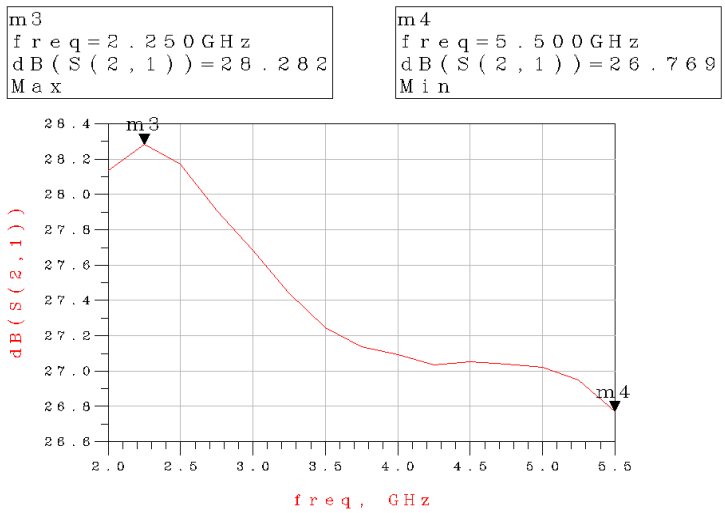

Fig. 9. Power gain (S21) of proposed high gain broadband low noise amplifier

Maximum of input and output return losses and reverse isolation are illustrated in fig. 10, and Minimum of them are shown in fig. 11.

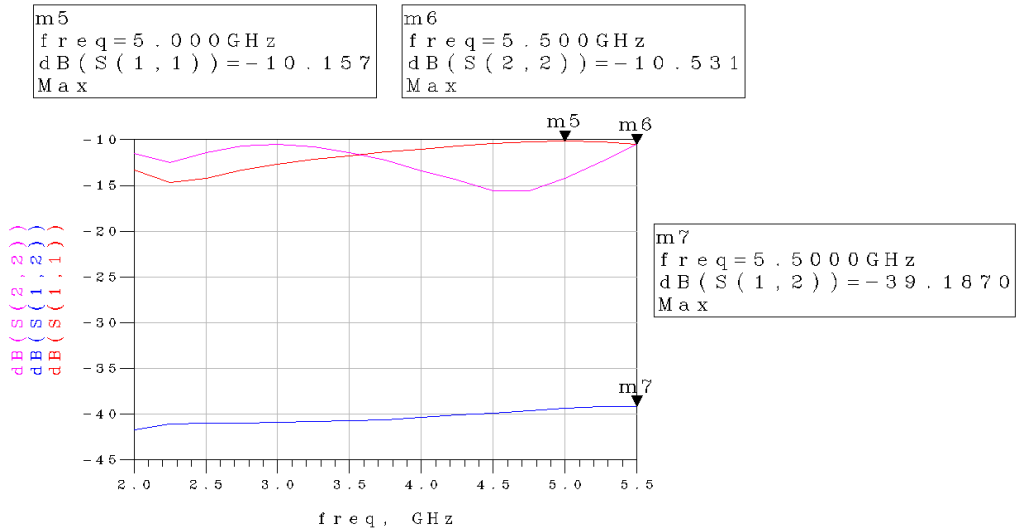

Fig. 10. Maximum of input and output return losses and reverse isolation of proposed high gain broadband low noise amplifier

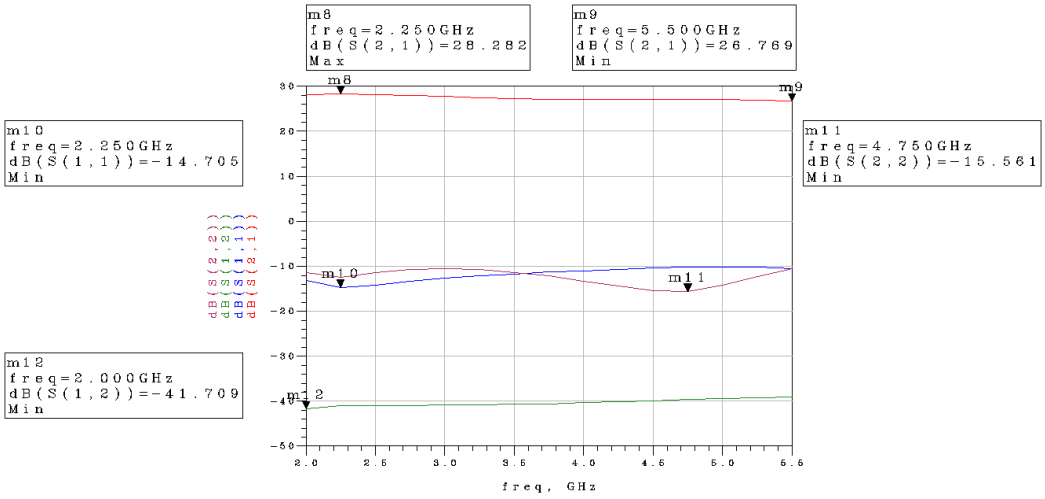

Fig. 11. Minimum of input and output return losses and reverse isolation of proposed high gain broadband low noise amplifie

One of the best criteria for comparison of LNAs performances is figure of merit (FOM) formulas. A conventional formula [17] for FOM is described in (5). In this relation, F, is noise figure and Pd, is DC power consumption of LNA [17].

$$FOM_1 = \frac{Gain_{\max}(dB) \times BW(GHz)}{[F-1] \times P_d(mW)} \quad (5)$$

In the table 2, specifications of the proposed high gain low noise amplifier include of NF, S21, return losses and …, in comparison with other works are listed. As seen in this table, the proposed LNA has the best FOM, between other GaAs LNAs.

Table II. Performance of the proposed LNA in comparison with other published works

Ref.	Tech.	Freq. (GHz)	Gain (dB)	NF (dB)	Pd (mW)	S11 (dB)	S22 (dB)	S12 (dB)	FOM
[18]	0.2 um GaAs	0.3-4	23 ± 1	0.6-0.8	292	< - 15	-	-	2.053
[18]	0.2 um GaAs	0.8-4	22 ± 1	0.5-0.8	212	< - 15	-	-	2.845
[19]	0.13 um GaAs	DC-3.4	10.99-11.96	< 1.287	-	< - 10.8	-	-	-
[19]	0.13 um GaAs	0.12-3	12.13-12.76	< 1.173	-	< - 9.4	-	-	-
[20]	0.2 um GaAs	0.6-1.6	29.33-20.89	0.346	852	< - 11.9	-	-	0.415
[21]	0.2 um GaAs	1-2	15	0.6-0.8	210	< - 12	-	-	0.482
This Work	0.25 um GaAs	2-5.5	28.28-26.77	0.94-1.07	54.92	< - 10.15	< - 10.53	< - 39.18	7.461

VI. conclusion

In this work, a high gain broadband LNA with flat power gain is designed for using in the wireless receiver applications in the frequency band of 2-5.5 GHz. This LNA, employed some techniques, such as; the inter-stage matching network, the current reuse topology, negative feedback and etc. The LNA is designed employing two pHEMT transistors that are in cascode topology while using current reuse technique. The LNA that is unconditionally stable over the frequency range of 2-5.5 GHz, is obtained to have maximum forward power gain (S21) of 28.28 dB at 2.25 GHz. The forward power gain ripple is about 1.51 dB over the band of interest. Minimum NF of the LNA is 0.939 dB. Minimum of input return loss, output return loss and reverse isolation are less than – 14.7 dB, less than – 15.56 dB and below – 41.7, respectively. The DC power consumption of the LNA is about 54.92 mW. The figure of merit of proposed broadband LNA was calculated that demonstrates good improvement compare with past researches. So, the proposed high gain broadband low noise amplifier can be a good candidate for using in the wireless receivers that is working in the frequency range of 2-5.5 GHz.

References

[1]. D. M. Pozar, *Microwave engineering* (4th edition, Amherst: John Wiley & Sons, 2011).
[2]. VMMK-1225 Datasheet, 0.5 to 26 GHz Low Noise E-PHEMT in a Wafer Scale Package, Avago Technologies, jan. 2014.
[3]. VMMK-1225 Applications Information, Avago Technologies, aug. 2010.
[4]. A. N. Ragheb, G. A. Fahmy, I. Ashour, A. Ammar, A 3.1-10.6 GHz Low Power High Gain UWB LNA Using Current Reuse Technique, in *2012 4th International Conf. on Intelligent and Advanced Systems (ICIAS2012)*, 2012, 741-744.
[5]. C. Zhang, D. Huang, D. Lou, Optimization of Cascode CMOS Low Noise Amplifier Using Inter-stage Matching Network, in *IEEE Conf. on Electron Devices and Solid-State Circuits*, 2003, 465-468.
[6]. B. Heydari, P. Reynaert, E. Adabi, M. Bohsali, B. Afshar, M. A. Arbabian, A. M. Niknejad, A 60-GHz 90-nm CMOS Cascode Amplifier with Interstage Matching, in *2nd European Microwave Integrated Circuits Conference (EuMIC)*, Munich, Oct. 2007, 88-91.
[7]. G. Gonzalez, *Microwave transistor amplifiers: analysis and design (2nd Edition)* (New Jersey: Prentice Hall, aug. 1996).
[8]. Tri.T.Ha, *Solid state microwave amplifier design* (New York: John Wiley & Sons, 1981, p. 326).
[9]. S. Long, Matching Networks, University of California, Santa Barbara, jan. 2007, [Online].Available: http://www.ece.ucsb.edu/~long/ece145a/Notes5_Matching_networks.pdf
[10]. Sichun Du, Chunhua Wang, Guangxiang Zhang, Current Reuse Enhances UWB LNA, microwaves & rf, feb. 2012. [Online]. Available: http://mwrf.com/active-components/current-reuse-enhances-uwb-lna
[11]. Z.Y. Lu, H.Y. Xie, W.R. Zhang, W.J. Huo, Z.J. Guo, G.H. Xing, C.B. Ding, L.Chen, Y.J. Zhang, Design of Dual band SiGe HBT LNA with Current Reuse Topology, in *International Conf. of Electron Devices and Solid-State Circuits (EDSSC)*, Tianjin, 2011, 1 - 2.
[12]. VMMK-1225 Scattering Parameters Files, 2009. [Online].Available: http://www.avagotech.com/docs/050509_VMMK-1225

[13]. ADS Model - VMMK1225 Modeling, AvagoTechnologies, [Online]. Available: http://www.avagotech.com/docs/33542
[14]. ADS Model - ADS Model of VMMK-1225, AvagoTechnologies, [Online]. Available: http://www.avagotech.com/docs/110209_VMMK-1225
[15]. Using ADS to simulate Noise Figure, University of California, Santa Barbara, 2004. [Online].Available: http://www.ece.ucsb.edu/~long/ece145a/ADStutorial_NF_F04.pdf
[16]. K. Payne, Practical RF Amplifier Design Using the Available Gain Procedure and the Advanced Design System EM/Circuit Co-Simulation Capability, Agilent Technologies, 2009. [Online].Available: http://cp.literature.agilent.com/litweb/pdf/5990-3356EN.pdf
[17]. M.-T. Hsu , Y.-C. Chang , Y.-Z. Huang, Design of low power UWB LNA based on common source topology with current-reused technique, *Microelectronics Journal,* 44(12), 2013, 1223-1230.
[18]. X. Li , W.A. Serdijn, On the Design of Broadband Power-to-Current Low Noise Amplifiers, *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS,* 59(3), 2012, 493-504.
[19]. Y. Yao, T. Fan, Design of DC-3.4GHz Ultra-Wideband Low Noise Amplifier with Parasitic Parameters of FET, *International Journal of Engineering Research and Applications,* 4(4) (Version 1), 2014, 280-284.
[20]. J. Xu, B. Woestenburg, J. Geralt bij de Vaate and W.A. Serdijn, GaAs 0.5 dB NF dual-loop negative feedback broadband low-noise amplifier IC, *ELECTRONICS LETTERS,* 41(14), 2005, 780-782.
[21]. X. Li , W. A. Serdijn , B. E. M. Woestenburg , J. G. B. de Vaate, A 1–2 GHz high linearity transformer-feedback power-to-current LNA, *Analog Integrated Circuits and Signal Processing,* 63(1), 2010, 113-119.