

## Design of novel cascaded multilevel inverter by series of sub multilevel inverters

Bolla Madhusudana Reddy, Dr.Y.V.Siva Reddy, Dr.M.Vijaya Kumar

*Ph.D scholar, JNTUA, Anathapuramu, A.P, India.*

*Dept. of Electrical and Electronics Engineering, G. Pulla Reddy Engineering College, Kurnool, A.P, India.*

*Dept. of Electrical and Electronics Engineering JNTUA College of engineering, Ananthapuramu, A. P, India.*

---

**Abstract:** This paper proposed novel multilevel inverter with low number of switches. Multilevel inverters are applicable for high power purpose in industries which become very popular. When compared to two level inverters these multilevel inverters produces good quality of output wave form. In such a way that, at first new proposed topology which as sub multilevel inverter is designed after that cascaded connection of sub multi level inverters called as novel cascaded multilevel inverter is proposed. This proposed novel cascaded multilevel inverter uses less number of switching devices. Separate attention optimal structure has been achieved by considering in different aspects such as number of switching devices, number of dc voltage sources and standing voltages on switching devices. This proposed novel cascaded multilevel inverter analyzed in symmetric and asymmetric forms of topologies which were compared with other multilevel inverter topologies suppose normal H bridge multilevel inverter by considering number components such as number of switches & IGBTs etc. The validity of proposed multilevel inverter verified with computer simulation.

**Keywords:** Power Electronics; multilevel inverters; sub multilevel inverter; optimal structure; symmetric and asymmetric; high quality wave form.

---

### I. Introduction

Basically multilevel inverter is an array of semiconductor devices and dc sources. Multilevel inverters are more popular for high power purposes in Industry because of high quality output voltage wave forms when compared to two level inverters. By increasing number of levels in Multilevel inverter the output voltage has more steps like staircase waveform which has less harmonic distortion. The concept of utilizing multiple small voltage levels to perform power conversion was patented by an MIT researcher over twenty years ago [1, 2]. Three types of well known Multilevel inverters are there 1. Neutral point clamped (NPC) Multilevel inverter or Diode clamped Multilevel (DCML) Inverter (Three level inverter) 2. Flying capacitor (FC) Multilevel Inverter 3. Cascaded H-Bridge (CHB) Multilevel inverter 4. Other multilevel inverters. Diode-clamped multilevel inverter is the first generation three level inverter. This provides multiple voltage levels through connection of the phases to a series bank of capacitors. A common dc bus is shared by all these phases there by capacitance requirement of converter is minimized. The capacitors can be charged as a group in advance. Efficiency is more for fundamental frequency witching. The real power flow is difficult for single inverter due to the intermediate dc levels will overcharge. The total number of clamping diodes requirement is quadratic ally related to the number of levels [5, 6]. Another fundamental multilevel inverter topology is the flying capacitor which involves series connection of capacitor clamped switching cells. Flying capacitor multilevel inverter offers some redundant switching states that can be used to regulate capacitor voltages. The number of capacitors increases by increasing number of voltage levels. According to the original invention [27], the concept can be extended to any number of levels by increasing the number of capacitors. Compared to the diode-clamped inverter, this topology has several unique and attractive features as described below: Inverter Structure i) added clamping diodes are not needed. ii) It has switching redundancy within the phase, which can be used to balance the flying capacitors so that only one dc source is needed. iii) The number of voltage levels obtained without connecting transformer so that cost of flying capacitor multi level inverter is reduced, in addition power loss reduced. iv) In flying capacitor inverter the capacitors in one phase leg are charged with different voltage levels where as in diode clamped multi l level inverter series connection of capacitors share same voltage level. v) In this Real and reactive power flow can be controlled. The disadvantages are i) Control is difficult to track the all voltage levels for all of the capacitors .ii) Recharging of the all capacitors to the same voltage level and their start up are very time taken.iii) real power transmission is not accurate there by efficiency poor. iv) Since the capacitors have large fractions of the dc bus voltage across them, rating of the capacitors is a design challenge. v) The large numbers of capacitors are more expensive and bulky than clamping diodes.

Cascaded H Bridge Multilevel inverter [12] use series connection of H Bridge cells with an isolated DC voltage sources connected on each cell. There are two groups of CHB Multilevel inverters based on the values of DC sources are Symmetrical and asymmetrical. In Symmetrical CHB MLI topology the values of DC

sources are equal. To increase output voltage levels, the number of switching devices are need to be increase. In asymmetrical CHB MLI topology the values of DC sources are different there by output voltage levels can be increased without increasing number of switching devices. CHB Multilevel inverters[20] have been industrially employed in several applications like pumps, fans, compressors etc.. The advantages are i) the regulation of the DC buses is simple. ii) Modularity of control can be achieved. In the diode clamped multi level inverter and flying capacitor multilevel inverter the individual phase legs must be modulated by a central controller where as in the H-bridge multilevel inverters of a cascaded structure can be modulated separately. iii) Requires the least number of components among all multilevel converters to achieve the same number of voltage levels. iv) soft-switching can be used in this structure to avoid bulky and loss resistor-capacitor-diode snobbery. The disadvantages are i) Communication between the full-bridges is required to achieve the synchronization of reference and carrier wave forms ii) Needs separate dc sources for real power conversions, and thus its applications are somewhat limited. One of the other topologies are Modular Multilevel inverter [10, 11], but to increase output voltage levels, more components or switches are required. Another topology is Hybrid Multilevel inverter [7, 17] which is a combination of CHB and diode clamped multilevel inverters which generates nine level.

## II. Proposed Multilevel Inverter

Primarily a sub multilevel inverter is designed and then series of all sub multilevel inverters considered as novel cascaded multilevel inverter.

Sub multilevel inverter is designed, used to reduce the number of switching devices. The proposed novel multilevel inverter has been analyzed in both symmetric and asymmetric topologies.

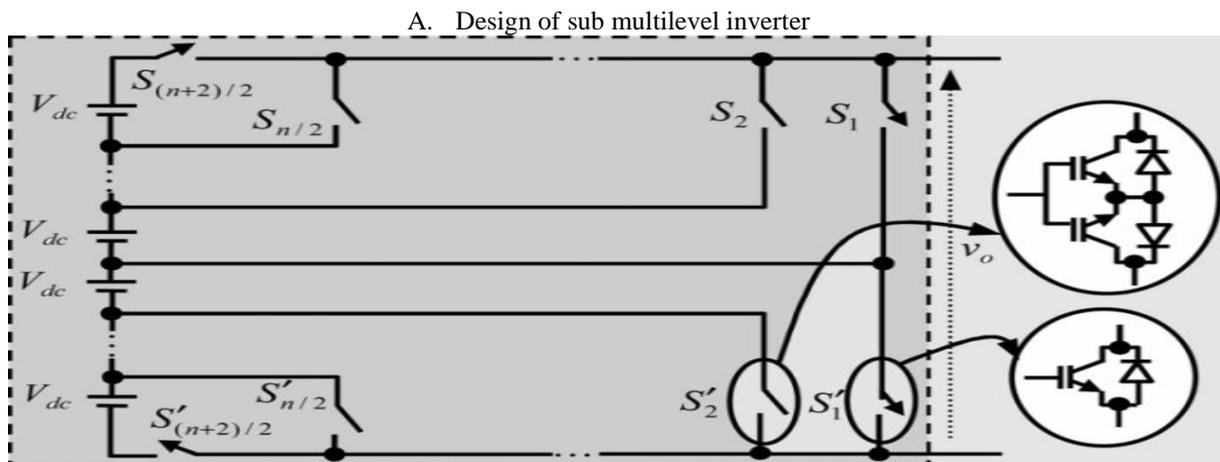


Fig 1 design of submultilevel inverter

The fig 1 designed sub multilevel inverter topology contains ‘n’ number of dc voltage sources. Some switching devices are considered as unidirectional and other are bidirectional. The unidirectional switching devices consists of an insulated gate bipolar transistor (IGBT) with anti parallel diode such as S1, S1’, S\_{(n+2)/2} & S’\_{(n+2)/2}. The bidirectional switching devices consists of two parallel unidirectional switches such as S2, S2’, S\_{n/2}, S\_{n/2}’. These switching devices can withstand both positive as well as negative voltages. The designed sub multilevel inverter can be able to generate zero and positive levels of voltages only but not negative voltage levels.

State	Switches states									v <sub>o</sub>
	S <sub>1</sub>	S <sub>1</sub> '	S <sub>2</sub>	S <sub>2</sub> '	...	S <sub>n/2</sub> '	S <sub>n/2</sub>	S <sub>(n+2)/2</sub>	S <sub>(n+2)/2</sub> '	
1	1	1	0	0	...	0	0	0	0	0
2	0	1	1	0	...	0	0	0	0	V <sub>dc</sub>
3	0	0	1	1	...	0	0	0	0	2V <sub>dc</sub>
⋮	⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮
n-1	0	0	0	0	...	1	1	0	0	(n-2)V <sub>dc</sub>
n	0	0	0	0	...	0	1	0	1	(n-1)V <sub>dc</sub>
n-1	0	0	0	0	...	0	0	1	1	nV <sub>dc</sub>

Table 1 Output voltage levels of sub multilevel inverter

In the given above table, ‘1’ means that corresponding Switch turned ON, ‘0’ means that corresponding switch turned OFF. In order to get each and every different voltage levels, two switches need to be ON, among them one from upper group and another from lower group. Example: To get out put voltage level  $(n-1)V_{dc}$ , the  $S_{n/2}$  and  $S_{(n+2)/2}$  switches are being turned ON. The proposed sub multilevel inverter can only generate zero and positive levels of voltages. Equations for proposed sub multilevel inverter

$$\begin{aligned}
 N_{\text{switch,sub}} &= 2, \text{ for } n = 1 && 1 \\
 &= (n + 2), \text{ for } n \geq 2 && \\
 N_{\text{driver,sub}} &= N_{\text{switch,sub}} && 2 \\
 N_{\text{IGBT,sub}} &= 2n && 3 \\
 N_{\text{source,sub}} &= n && 4
 \end{aligned}$$

All switching devices will get different OFF state voltages at different types switching combinations. The standing voltage is considered as the maximum voltage from these OFF state voltages. Standing Voltage (maximum Off state voltage) of  $S_1 = (n/2)V_{dc}$  and for  $S_2 = (n/2-1)V_{dc}$  when  $S_{(n+2)/2}$  switch is ON. Standing Voltage (maximum Off state voltage) of  $S_1' = (n/2)V_{dc}$  and for  $S_2' = (n/2-1)V_{dc}$  when  $S_{(n+2)/2}$  switch is ON. Total standing voltage of sub multilevel inverter is sum of standing voltages of all switching devices. With different types of ‘n’ value the standing voltage of  $i^{\text{th}}$  sub multilevel inverter ( $V_{\text{stand},i}$ ) can be considered as following Equations based ‘n’ is odd or even.

$$V_{\text{stand},i} = \begin{cases} 2 \sum_{k=0}^{\left(\frac{n-1}{4}-1\right)} \left(\frac{n-1}{2}-k\right)V_{dc,i} + 2 \sum_{k=0}^{\left(\frac{n+1}{2}-1\right)/2} \left(\frac{n+1}{2}-k\right)V_{dc,i} + \frac{n-1}{4}V_{dc,i} = \left(\frac{3n^2}{8} + n + \frac{5}{8}\right)V_{dc,i} & \text{if } n \text{ is odd and } \frac{n-1}{2} \text{ is even} \\ 2 \sum_{k=0}^{\left(\frac{n-1}{2}-1\right)/2} \left(\frac{n-1}{2}-k\right)V_{dc,i} + 2 \sum_{k=0}^{\left(\frac{n+1}{4}-1\right)} \left(\frac{n+1}{2}-k\right)V_{dc,i} + \frac{n+1}{4}V_{dc,i} = \left(\frac{3n^2}{8} + n + \frac{5}{8}\right)V_{dc,i} & \text{if } n \text{ is odd and } \frac{n-1}{2} \text{ is odd} \\ 4 \sum_{k=0}^{\left(\frac{n}{2}-1\right)/2} \left(\frac{n}{2}-k\right)V_{dc,i} = \left(\frac{3n^2}{8} + n + \frac{1}{2}\right)V_{dc,i}, & \text{if } n \text{ is even and } \frac{n}{2} \text{ is odd} \\ 4 \sum_{k=0}^{\left(\frac{n}{4}-1\right)} \left(\frac{n}{2}-k\right)V_{dc,i} + \frac{n}{2}V_{dc,i} = \left(\frac{3n^2}{8} + n\right)V_{dc,i} & \text{if } n \text{ is even and } \frac{n}{2} \text{ is even} \end{cases}$$

5

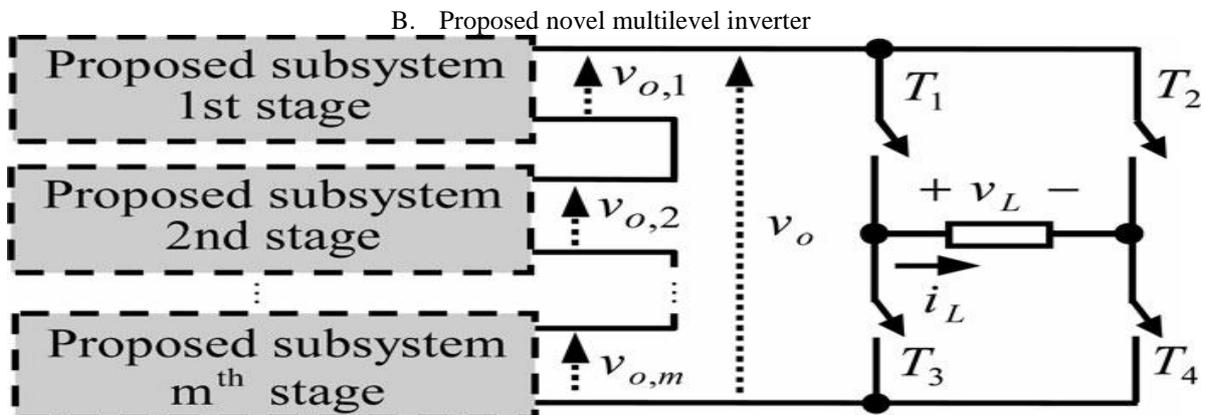


Fig 2 Design of proposed novel multi level inverter

The designed sub multilevel inverters are connected in cascaded to get the desired voltage and different number of voltage levels. 'm' is number of sub multilevel inverters, 'n' is dc sources' number in each sub multilevel inverter. The dc voltage sources are equal in symmetrical novel multilevel inverter where as in asymmetrical novel multilevel inverter the dc voltage sources are different.

The designed sub multilevel inverter can able to generate only zero and positive levels of voltages, so in order to get negative level of voltage ,H-bridge inverter is need to be connect at output of series connected sub multilevel inverters.

Equations for proposed novel multilevel inverter

$$N_{\text{switch}} = 2m + 4, \text{ for } n = 1 \quad 6$$

$$m(n + 2) + 4, \text{ for } n \geq 2$$

$$N_{\text{driver}} = N_{\text{switch}} \quad 7$$

$$N_{\text{IGBT}} = 2mn + 4 \quad 8$$

$$N_{\text{source}} = mn \quad 9$$

1) Proposed symmetric novel multilevel inverter

In this topology all of the dc sources of sub multilevel inverters are considered to be equal such as

$$V_{\text{dc},1} = V_{\text{dc},2} = \dots = V_{\text{dc},m} \quad 10$$

$$\text{Output voltage level number } N_{\text{level}} = 2mn + 1 \quad 11$$

$$\text{sub multilevel inverters number } m = (N_{\text{level}} - 1) / (2n) \quad 12$$

$$\text{Standing voltage on the switches of each sub multilevel inverters } V_{\text{stand},1} = V_{\text{stand},2} = \dots = V_{\text{stand},m} \quad 13$$

$$\text{Total standing Voltage on switches of general Multilevel inverter } V_{\text{stand,total}} = m \cdot V_{\text{stand},1} + 4mnV_{\text{dc},1} \quad 14$$

2) Proposed asymmetric novel multilevel inverter

In this topology the different number of sub multilevel inverters has different dc voltage sources. If first sub multilevel inverter contains a dc voltage source as  $V_{\text{dc},1}$  and second sub multilevel inverter consists a dc voltage source as  $V_{\text{dc},2}$ , and so on up to  $V_{\text{dc},m}$ . So that to get maximum number of levels below equations are to follow

$$V_{\text{dc},2} = (n+1) \cdot V_{\text{dc},1} \quad 15$$

$$V_{\text{dc},3} = (n+1)V_{\text{dc},1} + nV_{\text{dc},2} = (n+1)\text{pow}(2) V_{\text{dc},1}$$

$$\text{Therefore } V_{\text{dc},i} = (n+1)\text{pow}(i-1) \cdot V_{\text{dc},1} \quad 16$$

Where  $i = 1, 2, 3, \dots, m$

$$N_{\text{level}} = 2(n+1)\text{pow}(m) - 1 \quad 17$$

The maximum output voltage of asymmetric topology is  $V_{0,\text{max}} = [(n+1)\text{pow}(m) - 1]V_{\text{dc},1} \quad 18$

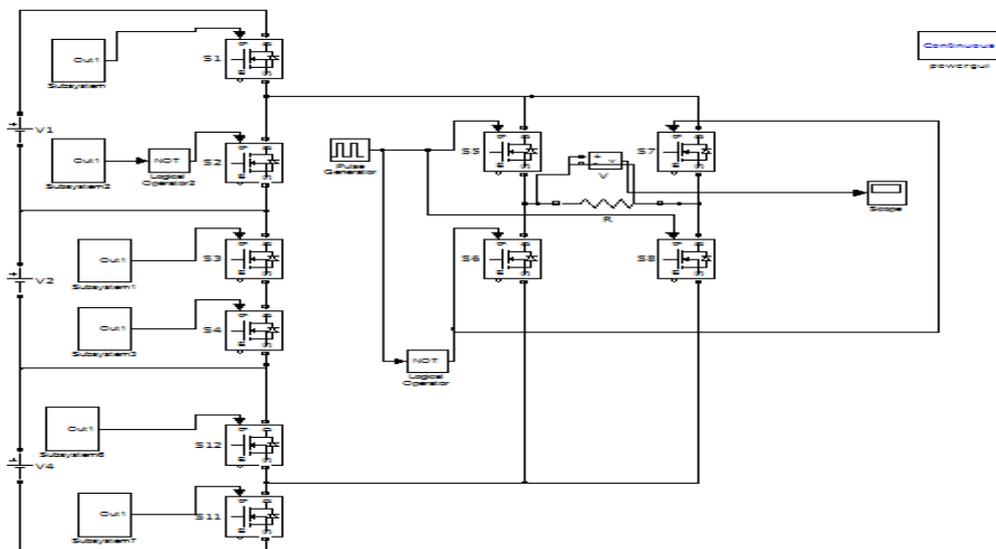
Total standing voltage of asymmetrical multilevel inverter

$$V_{\text{stand,total}} = \sum_{i=1}^m V_{\text{stand},i} + 4V_{0,\text{max}} \quad 19$$

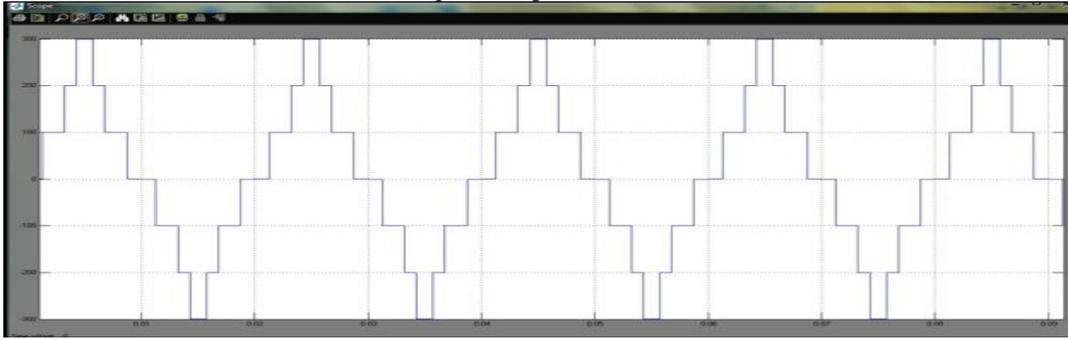
II. SIMULATION RESULTS & STUDIES

A. Seven level proposed symmetric novel multilevel inverter

Simulation circuit:

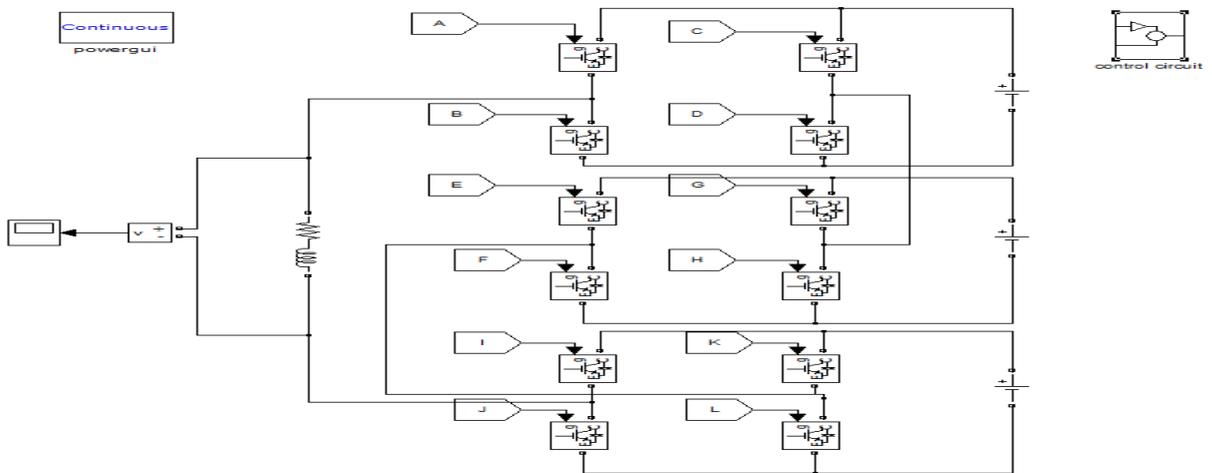


Output voltage waveform:

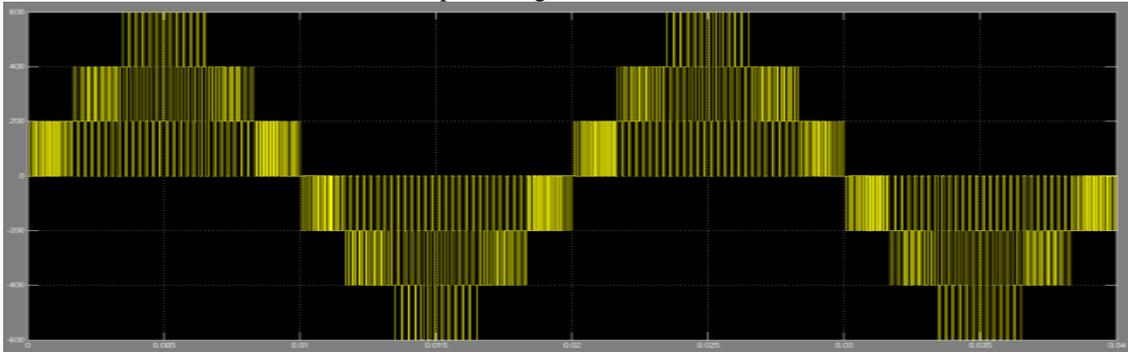


B. Seven level pre existing symmetric H Bridge multilevel inverter

Simulation circuit:



Output voltage wave form:



C. Comparison between Proposed novel multilevel inverter with cascaded H bridge multilevel inverter in case of number of switches for seven levels

Types	Level	No.of switches	% of switching losses
Pre-existing	7	12	X%
Proposed	7	10	0.83x%

$$\begin{aligned} \text{\% of Reduction in losses} &= (1 - 0.83) \times \% \\ &= 0.17 \times \% \end{aligned}$$

### III. Extension Of Proposed Topology

By using three single phase novel multilevel inverters connection considered as three phase novel multilevel inverter. In this the switches cannot be shared between any phases there by single unit is possible. The dc voltage sources in different phase units must be isolated hence the load can be star or delta connected. In place of three phase load the induction motor is connected for checking its performance like speed, torque, flux, losses and efficiency delta connected. In place of three phase load the induction motor is connected for checking its performance like speed, torque, flux, losses and efficiency

### IV. Conclusion

In this paper primarily a sub multilevel inverter is designed there after series connection all sub multilevel inverters would be considered as novel cascaded multilevel inverter. This can be analyzed in both in symmetrical and asymmetrical forms for achieving required voltage and reducing complexity. Finally this novel multilevel inverter consists superior features over conventional inverters in terms of reduced number of switches, isolated dc supplies, reduction of harmonics, optimal structure, good control, cost and reliability.

### References

- [1]. J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [2]. J. H. Kim, S. K. Sul, and P. N. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage-source inverter," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1239–1248, Jul./Aug. 2008.
- [3]. O. Lopez, J. Alvarez, J. Doval-Gandoy, F. D. Freijedo, A. Nogueiras, A. Lago, and C. M. Penalver, "Comparison of the FPGA implementation of two multilevel space vector PWM algorithms," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1537–1547, Apr. 2008.
- [4]. Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltage sharing converter to supply single-phase asymmetrical four-level diode clamped inverter with high power factor loads," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2507–2520, Oct. 2010.
- [5]. J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral point clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219–2230, Jul. 2010.
- [6]. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.
- [7]. M. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive application," in *Proc. Appl. Power Electron. Conf.*, 1998, vol. 2, pp. 523–529.
- [8]. Rufer, M. Veenstra, and A. Gopakumar, "Asymmetric multilevel converter for high resolution voltage phasor generation," in *Proc. Eur. Conf. Power Electron. Appl.*, Lausanne, Switzerland, 1999, pp. 1–10.
- [9]. J. I. Leon, S. Kouro, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Multidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 412–420, Feb. 2011.
- [10]. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," presented at the *IEEE PowerTech. Conf.*, vol. 3, Bologna, Italy, 2003.
- [11]. G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. McDonald, "Modular multilevel inverter: pulse width modulation and capacitor balancing technique," *IET Power Electron.*, vol. 3, no. 5, pp. 702–715, 2010.
- [12]. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657–2664, Nov. 2008.
- [13]. Babaei, S. H. Hosseini, G. B. Gharehpetian, M. Tarafdar Haque, and M. Sabahi, "Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology," *Elsevier J. Electric Power Syst. Res.*, vol. 77, no. 8, pp. 1073–1085, Jun. 2007.
- [14]. Babaei and M. S. Moeinian, "Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem," *Elsevier J. Energy Convers. Manage.*, vol. 51, no. 11, pp. 2272–2278, Nov. 2010.
- [15]. Y. Hinago and H. Koizumi, "A single phase multilevel inverter using switched series/parallel dc voltage sources," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 2643–2650, Aug. 2010.
- [16]. J. Li, S. Bhattacharya, and A. Q. Huang, "A new nine-level active NPC(ANPC) converter for grid connection of large wind turbines for distributed generation," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp.
- [17]. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 51–64, Jan. 2011.
- [18]. L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.
- [19]. Babaei, "Optimal topologies for cascaded sub-multilevel inverters," *J. Electron.*, vol. 10, no. 3, pp. 251–261, May 2010.
- [20]. W. K. Choi and F. S. Kang, "H-bridge based multilevel inverter using PWM switching function," in *Proc. Int. Telecomm. Energy Conf.*, 2009, pp. 1–5.
- [21]. J. F. Chen, J. N. Lin, and T. H. Ai, "The techniques of the serial and paralleled IGBTs," in *Proc. IEEE Ind. Electron. Soc.*, 1994, vol. 2, pp. 999–1004.
- [22]. Y. Xiao, B. Wu, F. A. DeWinter, and Reza Sotudeh, "A dual GTO current source converter topology with sinusoidal inputs for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 34, no. 4, pp. 878–884, Jul./Aug. 1998.
- [23]. B. Abdi, A. H. Ranjbar, G. B. Gharehpetian, and J. Milimonfared, "Reliability considerations for parallel
- [24]. performance of semiconductor switches in high-power switching power supplies," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 2133–2139, Jun. 2009.
- [25]. M. H. Rashid, *Power Electronics: Circuits, Devices and Applications*, 3rd ed. Upper Saddle River, NJ: Pearson Education, 2003.
- [26]. R. Strzelecki and G. Benysek, *Power Electronics in Smart Electrical Energy Networks*. London, U.K.: Springer-Verlag, 2008.
- [27]. Z. Ye, P. K. Jain, and P. C. Sen, "A two-stage resonant inverter with control of the phase angle and magnitude of the output voltage," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2797–2812, Oct. 2007.
- [28]. Y. Liang, C. O. Nwankpa, "A Power Line Conditioner Based On Flying Capacitor Multilevel Voltage Source Converter with Phase Shift SPWM," *IEEE Transactions on Industry Applications*, volume 36, number 4, pages 965-971, July 2000.