

Design of Asynchronous Viterbi Decoder using Bundled Data Protocol for Low Power Consumption

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Abstract: This paper proposes a review on the designing of Asynchronous Viterbi Decoder. In order to reduce the power consumption and increase the speed, it is necessary to design Asynchronous Viterbi Decoder. Therefore, the aim is to design Asynchronous Viterbi Decoder by using handshaking protocol. This paper focuses on Bundled data protocol to design Asynchronous Viterbi Decoder. This paper also describes study of various units of Viterbi decoder. Viterbi decoders employed in digital wireless communications are complex and dissipate large power. Asynchronous Viterbi Decoder have significant role in terms of performance because they saves power through not having to generate or distribute a global clock. Instead, timing between blocks is performed by local handshake signals. Asynchronous Viterbi decoders are used in wide range of applications i.e. in Wireless Communications, Digital Television broadcast, Largest applications in cell phones, Pattern recognition, Speech recognition CD ROMS and Magnetic disks etc. In Mobile station Baseband Modem, Viterbi Decoder consumes more than One-third of chip area and power dissipation of the baseband modem. Power efficiency can be increased if total power dissipation is decreased. Battery operated systems required Low power consumption. Asynchronous designs are inherently data driven and are active only when doing useful work, enabling significant savings in power and operating at the average speed of all components.

Keywords: Asynchronous Viterbi Decoder, Bundled Data Protocol, Convolutional Encoder, Viterbi Decoder

I. Introduction

Viterbi decoders are widely used in digital transmission and recording systems and are expected to be used in next generation wireless applications. Viterbi decoding algorithm proposed in 1967 by viterbi, is a decoding process for convolutional codes in memory-less noise. The algorithm can be applied to a host of problems encountered in the design of communication systems. The Viterbi Algorithm (VA) finds the most-likely state transition sequence in a state diagram, gives s symbols sequences. The Viterbi algorithm is used to find the most likely noiseless finite-state sequence, gives sequence of finite-state signals that are corrupted by noise.

This paper presents review of design of Asynchronous Viterbi decoder to reduce power dissipation with increased speed. Section I and II discuss the introduction and advantage of Asynchronous design. Section III explains about the Convolution Encoder. Also section IV discuss the blocks of Viterbi Decoder i.e. BMU, ACS and SMU. At last section V discusses the proposed work of design of Asynchronous Viterbi Decoder using Bundled Data Protocol. Thus the objective of the author is to analyze the performance of the decoder in terms of speed and power.

II. Synchronous Asynchronous Systems

The Viterbi decoder can be implemented by using Synchronous or Asynchronous design options. The majority of logic systems are based on the Synchronous principle because of design simplicity using discrete time, which avoids the hazards. In Synchronous systems, the subsystems change from one state to another state depending on a global clock signal. When the system is tend to become bigger and bigger, the problem of clock skew is becoming a bottleneck for many system designers. And also in synchronous systems, many gates switch unnecessarily just because they are connected to the clock, and not because they have to process new inputs. Due to this, the Synchronous systems consume more power than necessary. Therefore the design of clock-free or Asynchronous systems has thus become attractive for digital system designers during the past few years.

An Asynchronous system means in which there is no global synchronization within the system; subsystems within the system are only synchronized locally by the communication protocols between them. The Asynchronous systems benefits are following :

- Due to fine-grain clock gating and zero stand-by consumption, Low-power consumption is achieved.
- High operating speed by actual local latencies rather than global worst-case latency.

- Due to local clocks tend to tick random points in time, less electro-magnetic emission can be getting.
- Because of the simple handshake interface and the local timing, better composability and modularity will be achieved.
- No clock distribution and skew problems.

III. Convolution Encoder

Viterbi Decoders are commonly used to decode data encoded using convolutional encoders and transmitted over noisy channel. In recent years there has been great interest in the implementation of high-speed Viterbi Decoders for convolutional codes. A convolutional encoder is a Mealy machine, where the output is a function of the current state and the current input. It comprises of one or more shift registers and multiple XOR gates. The stream of information bits flows in to the shift register from one end and is shifted out at the other end. XOR gates are associated to some stages of the shift registers as well as to the current input to generate the output.

Convolutional codes are usually described using two variables, the code rate and the constraint length. The code rate $r=k/n$, is indicated as a ratio of the number of bits into the convolutional encoder (k) to the number of channel symbols output by the convolutional encoder (n) in a given encoder cycle. The constraint length parameter 'K' stands for the length of the convolutional encoder and it indicates how many k -bit stages are available to feed the combinational logic that produces the output symbols. A message encoded using a convolutional encoder follows what is called a trellis diagram which shows the different states of the encoder as well as the path taken to encode an arbitrary message. Viterbi's algorithm tries to reconstruct this correct path based on the received stream, despite errors in the received stream. This is done by reconstructing the trellis diagram and allocating a weight to each branch and node (i.e.state) of the reconstructed trellis, at each time slot. These weights define the likely branches and nodes used by the encoder. This is referred to as the Maximum Likelihood Probability (MLP). By tracing back through the reconstructed trellis, the decoder can detect and correct errors in the received stream.

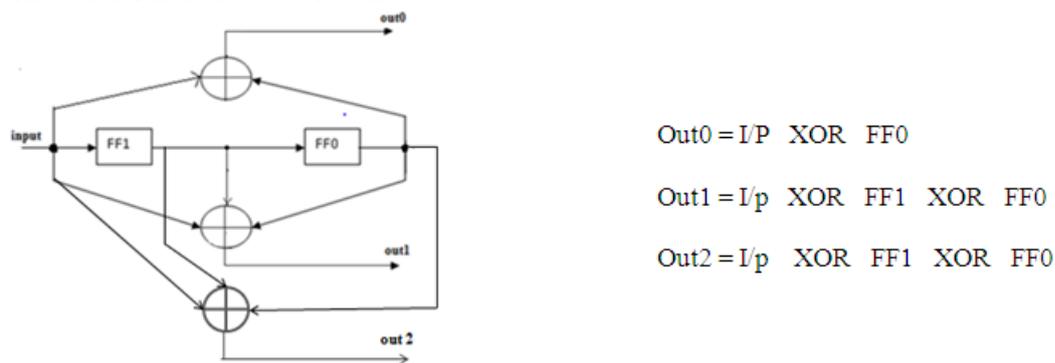


Figure 1. Convolution Encoder

IV. Viterbi Decoder

A Viterbi Decoder is composed of three basic computation units which are Branch metric unit (BMU), Add compare select unit (ACSU), Survivor-path memory unit (SMU), and Path metric unit (PMU). The branch metric computation block compares the received code symbol with the expected code symbol and counts the number of differing bits. Branch matrices are fed into ACSU which performs add compare and select operation for all the states. The decision bits produced in ACSU are stored and regained from the SMU in order to finally decode the source bits along the final survivor path. The decoded output sequence is determined by tracing back the information from the recorded survivor paths. The core elements of PMU are ACSU units. The path metrics of the current iteration are stored in the path metric unit (PMU) and are read out for the use of next iteration.

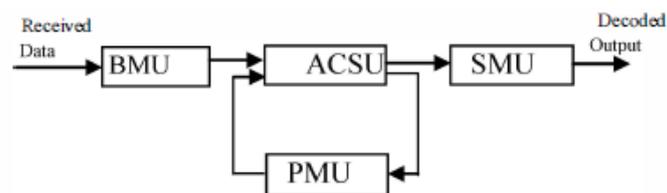


Figure 2. Viterbi Decoder

V. Proposed Asynchronous Viterbi Decoder

Asynchronous circuits are composed of blocks that communicate to each other using handshaking via Asynchronous communication channels, in order to achieve the necessary synchronization, communication, and sequencing of operations. To design Asynchronous Viterbi Decoder we have to take care of optimization of ACS unit and SMU units as it consumes more power. Asynchronous communication channel consists of a bundle of wires and a protocol to communicate the data between the blocks. There are two types of encoding scheme in Asynchronous channels. If the encoding scheme uses one wire per bit to transmit the data and a request line to identify when the data is valid is called single-rail encoding. The associated channel is referred a bundled-data channel. Alternatively, in dual-rail encoding the data is sent using two wires for each bit of information. In the proposed Asynchronous design of Viterbi decoder 4 phase Bundled Data Protocol scheme is used.

Bundled Data Protocol comprise data signals that use normal Boolean levels to encode information, and have separate request and acknowledge wires bundled with the data signals. It is also called as, single rail protocol. Bundled-data protocol is also categorized in two types – 4 phase bundled-data protocol & 2 phase bundled-data protocol. The bundled-data protocol uses a single request (acknowledge) wire and a set of data wires hence it is called as bundle as shown in fig.3. The request wire is used to inform the receiver about the validity of the data on the data bundle. This inherently places a constraint on the request wire, known as the bundling constraint. As stated in this constraint, the request wire must be asserted only after the bundled data is valid at the receiver end.

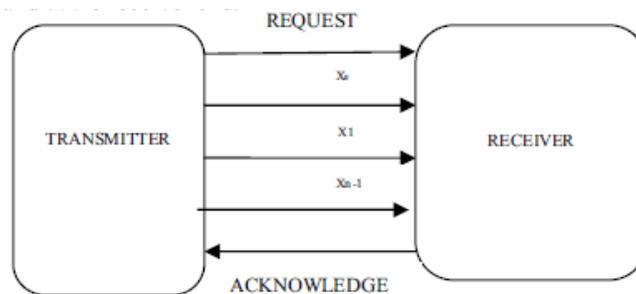


Figure 3. Bundled Data Protocol

The bundled-data protocols rely on delay-matching. This means that data should be before request just as on sender output as receiver output.

The 4-phase bundled-data protocol is based on level-signaling. The time diagram is in **Fig. 4.a**. It is simple, but superfluous return-to-zero cost time and energy. The whole transmit or processing data cycle consists of 4 phase. This means that 4-phase refers to the communication actions:

- The sender issues the data and sets request high,
- The receiver consumes the data and sets acknowledge high,
- The sender responds by taking request low, at which Point the data is no longer guaranteed to be valid and,
- The receiver acknowledges this by taking acknowledge low. At this point the sender may begins the next communication cycle.

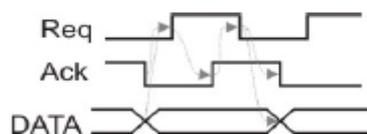


Figure 4.a. 4 Phase Protocol

The 2-phase bundled-data protocol is based on transition-signaling, see **Fig. 4.b**. The information is encoded by signal transition. If the information on the request and acknowledge wires is encoded as signal transitions on the wires and there is no difference between 0→1 and 1→0 transition, the protocol is called as two-phase protocol.

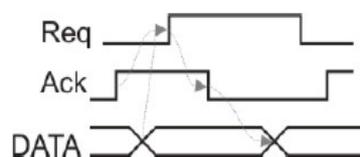


Figure 4.b. 2 Phase Protocol

Ideally, the 2-phase bundled-data protocol should be faster than the 4-phase, but result depend on a particular design. . Contrary to 4-phase, a 2-phase bundled-data circuits are faster but they are more complex and have more complex circuit implementation. Therefore, we will use 4 phase bundled-data protocol. And for the simulation results, we will use Model Sim tool in Verilog.

VI. Proposed Work

Finally aim is to design the Asynchronous Viterbi Decoder to reduce power consumption while maintaining the speed for wireless communication applications.

Objectives :

- 1) To design Convolution Encoder for constraint length $K=3$ and code rate $r=1/3$ and input bit $k=1$.
- 2) To design blocks of Viterbi Decoder and simulation using VHDL.
- 3) To design Asynchronous Viterbi Decoder system by applying Handshaking Protocol i.e. Bundled Data Protocol.

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