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Soft Switched Resonant Converters with Unsymmetrical Control

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Abstract: *Using PSPICE a resonant dc-dc converters operating at constant frequency was simulated. The paper concentrates on the working of a half bridge topology employing ZVS techniques. The operation of converter with LC filter in the output is discussed. The design and fabrication was done on a 5V, 50W converter using MOSFET to validate the performance of the converter. The converter has illustrated low reverse voltage, less current stresses and negligible conductivity losses owing to unsymmetrical duty ratio operation and zero voltage switching. This topology exhibits the merits of both resonant (zero switching loss) converters and switched mode (low conduction loss) circuits.*

Keywords: *Asymmetrical pulse width modulated (APWM , Half bridge converter, Gate pulse, Switched mode power supplies (SMPS), Unsymmetrical duty ratio, Zero Current Switching (ZVS), Zero voltage switching (ZVS),*

I. Introduction

Conventional resonant dc - dc topologies use frequency modulation technique to achieve soft switching and output regulation, which is undesirable because the frequency range can be very wide [1], [2],[5],[7]. At these variable frequencies the magnetic components and filter design create severe problems. To account for this, constant frequency operation came into picture which helps to overcome some limitations. However the soft switching conditions are lost when duty cycle is lowered owing to resonance problems [3], [6]. Hence this paper introduces asymmetrical pulse width control (APWM) or unsymmetrical duty ratio control of power devices / switches at constant frequency. The topology under study is half bridge utilizing Zero voltage switching (ZVS).

II. Asymmetric duty cycle PWM converter.

In any resonant topologies soft switching conditions (ZVS or ZCS) for power device transitions are achieved by either using the passive elements or auxiliary components[1],[7]. A passive element comprises of L and C while the diodes and power devices like MOSFET, IGBT etc. forms the auxiliary components. Even sometimes the leakage inductances of the transformer and parasitic capacitance of the semiconductor device are used to provide resonance. The soft switching converters use either Zero voltage switching (ZVS) or Zero current switching (ZCS) for turning ON and OFF the power devices.

The paper focuses on a half bridge converter with ZVS – clamped condition owing to its better-quality performance unlike full bridge topologies [4]. In this topology, the turn ON and OFF of the power devices takes place at zero voltage.

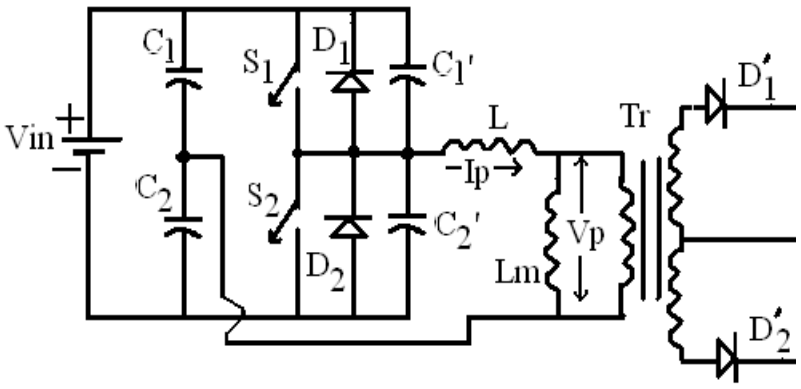

Fig.1 Half bridge ZVS-Clamped voltage configuration

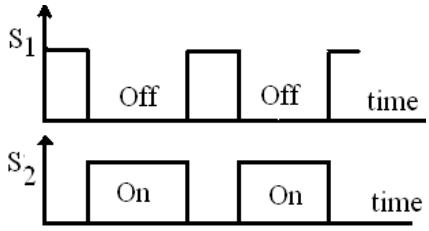

Fig.2 Gate pulse for APWM control

Consider a half bridge topology is shown in fig.1. Using APWM technique[6] operate one switch/power device with less than 50% and the other with greater than 50% duty cycle to exploit inductive "ring" for lossless switching. The gating pulse for APWM controlled half bridge converter is shown in Fig.2.

In this scheme the peak reverse voltages of the power devices are clamped at the input voltage level. The capacitor across each device makes sure the power device get turned on only at zero voltage. Else the charge in the capacitor gets dissipated through the power device or switch. The diode connected anti parallel to the power device must conduct prior to the gating of the power device. However, this converter has the disadvantage of high device/switch currents [4],[8].

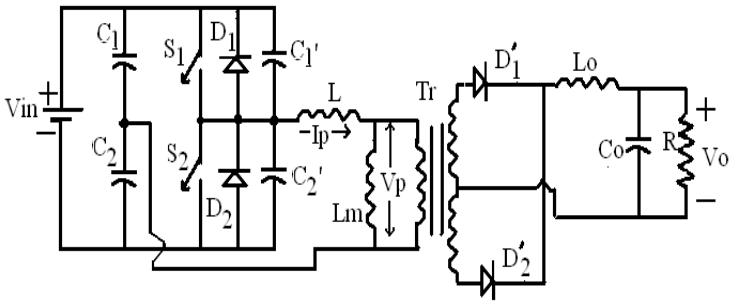

Fig.3 Half bridge LC filter circuit

Fig 3 shows the half bridge topology with inductive filter. Input capacitors C_1, C_2 have the same value and divide the supply voltage V_s such that $Vc_1 + Vc_2 = V_s$. L_m is the transformer magnetizing inductance and L the leakage inductance of primary winding, if necessary an external inductor. $\mathbf{C_1'}$ and $\mathbf{C_2'}$ can be the device parasitic capacitance or external. The operation of the above converter lies in the variation of duty cycle in the range of either 0 to 0.5 (minimum to maximum output) or 0.5 to 1.0 (maximum to minimum output).

In inductive filter configuration, an additional inductor L_o is used. The inductor L will be much less than L_o value [5], reflected onto the primary side of the transformer. Here the transformer is voltage fed and hence secondary voltage is rectified and fed to the L_o C_o filter. Unlike capacitive filter [], here primary currents are rectangular in shape.

III. Design

As per equal area criterion the capacitor voltages Vc_1, Vc_2 must satisfy the condition to maintain balanced volt-seconds on the transformer primary [1] as shown in fig.3. Vp, Ip are the transformer primary voltage and current.

Vc_1 D = Vc_2 (1-D) (1) where Vc_1, Vc_2 are the voltages across C_1 and C_2 .D is the duty ratio. V

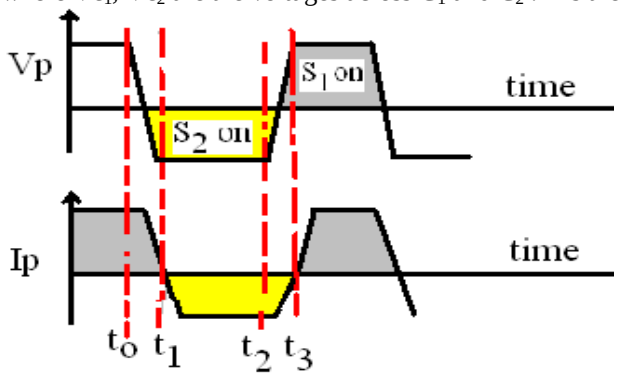

Fig.4 Half bridge APWM waveforms

The output voltage is given by [1],[6]

$$Vo = \frac{[Vc_1 D + Vc_2(1-D)]}{n} \quad \text{- (2)}$$

Where Vo is the output voltage and n is the number of turns.

The equation for the current through the power devices S_1, S_2 and Io, output current are given by the authors in reference [6].

$$I_1 = \frac{2Io(1-D)}{2}$$

$$I_2 = \frac{2IoD}{2}$$

-(3)

Finally to achieve lossless switching the boundary condition [1] must be fulfilled.

$$\mathbf{LI_2^2 = C_e Vc_1^2} \quad \textbf{(4)}$$

Where C_e is parallel equivalent of C_1' and C_2'.

Duty cycle in the range of 0 to 0.5 is selected. The current in L_o is assumed to be continuous. Transformer secondary side leakage inductance, forward drop and capacitance of the output diodes are neglected.

For successful implementation of ZVS, a minimum dead time between the turn of one switch and turn off of other must be incorporated. The minimum time depends on the value of the primary current Ip, the inductor value L, the value of capacitances $\mathbf{C_1'}$, $\mathbf{C_2'}$ and input supply voltage. Bigger the first two factors the smaller will be the minimum time whereas larger the later factors, the bigger the minimum time. Increase in later factors may cause difficulty in attaining ZVS [8].

For better results a variable dead time based on the conduction of body diode (D_1, D_2) can be implemented.

IV. Hardware Fabrication

Specifications:

1. Input Voltage Vin = 48V
2. Output Voltage Vo = 5V
3. Load current Io = 10A
4. Switching frequency fs = 20 KHz.

The maximum operating duty ratio is selected at 0.4. The turns ratio 'n' is selected as 4 to keep the peak current value lower. For designing the transformer [1],[3], the conventional Area product approach was used. The voltage across the transformer primary is a square wave. Hence while designing the transformer, the form factor was assumed to be 1.

The fabricated transformer parameters for converter with LC filter are given in Table 1.1. The leakage inductance so obtained are by varying the air gap. Hence no external inductance was required for the half bridge topology. Fig 5 shows the circuit diagram for experimental setup.

Table 1.1

Leakage inductance	20.5µH
Magnetizing inductance	97 µH
Secondary Leakage inductance	22.5 µH
Primary resistance	1.2 ohms
Primary number of turns	12 turns
Secondary number of turns	3 + 3 turns (centre Tapped)
Winding wire size (both primary & secondary)	SWG -13

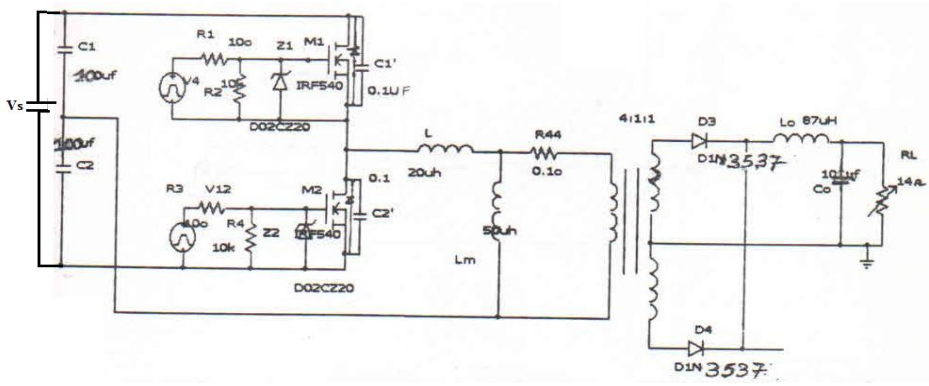

Fig 5 Hardware circuit diagram

V. Circuit Implementation

The power devices gate pulse circuit consisted of ICL8083 Precision waveform generator, IR2110 high speed MOS driver, operational amplifier LM324 and LM311. Complementary gate pulse were generated using NOR gates CD4001. A small delay of 0.15µs was introduced between gate pulses using CD4081. MOSFET are provided with heat sinks. The input voltage source of 48V is derived from 4*12 V batteries. The output comprises of a rheostat 14 ohms, 12A two rectifier diodes IN3537 and LC filter. By varying the control voltage to the comparator LM311 the pulse width of the gate signal can be varied. Fig.6 shows the circuit diagram for PSPICE simulation purpose.

MOSFET and output diode ratings depend on the duty ratio, output voltage and load current MOSFET, IRF 540, output diodes IN3537 and ferrite core transformer were chosen for this configuration. Capacitance value C_1' and $\mathbf{C_2}'$ of 0.1µf (from equation 2) across each MOSFET and the output filter of 10µf are selected. Based upon the equation 4 the output inductor Lo valued of 87µF is preferred. A maximum dead time of 0.2µs and minimum of 0.1µs is observed. Thus 0.15µs is taken for simulation and fabrication.

Since the network was bread boarded, the rated current of 5A was passed only for a short time to verify the ZVS characteristics of the power devices.

VI. Discussion

Certain constraints on the value of the input capacitance are observed during PSPICE simulation. C_1 and C_2 values greater than 100µF results in high current spikes across the devices. Hence series combination of 2 * 470µF capacitor is used. However with values of C_1' = $\mathbf{C_2}'$ = 0.01µF stress on primary voltage Vp is more than that observed for C_1' = $\mathbf{C_2}'$ = 0.1µF .

Only the fundamental component was found to be dominant during the Fourier analysis of the output waveform using PSPICE.

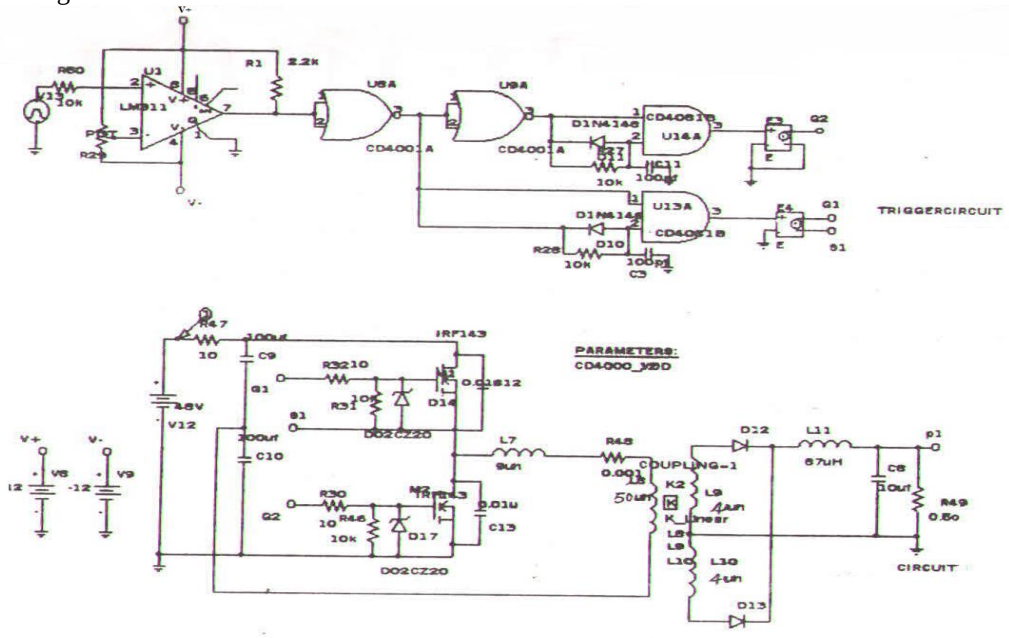

Fig6. Triggering and Power circuit in PSPICE

VII. Results

Fig.7 a & b depicts Vp primary voltage, Ip current and Vo output voltage from the experimental setup with duty ratio of 0.4. From the waveforms it is evident that drain to source voltage drops to zero before the power device gets turned on. Hence the volt time balance is maintained. Similarly the waveform of Ip verifies the equal area criterion. Net area for one cycle is zero even though the waveforms of Vp and Ip do not posses half wave symmetry as in fig 7. Thus achieving the APWM control.

Fig.8 a, b & c depicts the simulated waveform for the converter fabricated above. The simulated primary voltage and current waveforms also show turn ON and turn OFF of the MOSFET occur at zero voltage. The shaded portion in fig 8 marks the region where switch transition must take place to ensure ZVS technique.

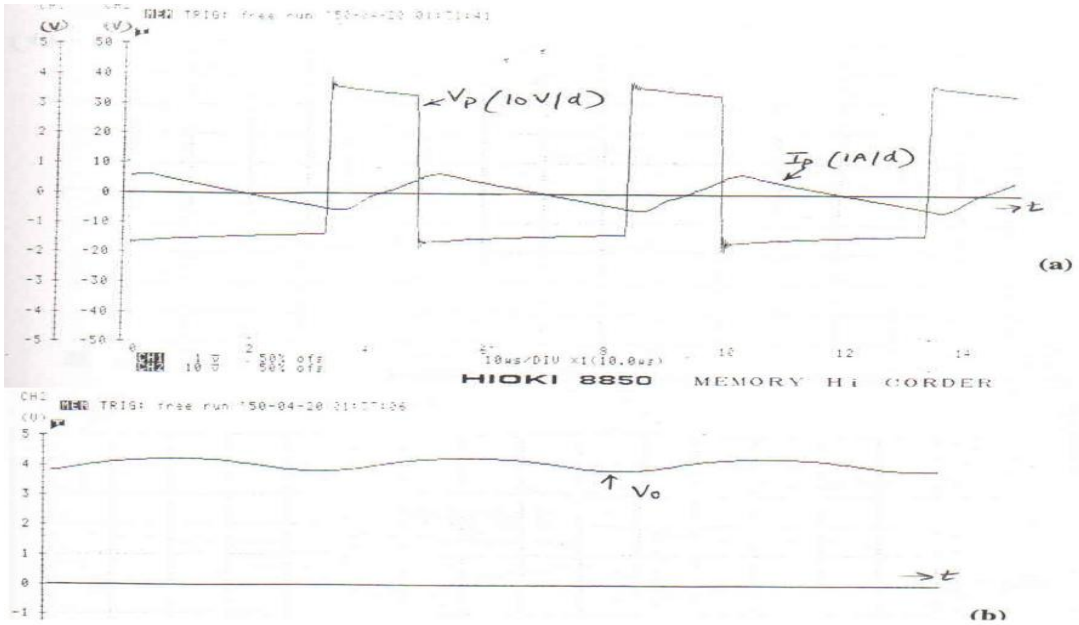

Fig.7. a) Vp, Ip b) Vo for experimental circuit

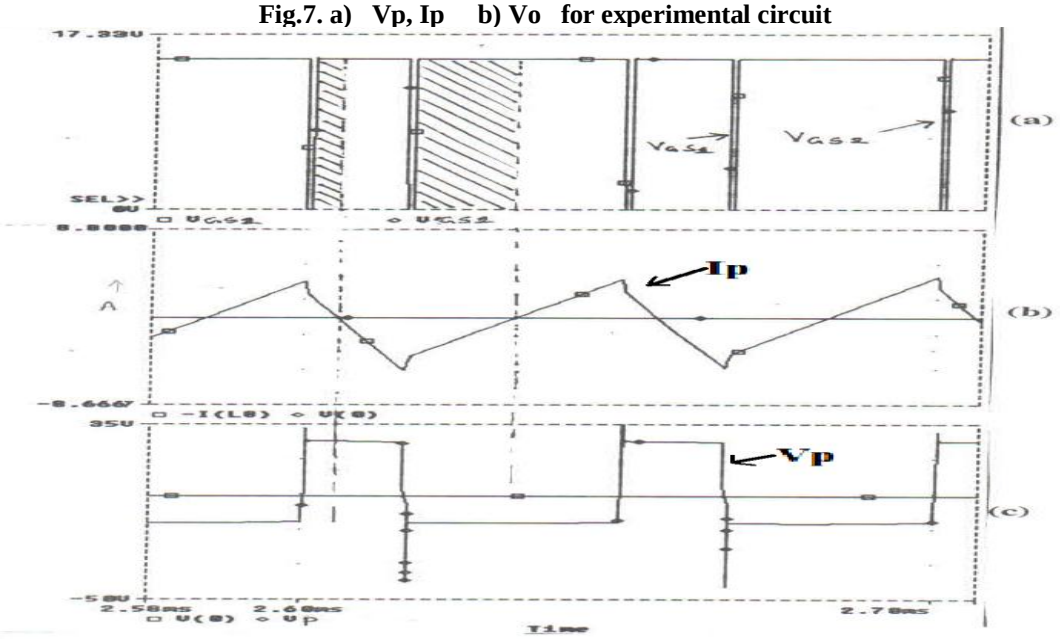

Fig8. a) Gating pulse for S_1 ans S_2 b) Primary voltage c) Primary current for LC filter in PSPICE

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VIII. Conclusions

Both the PSPICE simulation and experimental results obtained confirms ZVS at fixed frequency for a 5V, 50W dc-dc converter using APWM method. Less complex circuits, low voltage and current stress on device are the few advantages with this soft switching technique. However the output voltage is less owing to voltage drop across secondary inductance and filter at high loads.

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