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Design of BCD to Floating Point Converter Based On Single Precision Format

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ABSTRACT : *The requirement for floating point arithmetic operations in most of the commercial, financial and internet based applications is increasing day by day. Computation with floating point arithmetic is an absolutely important task in many Mathematical applications and accounts for most of the scientific operation. Adder is basic element of complex arithmetic circuits, in which inputs should be given in standard IEEE 754 format. The main objective of the work is to design a BCD to IEEE 754 floating point converter for representing 32 bit single precision floating point values. The proposed converter at the input side of the existing floating point adder/subtractor module helps to improve the overall performance of the design. Very High Speed Integrated Circuit(VHSIC) Hardware Description Language(VHDL) is used to write the modules.*

Keywords - *IEEE 754 format, Floating point arithmetic, single precision,*

I. INTRODUCTION

In BCD each digit of a decimal number is directly coded as a 4 bit binary number between 0 to 9. For example, the number (4921)10 = (0100 1001 0010 0001) BCD. We can see that each digit of the decimal number is coded in binary and then link together to form the BCD representation of the decimal number. Any BCD digit that lies between (0, 9) or (0000, 1001), multiplication of two BCD digits can result in numbers between (0, 81),[1].

The demand for floating point arithmetic operations in most of the applications such as commercial, internet based and financial field is increasing day by day.floating point arithmetic is used in many commercial, financial and internet based applications. Hence it becomes necessary to find out an option to give BCD numbers directly as input for these applications. This is much easier and also helps in saving time. But In the current scenario, the BCD inputs cannot be given as such, we needs to be convert the input to the sign, exponent and mantissa form. because, in the adder or subtractor, inputs should be given in IEEE 754 format[2,3]. Hence in this work we are going to design BCD to floating point converter for single precision bits which will solve this issue to an extent.

The converter we are going to design here is based on IEEE single precision format and this is 32 bits wide. The IEEE-754 standard specifies six numerical operations. such as multiplication, division,addition, subtraction, remainder, and square root. The IEEE 754 standard also specifies some rules for converting to and from the different floating-point formats. In order to get full functionality of the design ,The proposed converter can be added into the already existing adder/subtractor. The main difference between fixed point and floating point digital signal processors is their respective numeric representation of data. Fixed point hardware performs strictly integer arithmetic,Whereas floating point digital signal processors (DSPs) support integer or real arithmetic, And latter normalized in the scientific notation. Single precision operations, provides greater accuracy as well as precision than fixed point devices because of its wider word width, exponentiation and correct internal representations of data. With floating point format, real arithmetic can be directly coded into hardware operations.While Fixed point devices had to implement real arithmetic indirectly through software routines which require development time and many algorithmic instructions. The BCD input given will range from 0-9 which is the maximum input range that can be provided which will satisfy the exponent range in the 32 bit IEEE 754 single precision format.

Many people considered Floating-point arithmetic is an esoteric subject. Rather this is surprising because floating-point is present everywhere in computer systems. Almost each language has a floating-point datatype; from PCs to super-computers all have floating-point accelerators; most compilers will be called to compile floating-point algorithms from time to time.

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II. ABOUT IEEE 754 FLOATING POINT FORMAT

IEEE 754 standard is issued by the Institute of Electrical and Electronics Engineering (IEEE) for binary floating point arithmetic in 1985[5,6,7].Later revised version of the existing standard in developed in 2008. There are five basic floating point formats. Out of five basic formats, three formats are binary floating point formats and two are the decimal floating point formats. The first two binary formats are called 'Single precision',that is this format contain 32 bits and 'Double precision' that consist of 64 bits respectively.In this project We consider only IEEE Single precision format alone. And it is described below.
Single precision format uses 1-bit for sign bit,8-bits for exponent and 23-bits to represent the fraction as shown in Fig.[2,8]

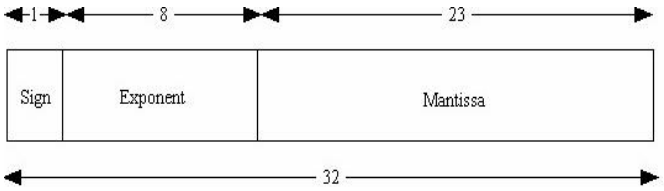

Fig 1.IEEE 754 single precision format

As shown in Fig.1 Sign bit determines the sign of a number, which is either 0 for a non-negative number or 1 for a negative number. In IEEE single precision format, a bias of 127 is added to the exponent. The significant or mantissa is composed of an implicit leading bit with value 1, in IEEE 754 it is necessary to represents the values in normalized form, therefore there is no need to show the implicit'1' bit, hence precision is increased[2].

III. CONVERSION PROCEDURE FOR BCD TO FLOATING POINT

Procedure for Converting a BCD number into an IEEE 754 format using the following outline :
• Consider a BCD number Example:- 9
• Convert the number into binary. Shift and subtract-3 Algorithm is used to convert the BCD number into binary.
• The Binary representation of 9.0 is given as 1001.0000
Also in IEEE 754 binary32 format values need to be represented in normalized form given as 1.0010000 x23
• From this, The exponent is 3,and in the biased form it is Add the power with 127 to form the exponent given as 127+3=130 represented as 10000010 in binary form.
Therefore 127+3=130 = (1000 0010)2.
• The fraction is 0010000 (looking to the right of the binary point)
Adjust the result to produce the final conversion.
•The resulting IEEE 754 (single precision) 32 bit format representation of
9 as: 0-10000010-00110000000000000000000.

IV. CONCLUSION

In this work our aim is to design the BCD to Floating point conversion for single precision format only i.e. output will be in sign, exponent and mantissa form .Simulation can be done using XILINX Integrated Software Environment Design Suite 9.1i.

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