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Comparative study of different PWM Strategies for Three Phase three-level Diode Clamped Multi-level Inverter

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Abstract: *This paper presents unipolar pulse width modulation technique with sinusoidal sampling and Space vector pulse width modulation are analyzed for three-phase Diode clamped multi-level inverter from the point of view of the Phase voltages, currents, voltage across the split capacitors and Total harmonic distortion. The necessary calculations for generation of PWM for the two modulation strategies have presented in detail. It is observed that the unipolar modulation ensures excellent,close to optimized pulse distributionresults but THD is high compared to SVPWM. Theoretical investigations were confirmed by the digital simulations using MATLAB/SIMULINK software.*

Keywords: *Three-level diode clamped inverter; unipolar PWM; SVPWM; THD;*

I. INTRODUCTION

In the region of high voltage and power, a high quality inverter fed ac drive is more easily obtained by the use of multi-level and in the first turn of three-level - inverters. Theneutral point clamped three-level inverter topology ispresented in Figure.1. Several PWM methods for this inverterhave been elaborated previously [1-5]. The pulse width modulation (PWM) strategies are the most effective to control multilevel inverters. The unipolar PWM and space vector PWM are the most preferred pwm control techniques. Even though space vector modulation (SVM) is complicated, it is the preferred method to reduce power losses by decreasing the power electronics devices switching frequency, which can be limited by pulse width modulation. Different aspects of the three-level NPC inverter will be discussed including the inverter topology. The operation theory will be discussed with the aspect of Unipolar PWM and space vector pulse width modulation [6-8]

In this paper the Unipolar PWM and spacevector PWM strategy of three-level inverters are compared for THD.The paper mainly deals withthe computation and the comparison of the motor harmonicclosses of different PWM solutions and with the selection ofthe solutions providing the best results. Finally, the driveharmonic losses will be compared for each technique.

II. THREE-PHASE NEUTRAL POINT CLAMPED MULTI-LEVEL INVERTER

The three phase neutral point clamped (NPC) or Diode clamped Multi-Level Inverter topology shown in figure.1 by Nabae et al will have

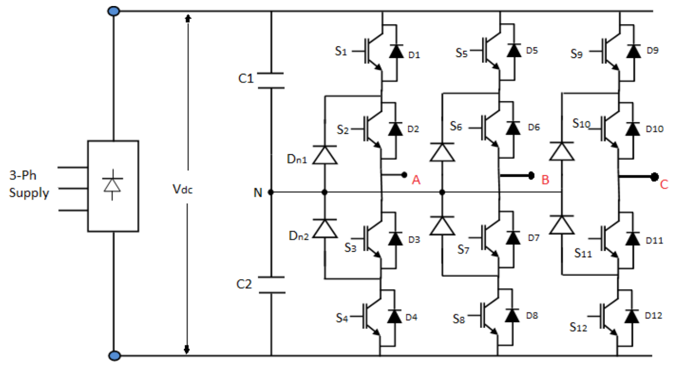

Figure.1 Three-level NPC inverter

Three-level inverter NPC inverter is shown in Figure1. Each leg contains four active switches S_1 to S_4 with anti-parallel diodes D_1 to D_4. The capacitors at the DC side are used to split the DC input into two, to provide a neutral point N. The clamping diodes can be defined as the diodes connected to the neutral point, D_{n1}, D_{n2}. When switches S_2 and S_3 are connected, the output terminal A can be taken to the neutral through one of the clamping diodes. The voltage applied to each of the DC capacitors is E, and it equals half of the total DC voltage $V_{d.}$ [13-14]

Switching states pertaining to three-level inverter are shown in Table. 1 can represent the operating status of the switches in the three-level NPC inverter. When switching state is ‘2’, it is indicated that upper two switches in leg A connected and the inverter terminal voltage V_{A0} , which means the voltage for terminal A with respect to the neutral point Z, is +E, whereas ‘0’ denotes that the lower two switches are on, which means V_{A0} = -E. When switching state ‘1’, it indicates that the inner two switches S_2 and S_3 are connected and V_{A0} =0 through the clamping diode, depending on the direction of the load current i_A . When D_{Z1} is turn on, the load current will be positive ($i_A > 0$) and the terminal A will be connected to the neutral point Z through the conduction of D_{Z1} and S_2 . Table 3 shows switching status for leg A. Leg B and leg C have the same concept.[12-14]

A. Unipolar PWM Technique applied to Three-level Diode Clamped Inverter.

The unipolar PWM method offers a good opportunity forthe realization of the Three-phase inverter control. In caseof the three level inverters it is better to use theunipolar PWM method with three carrier waves.

In such case the motor harmoniclosses will be considerably lower.

In this scheme, the triangular carrier waveform is compared with two reference signalswhich are positive and negative signal. The basic idea to produce SPWM with unipolar voltageswitching is shown in Figure 2. The different between the Bipolar SPWM generators is that thegenerator uses another comparator to compare between the inverse reference waveform−Vr. Theprocess of comparing these two signals to produce the unipolar voltage switching signal isgraphically illustrated in Figure 2. In Unipolar voltage switching the output voltage switchesbetween 0 and V_{dc}, or between 0 and $-V_{dc}$. This is in contrast to the Bipolar switching strategy inwhich the output swings between $V_{dc}$and $-V_{dc}$. As a result, the change in output voltage at each

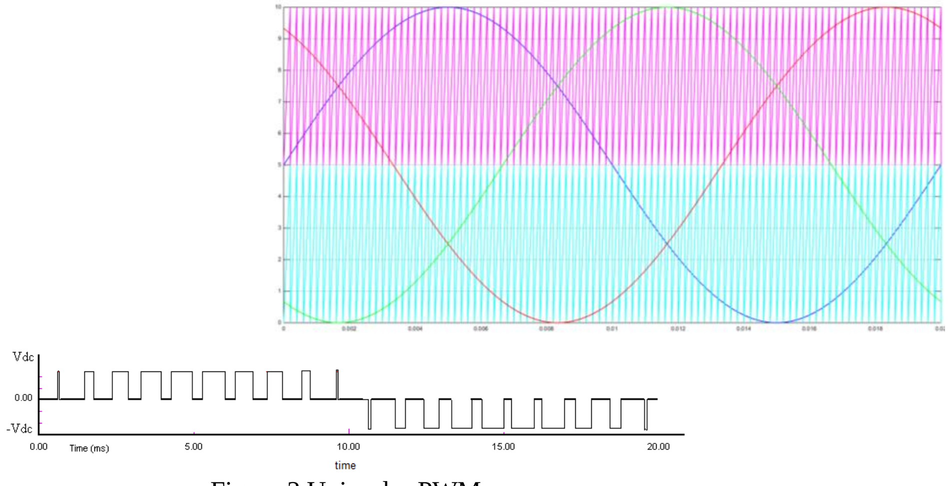

Figure 2.Uni-polar PWM

B. Three Phase three Level Inverter using Space Vector Modulation Technique

The space vector diagram of any three phase n-level inverter consists of six sectors. Each sector consists of $(n-1)^2$ tri-angles. The tip of the reference vector can be located within any triangle of a sector. Each vertex of any triangle represents a switching vector. A switching vector represents one or more switching states depending on its location. There are n^3 switching states in the space vector diagram of n-level inverter. The SVM is performed by suitably selecting and executing the switching states of the triangle for the respective on-times. It is also known as “Nearest three vector” concept. The performance of the inverter significantly depends on the selection of these switching states.

i. principle of operation

The space vector modulation diagram of three level as shown in figure 3. There are six sectors (S_1 to S_6) in which again each sector is having four regions A_i, B_i, C_i and D_i where i=1.2…6 corresponding to all sectorsand total of 27 i.e. 3^3 switching states are available in this space vector diagram. As the level n increase the number of regions in each sector, switching states and on-time calculations will increase. This can be little complex when moving to the higher level.[12]

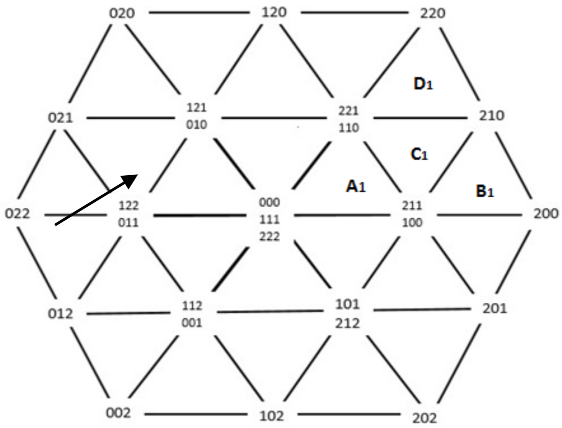

Figure 3.Switching vectors along each sector and region

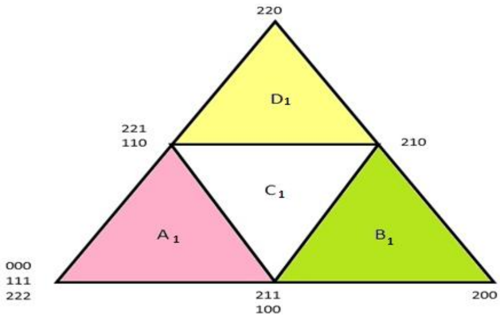

Figure 4.Four regions of sector-1

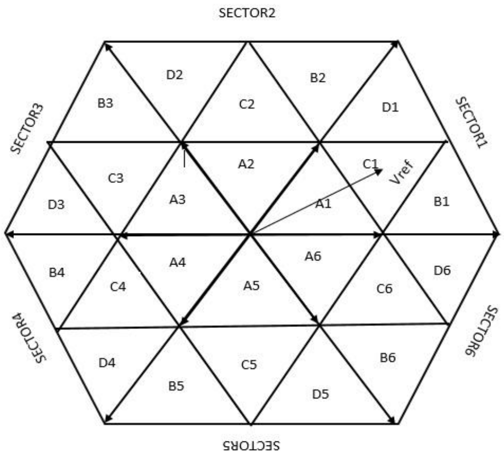

Figure.5 Division of sectors and regions for three-level inverter

TABLE 1DEFINITION OF SWITCHING STATES

Switching state	Device switching state (phase A)				Output pole Voltage
	S_1	**S_2**	**S_3**	**S_4**	
2	on	on	off	off	**+E**

1	off	on	on	off	**0**
0	off	off	on	on	**-E**

ii. Stationary Space Vectors of three-level Inverter

Three switching states [1], [0] and [2] can represent the operation of each leg. By taking all three phases into account, the inverter has a total of 27 possible switching states. Table 4, shows the possibility of three phase switching states that are represented by three letters in square brackets for the inverter phases A, B, and C. Table 3.2 shows the 27 switching states that are shown in Table 2.

TABLE 2 VOLTAGE AND SWITCHING STATES

Space Vector	**Switching State**	**Vector Classification**	**Vector Magnitude**
V_1, V_2, V_3	[2 2 2], [1 1 1] [0 0 0]	Zero vectors	0
V_4, V_5	100, 211	Small Vectors	$\frac{1}{3}V_d$
V_6, V_7	110, 221		
V_{11}, V_{12}	010, 121		
V_{15}, V_{16}	011, 122		
V_{19}, V_{20}	001, 112		
V_{22}, V_{23}	101, 212		
V_9	210	Medium vectors	$\frac{1}{\sqrt{3}}V_d$
V_{13}	120		
V_{17}	021		
V_{21}	012		
V_{25}	102		
V_{27}	201		
V_8	200	Large vectors	$\frac{2}{3}V_d$
V_{10}	220		
V_{14}	020		
V_{18}	022		
V_{24}	002		
V_{26}	202		

The voltage has four groups

I. Zero vector (V_0), representing three switching states [1 1 1], [0 0 0] and [2 2 2]. The Magnitude of V0is Zero.
II. Small vector (V_1 to V_6), all having a magnitude of V_d /3. Each small sector has two switching states, one containing [1] and the other containing [2] and they classified into P or N- type small vector.
III. Medium vectors (V_7 toV_{12}), whose magnitude is $\frac{\sqrt{3}}{3}V_{d.}$
IV. Large vectors (V_{13} to V_{18}), all having a magnitude of $\frac{2}{3}V_{d.}$

ii. Time Calculation using Volt-sec balance concept

The space vector diagram that is shown in Figure 9 can be used to calculate the time for each sector (I to VI). Each sector has four regions (1 to 4), as shown in figure 6, with the switching states of all vectors as shown in Table 4. By using the same strategy that was used in two-level inverter, the sum of the voltage multiplied by the interval of chose space vector equals the product of the reference voltage $V_{ref}$and sampling period T_S. To illustrate, when reference voltage is located in region 2 of sector I then the nearest vectors to reference voltage are V_1 ,V_7,and V_2 as shown in Figure 8, and the next equations explain the relationship between times and voltages

$$\overrightarrow{\mathbf{V_{ref}}}\ \mathbf{T_s} = \overrightarrow{\mathbf{V_1}}\mathbf{T_a} + \overrightarrow{\mathbf{V_7}}\ \mathbf{T_b} + \overrightarrow{\mathbf{V_2}}\mathbf{T_c} \qquad (1)$$

$$\mathbf{T_s} = \mathbf{T_a} + \mathbf{T_b} + \mathbf{T_c} \qquad (2)$$

Where T_a, Tband $T_c$are the times for V_1, V_7 and V_2 respectively

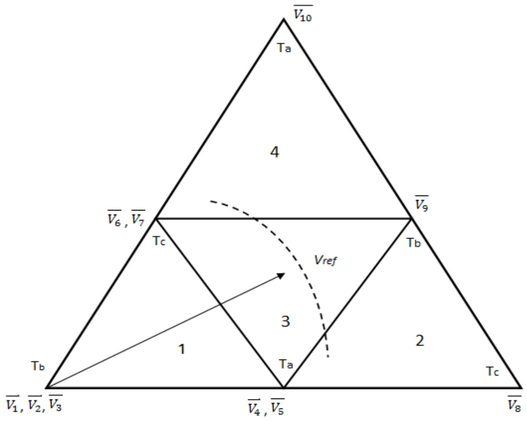

Figure.6 Voltage vector I and their times in sector I

TABLE 3 TIME CALCULATION FOR REF **V** IN SECTOR I

Region	**Ta**	**Tb**	**Tc**
1	Ta=2kTs[sin(60-θ)]	Tb=2Ts[1(2ksin(θ+60))]	Tc=2kTs[sin(60-θ)]
2	Ta=2Ts[1-(ksin(θ+60)]	Tb=2kTs[ksin(θ)]	Tc=Ts[(2ksin(60-θ))-1]
3	Ta=Ts[1-2ksin(θ)]	Tb=Ts[(2ksin(θ+60))-1]	Tc=Ts[(2ksin(θ-60)+1]
4	Ta=Ts[(2ksin(θ))-1]	Tb=2kTs[sin(60-θ)]	Tc=2Ts[1-ksin(θ+60)]

The times can be calculated for sectors (II to VI) by using the equations in table 5 with multiple of π / 3 subtracted from the actual angular displacement θ, such that modified angle falls into the range between zero and π / 3 for use in the equations as in two-level Inverter.

iii. The Switching States by Using Switching Sequence.

By considering the switching transition and using sequences direction, shown in Figure 12, the direction of the switching sequences for all regions in six sectors can be derived and the switching orders are given in the tables below, which are obtained for each region located in sectors I to VI, if all switching states in each region are used..

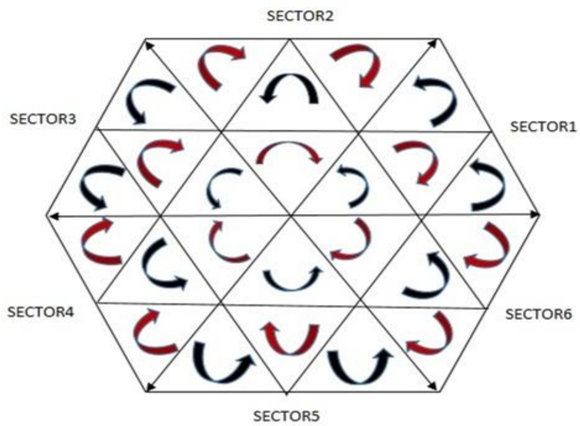

Figure7.Switching sequence for three-level SVM inverter

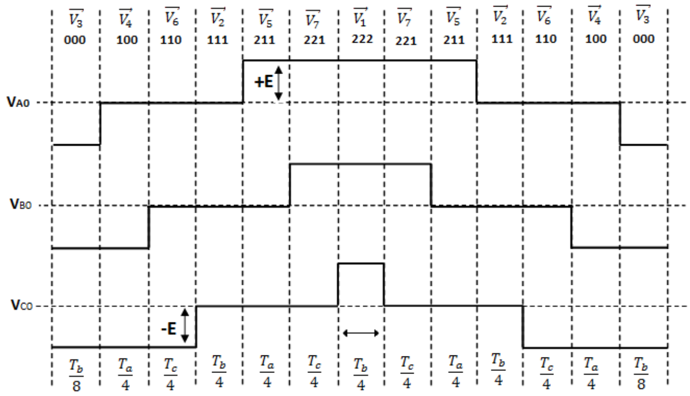

Figure.8 switching sequence of thirteen segments for V_{ref} in sector-I of region-1

The figure 8 represents the switching states corresponding to each switching vector position in region-I as an example.

III. SIMULATION RESULTS

The simulation of diode clamped multi-level inverter with proposed comparison of control strategies applied to three phase three-level diode clamped multi-level inverter is shown in figure 9.

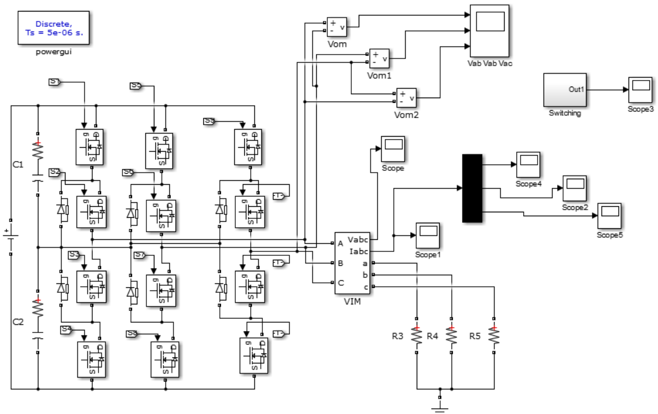

Figure 9.Three-level diode clamped Multi-level inverter

A. Unipolar PWM Technique applied to inverter

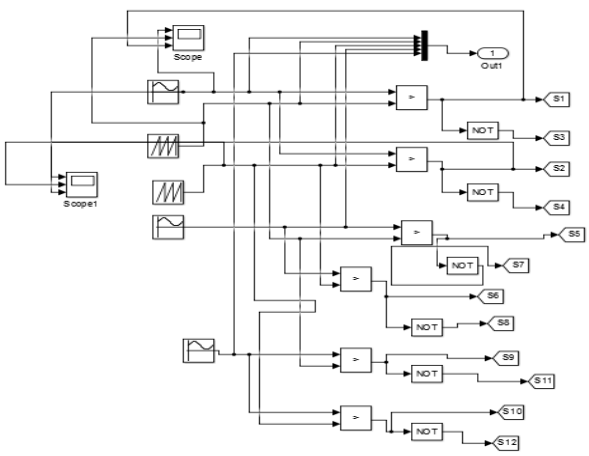

Figure.10 Unipolar PWM technique

As per the principle of unipolar pwm three reference sine and two carrier waves are compared as shown in figure.2 for pwm signals. The generated signals are as shown in figure 11.

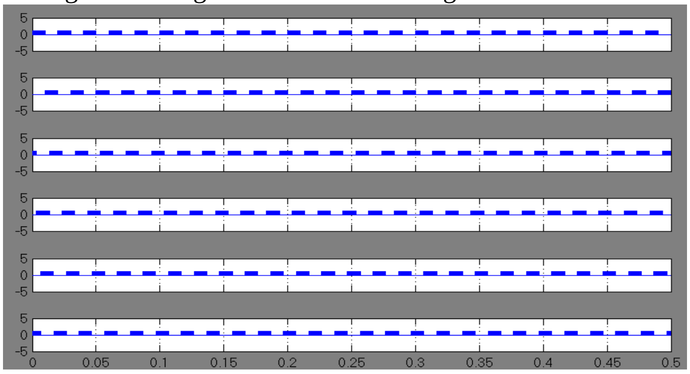

Figure.11Switching pulses using unipolar PWM

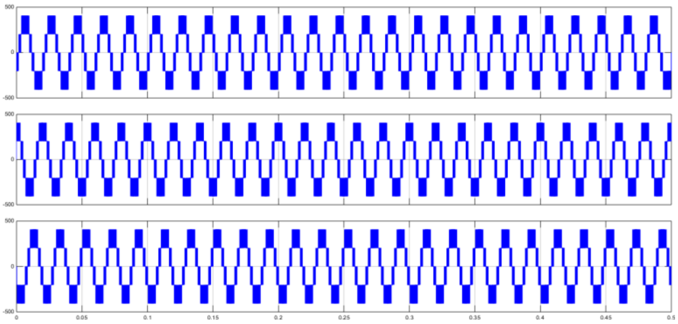

Figure.12 output line voltages of the inverter

The output line voltages are of 398V magnitude peak to peak as shown in figure 12 for the DC input of 415V and the line current are as shown in figure 13 with a magnitude of 30A.

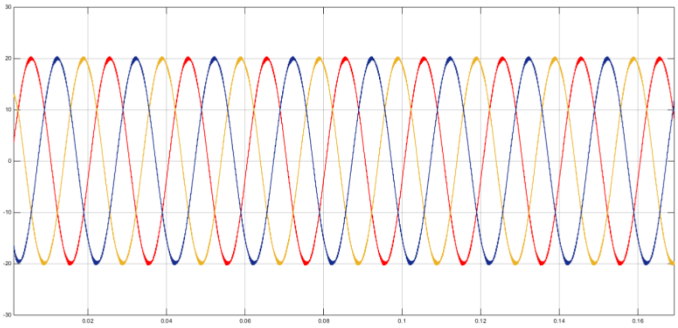

Figure.13 output currentsat the load

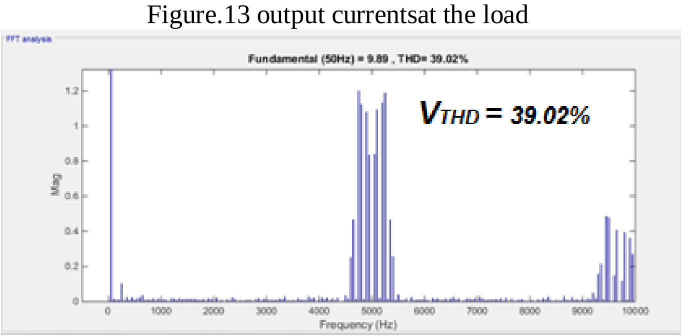

Figure 14 THD for unipolar PWM

The total harmonic distortion of the output voltage is about 39.02% for unipolar PWM technique with perfect voltage and current shapes.

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B.SVPWM Technique applied to inverter

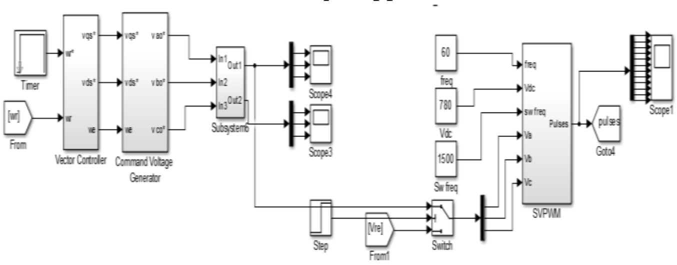

Figure 15. Proposed SVPWM Technique

The figure 15 shows the proposed SVPWM control strategy as per the theory stated above in part B. The corresponding switch states are shown in figure 16

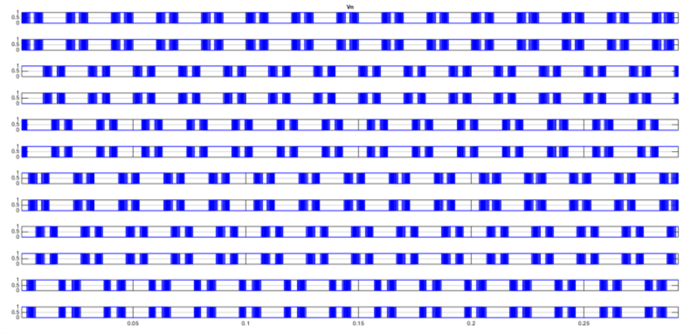

Figure 16. Switching pulses

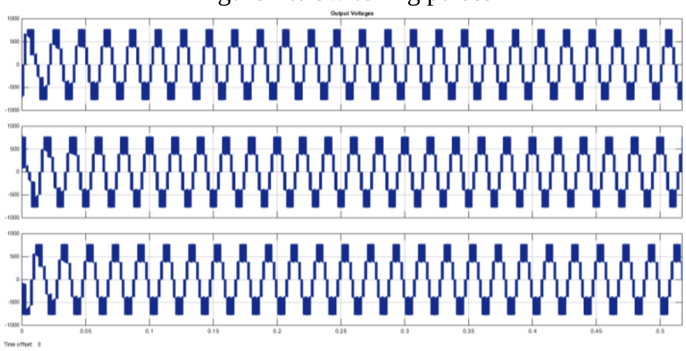

Figure 17. Output Phase voltages of the inverter for SVPWM

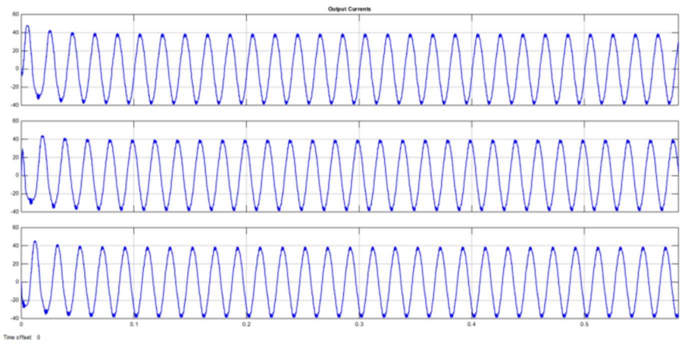

Figure. 18 output currents of the load

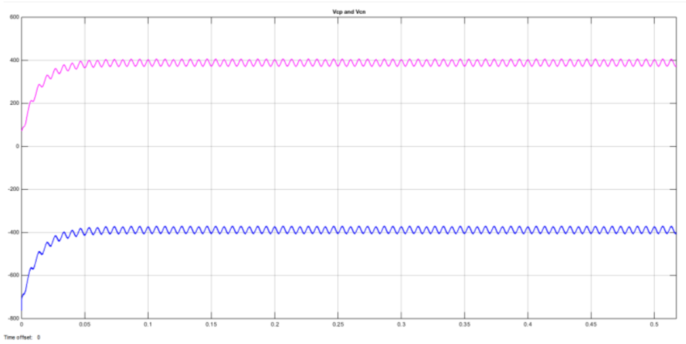

Figure.19 voltages across the split capacitor

The output voltage of the inverter for line to line is about 410V when using SVPWM. The voltages and currents are as per load requirement. Here in figure 19 one can observe the voltages across the split combination. It is so clear that SVPWM with redundant switching states the capacitor voltages are balanced.

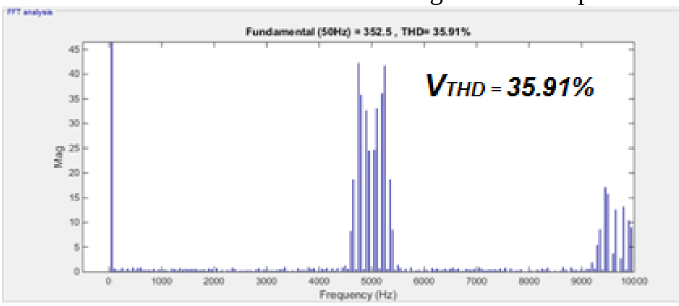

Figure 20. THD for SVPWM technique

The total harmonic distortion of the output voltage is about 35.91% when using SVPWM technique on three-level diode clamped multi-level inverter.

IV. CONCLUSION

In this paper the comparison of two most proffered control strategies applied to three phase three-level diode clamped inverter are presented. The waveforms clearly depicting that almost all the two control strategies are functioning well in controlling the split capacitor voltage balance, output voltage and currents. But THD of the two strategies when compared, it is obvious that SVPWM is the most efficient control strategy with low THD of about 35.91% among those two. The output voltage quantity and split capacitor voltage balance are better when using SVPWM.

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